RF Power Potential of 45 nm CMOS Technology

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***Abstract* − This paper presents the first measurements of the RF power performance of 45 nm CMOS devices with varying device widths and layouts. We find that 45 nm CMOS can deliver a peak output power density of around 140 mW/mm with a peak power-added efficiency (PAE) of 70% at 1.1 V. The PAE and P_{out} decrease with increasing device width because of a decrease in the maximum oscillation frequency (f_{max}) for large width devices. The PAE also decreases with increasing frequency because of a decrease in gain as the operating frequency approaches f_{max}. The RF power performance of 45 nm devices is shown to be very similar to that of 65 nm devices.**

I. Introduction

The remarkable improvement in the frequency response of silicon CMOS devices in recent years has motivated their use in millimeter-wave power applications. Specific applications in the millimeter-wave regime include high capacity wireless LAN, short-range high data-rate wireless personal area networks, and collision avoidance radar for automobiles. Using silicon CMOS for these applications allows for higher levels of integration and lower cost. Also, special circuits for improving efficiency and linearity of power amplifiers can be easily integrated into CMOS.

The state-of-the-art technology for 60 GHz power amplifier designs today is the 65 nm technology [1-2]. Recently a few research groups have demonstrated 60 GHz power amplifiers in 45 nm technologies [3-4]. However, a detailed study of the power performance of 45 nm technology has not been published so far.

In this paper, we present a comprehensive study of the RF power performance of 45 nm low-power CMOS devices. Device structures with different layouts and widths are studied to understand the effect of device geometry on RF power performance. A comparison of the RF power capability of 45 nm and 65 nm technologies is also presented. We show that PAE and P_{out} decrease with increasing device width because of a reduction in f_{max}. The RF power performance of 45 nm devices is shown to be very similar to that of 65 nm devices.

II. TECHNOLOGY

The devices used in this study are 45 nm low-power CMOS [5, 6] and 65 nm CMOS [7] devices from IBM. The 45 nm devices all have a gate length of 40 nm and V_{DD} = 1.1 V, while the 65 nm devices have a gate length of 50 nm and V_{DD} = 1 V. For the 45 nm devices, the device width is increased by either (a) keeping the number of fingers (NF) constant (NF=60) and increasing the unit finger width (WF) from 0.5 µm to 5 µm, or (b) keeping the finger width constant (WF=1.5 µm) and increasing NF from 20 to 120. For the 65 nm devices, the device width is increased by connecting multiple unit cells in parallel. Each unit cell has 12 fingers of 2 µm finger width.

S-parameter measurements from 0.5 GHz to 40 GHz were performed using an Agilent 8510C. The S-parameter data was de-embedded using on-wafer open and short de-embedding structures that were custom designed for each device. RF power measurements were made in the 2 GHz – 18 GHz range using a Maury Microwave load-pull system. Unless otherwise indicated, all S-parameter and power measurements were done at V_{DS} = V_{DD} and V_{GS} set to ensure an identical DC drain current density across devices under low input power conditions..

III. 45 nm Measurements

S-parameter and RF power measurements were made on 45 nm device structures with different geometries in an effort to understand the effect of device layout and width on RF power performance.

The first set of test structures explores the effect of contacting the gate at one end or at both ends of the gate finger. Fig. 1 compares the de-embedded f_T and f_{max} of a single gate contact structure with that of a double gate contact structure as a function of bias current. A double

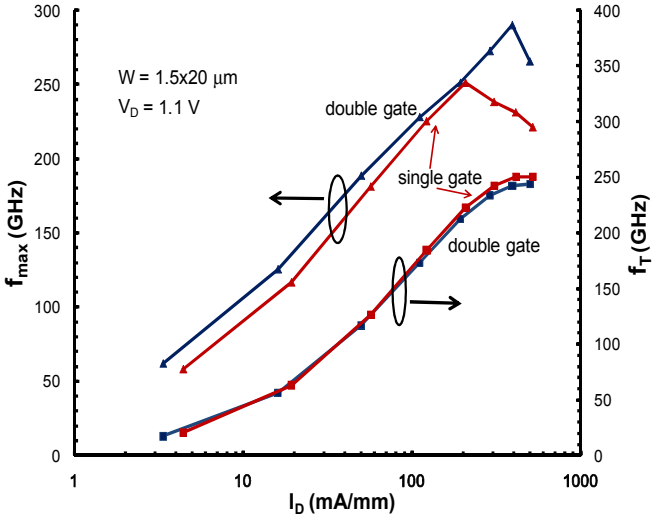

Fig. 1: f_T and f_{max} as a function of drain current density for single and double gate contact structures.

gate contact results in a significantly lower gate resistance, but a slightly higher gate capacitance. This leads to a slightly lower f_T for the double gate contact structure compared to single gate contact at the same drain current density. However, f_{max} is higher in the double gate contact structure because the reduction in gate resistance more than compensates for the increase in gate capacitance. The improvement in f_{max} is more pronounced at higher current densities.

Fig. 2 shows the PAE and normalized output power (P_{out}/W), measured at I_D = 200 mA/mm and V_{DD} = 1.1 V, as a function of measurement frequency for the single and double gate contact structures. The load and source impedances were tuned for optimum PAE and the output power and PAE were measured at peak PAE. The PAE for the double gate contact is similar to that of the single gate contact structure. The PAE is also remarkably frequency independent. The output power is slightly higher for the double gate contact structure.

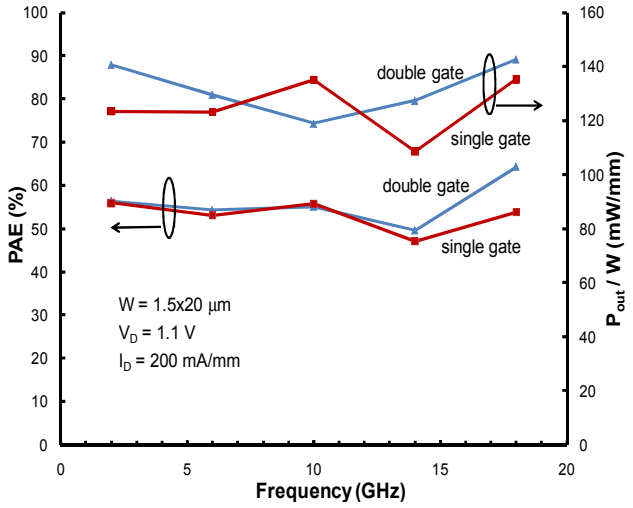

Fig. 2: PAE and normalized output power as a function of measurement frequency for single gate and double gate contact structures.

Fig. 3 shows the impact of number of fingers (NF) and finger width (WF) on de-embedded f_{max}. The devices with the same WF are connected by solid lines. The numbers beside each symbol denote the number of fingers in that device. All devices used in this study and in the rest of the paper have double gate contacts. It is clear from Fig. 3 that f_{max} decreases with increasing total device width. For a given NF, increasing WF initially leads to an increase in f_{max} but eventually f_{max} decreases as the gate resistance increases. The optimum unit finger width for this technology is 1.5 µm. On the other hand, for a given WF, increasing NF leads to a decrease in f_{max}. This is because of the increased parasitic resistance resulting from the additional wiring needed to connect all the fingers in parallel.

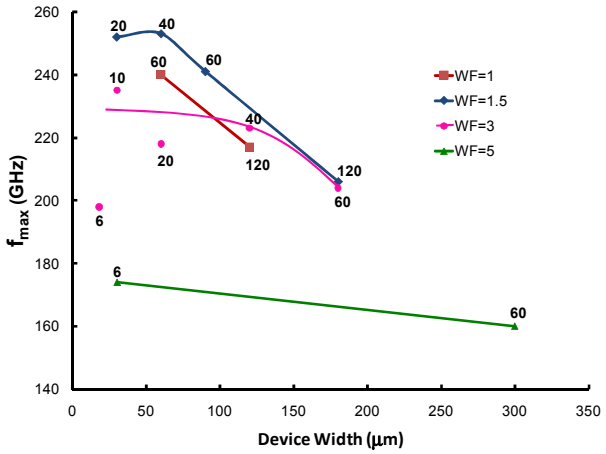

Fig. 3: f_{max} as a function of total device width. The numbers beside each symbol denote the number of fingers in that device. V_{DD} = 1.1 V, I_D = 200 mA/mm.

The peak PAE for the NF=60 structures is shown as a function of total device width for different measurement frequencies in Fig. 4. PAE increases with width for small device widths (W < 100 µm) because of an increase in power gain as a result of lower relative parasitics. For W > 100 µm, PAE is constant with width at lower frequencies but tends to decrease with width at higher frequencies because of the reduction in gain with frequency.

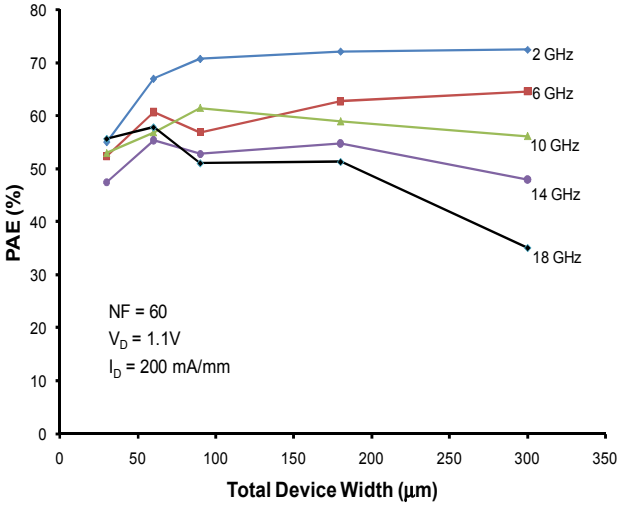

Fig. 4: PAE, measured at different frequencies, as a function of total device width. Device width is increased by keeping NF constant at 60 and increasing WF from 0.5 µm to 5 µm.

Fig. 5 shows the corresponding normalized output power as a function of total device width. The output power shows no clear dependence on frequency, as expected, but shows a gentle decrease with increasing width. This decrease in output power at large widths is because of a decrease in gain and f_{max}.

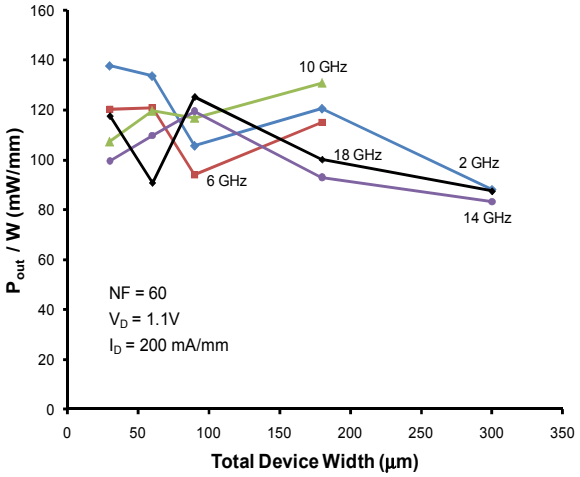

Fig. 5: Normalized output power, measured at different frequencies, versus total device width. Device width is increased by keeping NF constant at 60 and increasing WF from 0.5 µm to 5 µm.

Fig. 6 shows the peak PAE versus device width for structures in which WF=1.5 µm and the device width is increased by increasing the number of fingers from 20 to 120. Similar to Fig. 4, but to a smaller scale, the peak PAE initially increases with width for W < 100 µm and remains constant for W > 100 µm. PAE also decreases with increasing frequency. The change in PAE is mainly due to the change in the power gain.

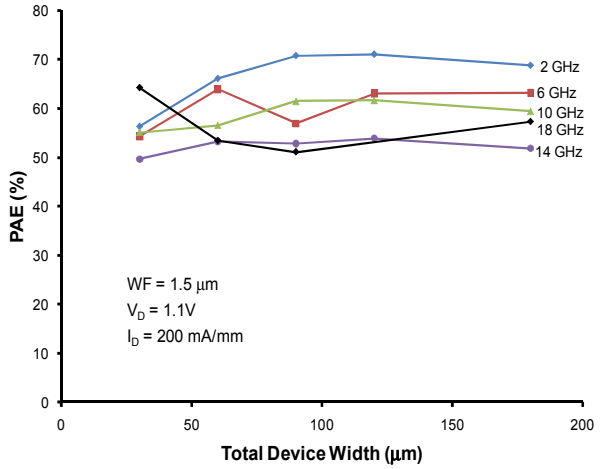

Fig. 6: PAE, measured at different frequencies, as a function of total device width. Device width is increased by keeping WF constant and increasing NF from 20 to 120.

The corresponding normalized output power is shown as a function of total device width in Fig. 7. The output power shows a slight decrease with increasing device width but is rather independent of frequency. This is further discussed below.

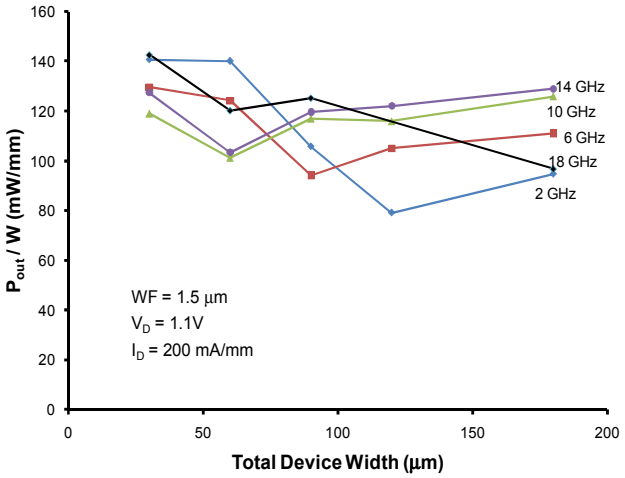

Fig. 7: Normalized output power, measured at different frequencies, versus total device width. Device width is increased by keeping WF constant and increasing NF from 20 to 120.

IV. Comparison of 45 nm and 65 nm Technologies

We now compare the RF power performance of 45 nm low-power devices with 65 nm devices. Fig. 8 shows the de-embedded f_{max} as a function of device width for both 45 nm and 65 nm technologies. For 45 nm devices, NF=60 and the device width is increased by increasing WF from 0.5 µm to 5 µm (same data as in Fig. 3). For the 65 nm devices, the device width is increased by connecting multiple unit cells in parallel. Each unit cell has 12 fingers of 2 µm finger width. It is clear from Fig. 8 that f_{max} is slightly higher for the 45 nm devices with W < 100 µm. However, at large device widths f_{max} of 45 nm devices is lower than 65 nm devices. This is because the finger width for the 45 nm devices is large (> 3 µm), which results in a rather high gate resistance and thus reduced f_{max}. There is no reason that prevents 45 nm technologies from achieving higher f_{max} at large device widths by using optimized values of WF. This should boost its maximum power handling ability.

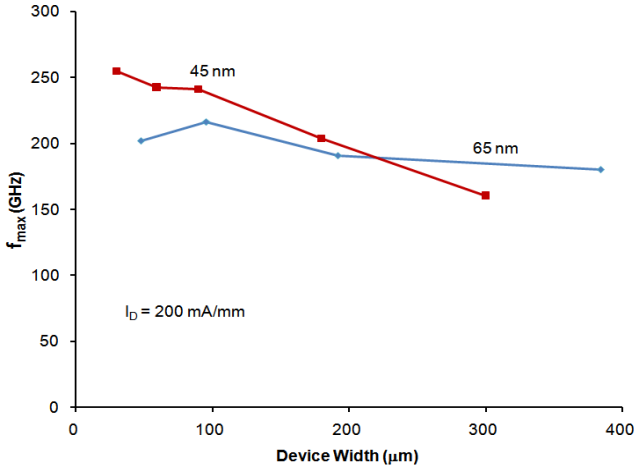

Fig. 8: f_{max} as a function of device width for 45 nm and 65 nm devices. V_{DD} = 1.1 V for 45 nm and V_{DD} = 1 V for 65 nm.

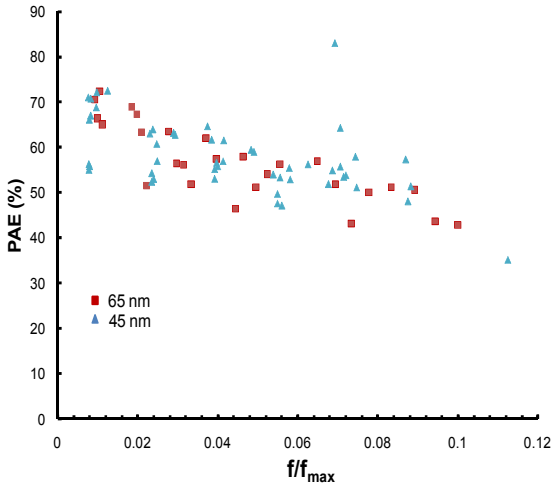

Fig. 9: Dependence of peak PAE on the f/f_{max} ratio for 45 nm and 65 nm devices. I_D=200 mA/mm, V_{DD} = 1.1 V for 45 nm, V_{DD} = 1 V for 65 nm.

An alternative way to compare the RF power performance of 45 and 65 nm technologies is to focus on PAE and P_{out} at different frequencies as a function of the ratio of the application frequency to the f_{max} of the device. The higher the f/f_{max} ratio, the closer the device is operating to its frequency limit. As the operating frequency approaches f_{max}, the power gain decreases, resulting in a decrease in the peak PAE [8]. Fig. 9 shows peak PAE, measured at I_D=200 mA/mm, as a function of f/f_{max} for both 45 nm and 65 nm devices. When viewed this way, both CMOS technologies behave in a very similar way.

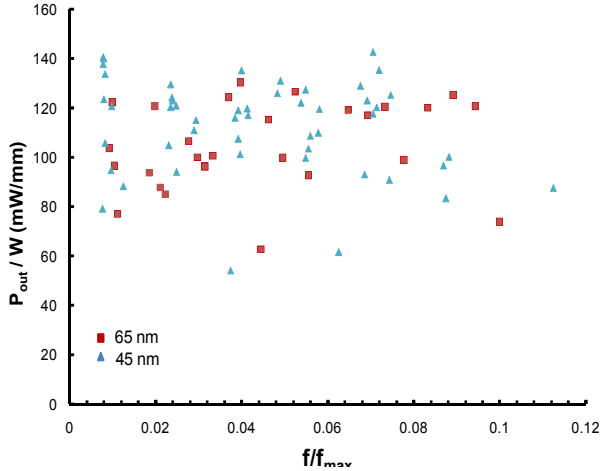

Fig. 10: Normalized output power versus f/f_{max} ratio for 45 nm and 65 nm devices. I_D=200 mA/mm, V_{DD} = 1.1 V for 45 nm, V_{DD} = 1 V for 65 nm.

Fig. 10 shows the normalized output power as a function of f/f_{max} for 45 nm and 65 nm devices. The output power is relatively constant across measurement frequency for both devices. There is also a slightly higher output power in the 45 nm devices which can be attributed to the higher V_{DD} (1.1 V for 45 nm versus 1 V for 65 nm).

Hence, we conclude that the RF power performance of 45 nm low-power technology is very similar to that of 65 nm technology. This is not surprising because the gate lengths for both technologies are close and f_{max} is already quite high (> 200 GHz) for 65 nm technology. Most of the 60 GHz applications require a significant amount of digital content. Our research suggests that designers can take advantage of the higher integration density of 45 nm CMOS without losing any of the RF power performance of 65 nm technology.

V. CONCLUSION

We have studied the power and frequency response of 45 nm low-power CMOS devices. Our data shows that the peak output power density in these devices, at I_D=200 mA/mm, is around 140 mW/mm and the peak PAE is over 70%. A device structure with a double gate contact shows a slight improvement in f_{max} and P_{out} compared to a single gate contact structure. Increasing the device width leads to a decrease in PAE and P_{out} due to a decrease in f_{max} for large width devices. For a given device width, f_{max}, PAE and P_{out} are independent of the number of fingers and unit finger width as long as the unit finger width is less than 1.5 µm. Comparison of frequency and power data of 45 nm and 65 nm devices shows that the RF power potential of 45 nm low-power technology is very similar to that of 65 nm technology.

REFERENCES

[1] W.L. Chan et al, "A 60GHz-band 1V 11.5dBm power amplifier with 11% PAE in 65nm CMOS", *International Solid State Circuits Conference*, 2009, pp. 380 – 381.

[2] A. Valdes-Garcia et al, "60 GHz transmitter circuits in 65nm CMOS", *Radio Frequency Integrated Circuits Symposium*, 2008, pp. 641-644.

[3] K. Raczkowski, et al, "50-to-67GHz ESD-Protected Power Amplifiers in Digital 45nm LP CMOS", *International Solid State Circuits Conference*, 2009, pp. 382 – 384.

[4] E. Cohen, et al, "60GHz 45nm PA for Linear OFDM Signal with Predistortion Correction achieving 6.1% PAE and -28dB EVM", *Radio Frequency Integrated Circuits Symposium*, 2009, pp. 35-38.

[5] J. Yuan, et al, "A 45nm low cost low power platform by using integrated dual-stress-liner technology", *VLSI technology symposium*, 2006, pp. 100-101.

[6] U. Gogineni, et al, "Effect of substrate contact shape and placement on RF characteristics of 45 nm low-power CMOS devices", *Radio Frequency Integrated Circuits Symposium*, 2009, pp. 163-166.

[7] Z. Luo, et al, "High performance and low power transistors integrated in 65nm bulk CMOS technology", *International Electron Device Meeting*, 2004, pp. 661-664.

[8] J. Scholvin, et al, "Fundamental power and frequency limits of deeply-scaled CMOS for RF power applications", *International Electron Device Meeting,* 2006, pp. 217-220.