Chapter 3
Device Physics and Performance Potential of III-V Field-Effect Transistors

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Abstract The device physics and technology issues for III-V transistors are examined from a simulation perspective. To examine device physics, an InGaAs HEMT structure similar to those being explored experimentally is analyzed. The physics of this device is explored using detailed, quantum mechanical simulations based on the non-equilibrium Green's function formalism. In this chapter, we: (1) elucidate the essential physics of III-V HEMTs, (2) identify key technology challenges that need to be addressed, and (3) estimate the expected performance advantage for III-V transistors.

3.1 Introduction

Driven by tremendous advances in lithography, the semiconductor industry has followed Moore's law by shrinking transistor dimensions continuously for the last 40 years. The big challenge going forward is that continued scaling of planar, silicon, CMOS transistors will be more and more difficult because of both fundamental limitations and practical considerations as the transistor dimensions approach ten nanometers. The issues at small gate lengths are many fold. First, transistor scaling increases the number of gates on a chip and the operating frequency. To prevent the chip from overheating, the power dissipation should be limited, which requires lowering the power supply voltage while maintaining the ability to deliver high on-currents for each new generation of technology. Secondly, the drain bias decreases the energy barrier height between the source and channel in a transistor due to 2D electrostatics. Degraded short channel effects become more significant as the gate length gets shorter, and the increased off-state leakage has pushed the stand-by power to its practical limit. Thirdly, the accompanying scaled oxide thickness provides better gate control of the channel potential, but this inevitably increases

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the gate leakage and makes it very difficult to obtain both high on-currents and low off-currents at lowered supply voltage. Lastly, the parasitic resistance and capacitance have become comparable to, or even larger than the continuously decreasing intrinsic channel capacitance and resistance, which may provide a practical limit to scaling [1]. A 45 nm process based on high-k, metal gate, and strained silicon was introduced in 2007 [2]. With such technologies, scaling will continue to the 32 nm node and beyond [3]. Conventional silicon-based CMOS scaling will, however, become very difficult at the 15 nm node and beyond. Further improvements in transistor speed and performance may have to come from new channel materials.

To address the scaling challenge, both industry and academia have been investigating alternative device architectures and materials, among which III-V compound semiconductor transistors stand out as promising candidates for future logic applications because their light effective masses lead to high electron mobilities and high on-currents, which should translate into high device performance at low supply voltage. Recent innovations on III-V transistors include sub-100 nm gate-length, high performance InGaAs buried channel [4, 5] and surface channel MOSFETs [6], sub-80 nm E-mode InGaAs/InAs HEMTs [7–10], and InSb p-channel HEMTs [11] with outstanding logic performance at short channel lengths and low supply voltages. At the same time, theoretical work has predicted the performance of III-V transistors with respect to Si at near future technology nodes with the focus on device design, bandstructure effects, source engineering, etc [12–21].

In this chapter, we will examine device physics issues of III-V transistors from a simulation perspective by addressing a very specific question: how would an In-rich, InGaAs MOSFET operate if the technological challenges identified in other chapters of this volume are solved. To examine device physics, we will use an InGaAs HEMT structure similar to that being used by the MIT and Intel groups [10, 22]. We will begin by examining the device physics using detailed quantum mechanical simulations based on the non-equilibrium Green's function formalism [23]. Our objectives are threefold: (1) to elucidate the physics of III-V HEMTs, (2) to identify key technology challenges that need to be addressed, and (3) to determine what the performance advantage (if any) for III-V transistors would be.

3.2 InGaAs HEMTs

3.2.1 Device Structure

The HEMT structure for logic applications studied in this chapter is shown in Fig. 3.1a [22]. The high-mobility channel consists of $In_{0.53}Ga_{0.47}As/In_{0.7}Ga_{0.3}As/In_{0.53}Ga_{0.47}As$ quantum well of 2 nm/8 nm/3 nm in thickness and is sandwiched between two $In_{0.52}Al_{0.48}As$ barrier layers on the top and bottom with thickness of 4 nm and 500 nm respectively. The gate length of these devices ranges from 40 to 130 nm.

A silicon δ-doped layer of $5 \times 10^{12}\,cm^{-2}$ is placed 3 nm away from the channel in the upper barrier layer to provide carriers for the source and drain. In real devices,

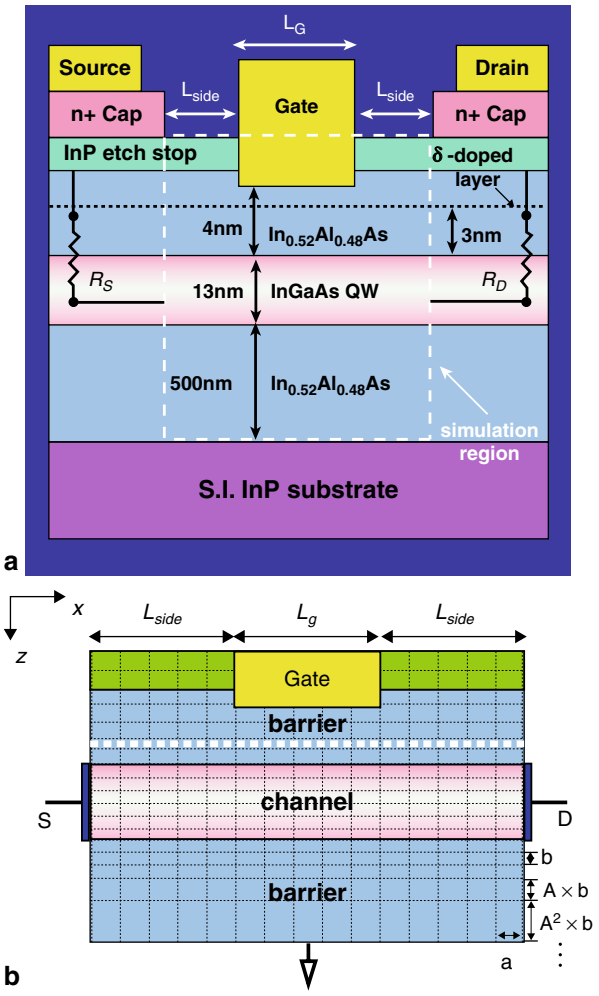

Fig. 3.1 **a** The structure of the MIT InGaAs HEMTs designed for logic application (after [22]). The simulation domain is indicated by the *dashed square* which is modeled with quantum ballistic transport. The heterostructure stack is simply replaced with two series resistances. **b** The simplified device structure with proper boundary conditions. The delta-doped layer is indicated by the *white dashed line*

the current flow is 2D from the raised source to the drain through the doped heterostructure stack and then laterally to the channel. Rather than attempting to simulate the contacts and the associated metal semiconductor contact resistance, we place ideal contacts at the two ends of the channel to simplify the structure. The simulated "intrinsic" device structure, where quantum ballistic transport is expected to dominate, is indicated by the dashed square in Fig. 3.1a. The effects of the heterostructure contact stack on the intrinsic device are approximated by simply adding two series resistance R_S and R_D to both ends. This approach neglects some source design issues such as source access [24] and so-called source starvation [14] that may be important in practice. Nevertheless, it is a reasonable starting point and should provide us with upper limit projections. The comparisons with experiment to be discussed later show that neglecting source design issues is acceptable at this stage of technology development.

3.2.2 Simulation Approach

The 2D simulation program used for these studies evolved from the nanoMOS simulation program [25]. The Poisson equation is first solved with the charge from an initial flat band profile as the estimated potential. To compute the carrier density, the uncoupled mode space approach is then used to solve the quantum transport problem assuming ballistic transport. The resulting spatial charge distribution from the 2D charge density weighed by the wavefunction in the quantum well is inserted in the Poisson equation, and the new charge distribution leads to a new potential profile. This process continues until the desired convergence is achieved (typically when the maximum difference in potential for the last two iterations is under 0.1 meV). The quantum ballistic current is then readily calculated for each subband within the mode space NEGF formalism. Final post-processing steps utilize the two fitting parameters (the metal work function and the series resistance) to fit the simulation results to the experimental data. The simulation procedure was discussed in detail in [26]. Note that different from [26], we adopt an embedded gate structure to capture the fringing effects which become important in short gate length devices. Figure 3.1b shows the simplified device structure in the simulation with the following boundary conditions: (1) the potential of the embedded gate region is fixed according to the gate bias and workfunction, (2) the bottom layer of the substrate is grounded, and (3) zero normal electrical field boundary conditions are applied for the rest of the boundary.

3.2.3 Materials Parameters

Non-parabolicity effects are important in the conduction band of III-V materials, and the use of bulk effective masses would lead to significant errors for ultra-thin-body structures [27]. Before simulating the HEMTs, we extract the channel effective masses of the III-V HEMT devices from atomistic $sp^3d^5s^*$ tight-binding simulations using the NEMO-3D program [28]. The bandstructure calculated with the atomistic tight-binding model incorporates the non-parabolicity effects as well as the strain effects due to the lattice mismatch between the $In_{0.53}Ga_{0.47}As/In_{0.7}Ga_{0.3}As$ layers. The tight-binding bandstructure calculation also shows that higher valleys are well above the Γ valley subbands and therefore make a negligible contribution to the carrier and current density. The effective mass is extracted from the first subband by fitting a parabola from the band bottom to up to 0.1 eV higher. The extracted equivalent effective masses for the quantum well channel are $0.053m_0$ for transport and transverse directions, and $0.067m_0$ for the confinement direction, in contrast with the value of $0.041m_0$ obtained from a linear interpolation of the bulk effective masses of InAs and GaAs [29]. The confinement effective mass of $In_{0.52}Al_{0.48}As$ barrier is $0.075m_0$. The dielectric constant of the InGaAs channel used in the simulation is assumed to be $\varepsilon = 14.3$ and that of the $In_{0.52}Al_{0.48}As$ barrier is 12.7 [29]. The conduction band discontinuity between $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ layers is assumed to be $\Delta E_C = 0.50$ eV [30, 31].

3.2.4 Results

We compare the simulation results with experimental data by examining the *I–V* characteristics. Two fitting parameters are used: (1) the workfunction of the gate metal and (2) the series resistance. The gate workfunction is first determined by tuning its value so that the subthreshold regime of the intrinsic $\log I_d$–V_{GS} overlaps that of the experimental data. Below subthreshold, the current is so small that the *I–V* characteristics are not affected by the series resistance. Once we fit the subthreshold regime by determining the gate workfunction, we choose an appropriate series resistance to include in the ballistic intrinsic *I–V* and adjust to best match the linear region within the above-threshold I_d regime (low V_{DS} and high V_{GS}).

Figure 3.2 compares the simulation with the experimental data [32] in $\log I_d$–V_{GS} and linear I_d–V_{DS} plots for nominal gate lengths of L_g = 40 nm and L_g = 130 nm InGaAs HEMTs after tuning the workfunction and including the series resistance. Good quantitative agreement is achieved with adjustment of the nominal gate length and insulator thickness by about 10%. For the device with a nominal gate length of L_g = 40 nm and t_{ins} = 4 nm, the best fit was obtained with L_g = 45 nm and t_{ins} = 3.6 nm. For the device with a nominal gate length of 130 nm a t_{ins} = 4 nm, the best fit was obtained with L_g = 125 nm and t_{ins} = 4.6 nm. These values are within the measurement error and reasonable [33]. The fitted series resistance $R_S = R_D$ = 220 Ω μm is identical to the value quoted from the measurement [34]. We also observe that the difference in current between experimental data and simulation

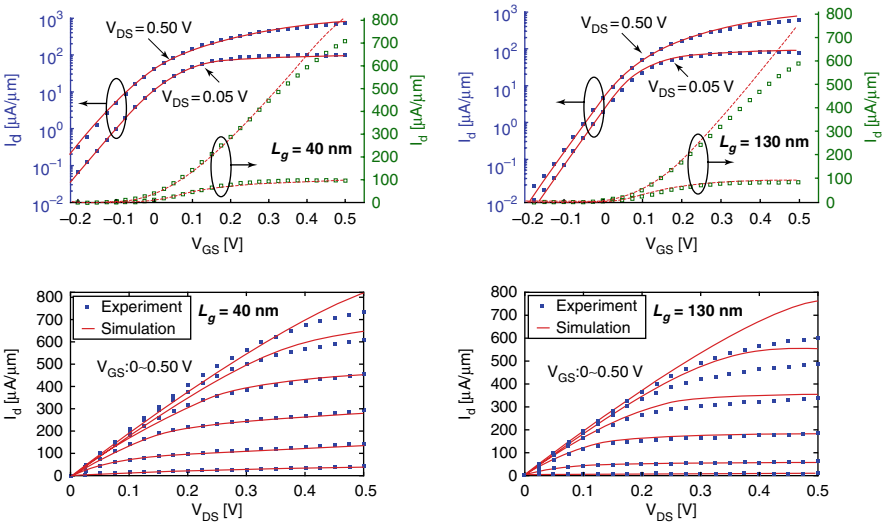

Fig. 3.2 Comparison of the *I–V* characteristics between experimental (*square symbols*) and simulation results (*solid and dash lines*) for 40 nm (*left*) and 130 nm (*right*) HEMTs shows quantitatively good agreement by adjusting the gate length and insulator thickness in a reasonable range

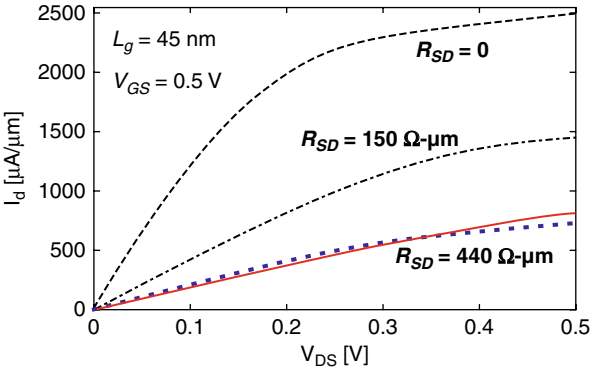

Fig. 3.3 I_d–V_{DS} of 45 nm HEMTs at $V_{GS} = 0.5$ V with different series resistance; the *square symbols* are experimental data. The on-current is expected to be improved by about 100% with reduced series resistance matched to Si transistors

results at high V_{DS} increases as both V_{GS} and L_g increases, which might be due to three reasons. First, the assumed constant series resistance used in the simulation might not hold when the current becomes large. Second, as the gate length increases from 40 to 130 nm the device may become less ballistic. Finally the source may not be able to supply the desired on-current. Nevertheless, the simulation demonstrates that the ballistic model with attached series resistance is a good first order description of the HEMTs' *I–V* characteristics.

Note that the series resistance in these transistors is quite large, and it presents a significant limit on device performance. This is shown in Fig. 3.3, where the simulated I_d–V_{DS} for $L_g = 45$ nm at $V_{GS} = 0.5$ V is compared for different assumed values of R_{SD} (the square symbols are experimental data for the nominal $L_g = 40$ nm device). It is observed that the predicted on-current could be improved by 100% if the series resistance in III-V HEMTs could be reduced to the typical value for good Si transistors ($R_{SD} \sim 150\,\Omega\,\mu$m). Note also that even the fully ballistic simulation displays a channel resistance of about 80 Ω μm.

3.3 Discussion

3.3.1 Gate Capacitance

The gate capacitance of the HEMTs can be determined from the charge in the quantum well channel. Figure 3.4a shows the simulated carrier density (half-way between the source and drain) vs. the gate bias at $V_{DS} = 0$ when $L_g = 45$ nm and $t_{ins} = 3.6$ nm; the slope of the curve gives a gate capacitance of 1.41 μF/cm^2 at $V_{GS} = 0.5$ V. The gate capacitance is the upper barrier layer insulator capacitance in series with the semiconductor capacitance:

$$\frac{1}{C_G} = \frac{1}{C_{ins}} + \frac{1}{C_S}, \tag{3.1}$$

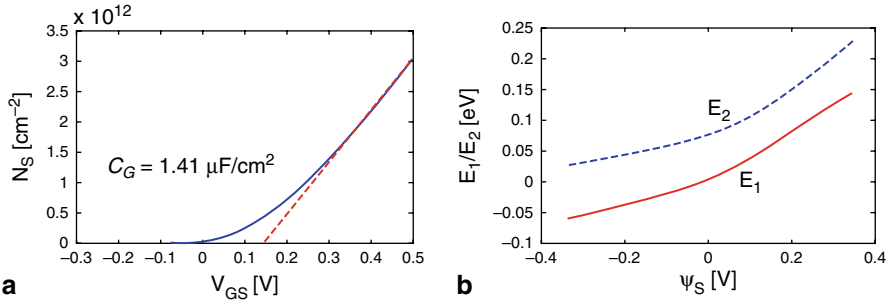

Fig. 3.4 **a** The charge density in the quantum well gives $C_G = 1.41\,\mu F/cm^2$ at $V_{GS} = 0.5\,V$. **b** The 1st and 2nd subband energy as a function of the surface potential of the quantum well

where $C_{ins} = \dfrac{\varepsilon_{ins}}{t_{ins}} = 3.12\ \mu F/cm^2$. The semiconductor capacitance C_S can be expressed as [35]:

$$C_S = \frac{q^2 m^*}{\pi \hbar^2} \cdot \sum_i f\,(E_i; E_F) \cdot (1 - \partial E_i / \partial \psi_S), \tag{3.2}$$

where $C_Q = q^2 m^* / \pi \hbar^2$ is the so called quantum capacitance at 0 K in a 2D system, $f\,(E_i; E_F)$ is the Fermi function for subband i, and $\partial E_i / \partial \psi_S$ is the change of the ith subband energy E_i with respect to the surface potential ψ_S. Equation (3.2) may be viewed as the product of C_Q and a factor that depends on how the shape of the quantum well changes with gate bias. The second factor is often interpreted as describing how the centroid of the charge changes with gate voltage. At $V_{GS} = 0.5\,V$ only two subbands are occupied in the quantum well, and Fig. 3.4b shows the two subband energies as a function of ψ_S . The semiconductor capacitance is then readily calculated from Eq. (3.2) as $C_S = 3.05\,\mu F/cm^2$, which is, close to the quantum capacitance $C_Q = 3.53\,\mu F/cm^2$. Using Eq. (3.1) we find $C_G = 1.54\,\mu F/cm^2$, close to $C_G = 1.41\,\mu F/cm^2$ as calculated directly from the charge in the quantum well. An independent determination of the gate capacitance obtained by de-embedding the capacitance from S-parameter measurements yields a somewhat lower value of $C_G = 1.08\,\mu F/cm^2$. The reason for this discrepancy is still not understood.

Our calculations show that C_S is comparable to C_{ins} for this transistor. We also find that $C_G < C_{ins}$. This occurs because of the small density of states effective mass in III-V materials [14, 16]. The result is a significant degradation of the total gate capacitance. One can describe this effect as an effective increase of the insulator thickness according to

$$C_G = \frac{\varepsilon_{ins}}{t_{ins} + \Delta t_{ins}}. \tag{3.3}$$

For the device being studied here, $t_{ins} = 3.6\,\text{nm}$ and $\Delta t_{ins} = 4.4\,\text{nm}$, so the low density-of- states seriously degrades the gate capacitance.

3.3.2 Charge Control in a Nanoscale HEMT

The current of nanoscale MOSFETs can be accurately described by a virtual source model as [1]

$$I_D/W = Q_i(x_0) \cdot \langle \upsilon\,(x_0) \rangle \tag{3.4a}$$

where I_D is the drain current, W is the device width, and $Q_i(x_0)$ is the charge per unit area at the virtual source. In the ballistic limit, the virtual source model becomes the top-of-the-barrier ballistic model [36, 37] and for on-current conditions,

$$I_{ON}/W = Q_i(x_0) \cdot \upsilon_{inj} \tag{3.4b}$$

where $\langle \upsilon\,(x_0) \rangle = \upsilon_{inj}$ is the so-called ballistic injection velocity and is a key figure of merit for nanoscale MOSFETs [1].

When analyzing experimental results, the charge at the virtual source (top of the barrier) and injection velocity at the same location are estimated. Consider first the charge at the virtual source. It can be estimated from experiment C–V (long channel) from [38, 39]

$$Q_i(x_0) = \int_0^{V_{gs}^*} C'_{gsd}\Big|_{V_{ds}=(\text{long-chan.})} dV_{gs}, \tag{3.5}$$

where $V_{gs}^* = V_{gs} + \Delta V_T - I_{on}R_S$ accounts for the correction of V_T roll-off, *DIBL*, and series resistance.

For the 45 nm HEMTs studied here, the simulated on current at $V_{GS} = V_{DS} = 0.5\,\text{V}$ is $I_{ON}/W = 813\,\mu\text{A}/\mu\text{m}$, the intrinsic biases are $V_{GS,in} = 0.32\,\text{V}$, $V_{DS,in} = 0.14\,\text{V}$ with $R_S = R_D = 220\,\Omega\,\mu\text{m}$. Figure 3.5 plots the first subband profile vs. position along with the electron density vs. position as a function of position along the

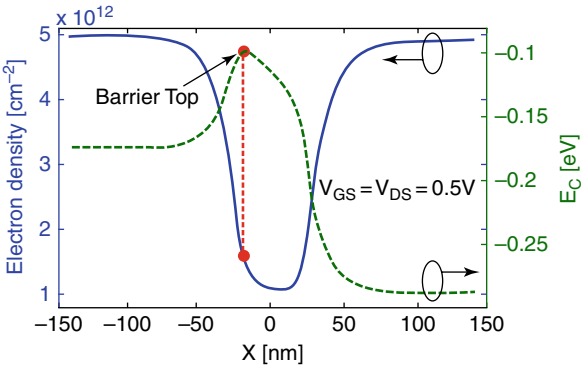

Fig. 3.5 The sheet charge density at the virtual source is determined from the spatial sheet charge density at the top of the potential barrier

device channel. From this plot, we find the charge at the virtual source (top of the potential barrier) to be $1.60 \times 10^{12}\,\mathrm{cm}^{-2}$. From Eq. (3.5) and the intrinsic simulated C–V of a long channel device ($L_g = 125\,\mathrm{nm}$), the electron density extracted at $V_{GS} = V_{DS} = 0.5\,\mathrm{V}$ is about $1.90 \times 10^{12}\,\mathrm{cm}^{-2}$, which is reasonably close to the charge density obtained directly from the top of the potential barrier. As will be discussed in Sect. 3.3.7, the charge at the top of the barrier under high drain bias is less than the equilibrium charge because the semiconductor capacitance is reduced under high drain bias.

3.3.3 Velocity at the Virtual Source

The ballistic injection velocity υ_{inj} is of particular interest in MOSFETs, and can be evaluated at the top of the source-channel potential barrier ($x = x_0$):

$$I_D/W = Q_i(x_0) \cdot \upsilon_{inj} \tag{3.6}$$

where I_D, W, and $Q_i(x_0)$ have the same meaning as in Eq. (3.4a). For the 40 nm HEMTs studied, the on current at $V_{GS} = V_{DS} = 0.5\,\mathrm{V}$ is $I_{ON}/W = 813\,\mu\mathrm{A}/\mu\mathrm{m}$, the intrinsic biases are $V_{GS,in} = 0.32\,\mathrm{V}$, $V_{DS,in} = 0.14\,\mathrm{V}$ with $R_S = R_D = 220\,\Omega\,\mu\mathrm{m}$. Figure 3.6 plots the first subband profile and average velocity as a function of position along the device channel. The ballistic injection velocity is readily read from the average velocity at the top of the barrier, which gives $\upsilon_{inj} = 3.17 \times 10^7\,\mathrm{cm/s}$, and is close to the experimental reported value [40]. In comparison, the injection velocity extracted with the simulated on-current ($813\,\mu\mathrm{A}/\mu\mathrm{m}$) and the charge from the integration of the long channel device C–V as in last section ($1.90 \times 10^{12}\,\mathrm{cm}^{-2}$) is $\upsilon_{inj} = 2.67 \times 10^7\,\mathrm{cm/s}$. Note that the III-V HEMTs have much larger ballistic injection velocity than that of the strained Si MOSFETs in spite of the small intrinsic gate and drain biases in III-V HEMTs that result from the large series resistance.

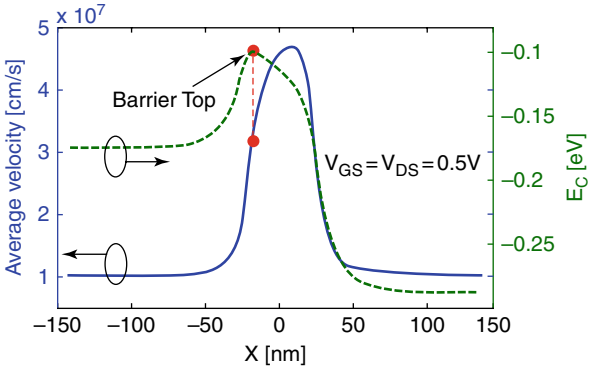

Fig. 3.6 The ballistic injection velocity is the average velocity at the top of the potential barrier

3.3.4 Ballistic Mobility

The "ballistic mobility" is a reflection of the ballistic quantum contact conductance, and imposes severe limitation on the apparent channel mobility in III-V transistors when the gate length scales down to ballistic regime. The apparent channel mobility μ_{app} is defined from the linear region of the I_d–V_{DS} as

$$I_d \equiv \frac{W}{L_g}\mu_{app}C_G\left(V_{GS}-V_T\right)V_{DS}. \tag{3.7}$$

Since the current in a ballistic FET is independent of channel length, it is clear that the apparent mobility must be a channel length dependent quantity. The apparent channel mobility μ_{app} is the combination of the "ballistic mobility" μ_B and the bulk mobility μ_0 through the Mathiessen's rule [41]:

$$\frac{1}{\mu_{app}} = \frac{1}{\mu_B} + \frac{1}{\mu_0}. \tag{3.8}$$

From ballistic theory, μ_B can be calculated from

$$\mu_B = \frac{\upsilon_T \cdot L_g}{V_{DS}} \frac{\sum\limits_i \left(\Im_{1/2}(\eta_{FS,i}) - \Im_{1/2}(\eta_{FD,i})\right)}{\sum\limits_i \left(\Im_0(\eta_{FS,i}) + \Im_0(\eta_{FD,i})\right)}, \tag{3.9}$$

where $\upsilon_T = \sqrt{2k_BT/\pi m_c}$, m_c is the transport effective mass; L_g is the gate length; V_{DS} is the intrinsic drain bias; and $\Im_{1/2}(x), \Im_0(x)$, are the Fermi-Dirac integrals of order 1/2 and 0, with $\eta_{FS,i} = (E_{FS} - E_i)/k_BT$, $\eta_{FD,i} = \eta_{FS,i} - q_0V_{DS}/k_BT$. Assuming $V_{DS} \ll k_BT/q_0$, and only one subband occupied, Eq. (3.9) reduces to [42, 43]:

$$\mu_B = \frac{\upsilon_T \cdot L_g}{2k_BT/q_0} \cdot \frac{\Im_{-1/2}(\eta_{FS,1})}{\Im_0(\eta_{FS,1})}. \tag{3.10}$$

In the nondegenerate limit, the ratio of Fermi-Dirac integrals reduces to unity.

Equation (3.8) can well explain the mobility of the transistors in both ballistic and diffusive limit; when the gate length L_g is so short that the transistor is in the ballistic limit, the apparent channel mobility is just the ballistic mobility. When L_g is much longer than the mean-free-path, the device is in the diffusive limit, and L_g in Eq. (3.9) is replaced with the carrier's mean free path, λ_0, so the apparent channel mobility will be largely determined by the bulk mobility.

The ballistic mobility can also be obtained from the simulated linear ballistic I_d–V_{DS}:

$$I_d = Q_i \cdot \mu_B \cdot V_{DS}/L_g, \tag{3.11}$$

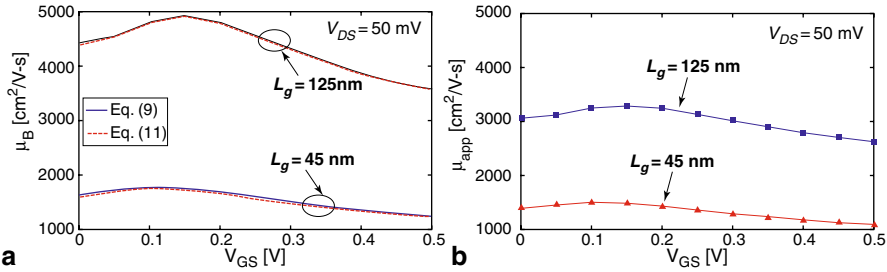

Fig. 3.7 **a** The ballistic mobilities μ_B determined from Eqs. (3.9) and (3.11) are almost identical for 45 nm and 125 nm HEMTs respectively. **b** The apparent channel mobility μ_{app} is gate length dependent and significantly degraded from the bulk mobility μ_0 (= 10,000 cm^2/V s) due to the small μ_B. The series resistance is $R_S = R_D = 220\,\Omega\,\mu$m

where Q_i is the charge density at the top of the barrier. Figure 3.7a compares μ_B vs. V_{GS} as obtained from Eqs. (3.9) and (3.11) respectively for the 45 and 125 nm HEMTs; the two methods give very close results. Note that the gate-length dependent μ_B is much smaller than the bulk mobility (~10,000 cm^2/V s), and therefore it degrades the apparent mobility significantly. This effect is shown in Fig. 3.7b, where μ_{app} is calculated from Eq. (3.8) with $\mu_0 = 10{,}000$ cm^2/V s, and plotted as a function of V_{GS} for 45 and 125 nm HEMTs. The point is that the large bulk mobilities of III-V materials will not be reflected in the apparent mobility that describes the linear region of a FET.

3.3.5 Source Design Issues

Fischetti and Laux have pointed out the importance of source design considerations such as access geometry and source starvation for III-V transistors [14, 18, 19]. The first issue refers to the fact that the source access geometry may restrict the flow of carriers into the channel. Source starvation refers to the condition when the source is unable to inject electrons into longitudinal momentum states in the channel—these states become depleted, or "starved". In addition, a third effect may also occur.

Transistors operate by modulating potential energy barriers [44, 45]. As the gate voltage increases, the potential energy barrier decreases, and the charge in the channel increases. When the gate voltage increases to the point where the barrier is removed and the channel charge is equal to the charge in the source, the transistor drops. In other words, there can't be more charge in the channel than in the source. This effect has been called "source exhaustion" [46, 47]. Its effect on the transistor's IV characteristics is similar to that produced by the "source starvation" effect discussed by Fischetti [14, 19], but it is simply consequence of electrostatics.

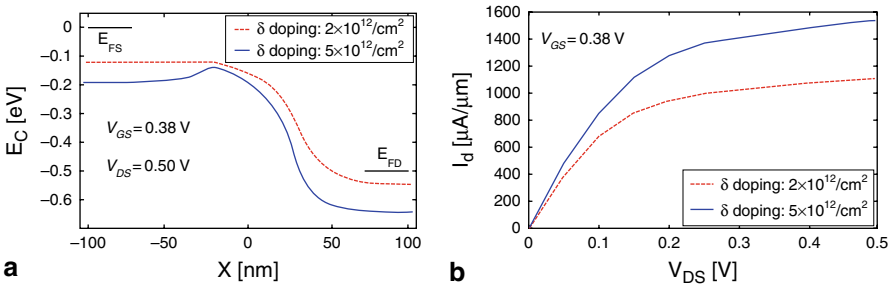

Fig. 3.8 **a** The first subband profile of the HEMT transistor indicates that the potential barrier of the low doping HEMT vanishes at smaller gate bias than the high doping HEMT. **b** The I_d–V_{DS} plot shows low delta-doping HEMT has smaller current than the one with higher delta doping at the same gate bias

Our simulations do not capture the source access and source starvation effects, but they do include the possibility of source exhaustion. Source exhaustion is illustrated in Fig. 3.8a, where the first subband profiles along the channel for delta-doping equal to $2 \times 10^{12}\,\mathrm{cm}^{-2}$ and $5 \times 10^{12}\,\mathrm{cm}^{-2}$ at $V_{GS} = 0.38\,\mathrm{V}$, $V_{DS} = 0.50\,\mathrm{V}$ (intrinsic) are compared for the $L_g = 45\,\mathrm{nm}$ HEMT. For lower delta-doping, the barrier in the channel is smaller and reaches the same level as the "source" region beyond the gate at $V_{GS} = 0.38\,\mathrm{V}$, while for the higher doping the barrier still exists. The electron sheet density at the almost flat potential barrier is $1.7 \times 10^{12}\,\mathrm{cm}^{-2}$, which is very close to the delta doping density, and the transistor begins to lose transconductance as the channel barrier vanishes. In ballistic simulations, this effect in simulation results in non-convergent results if V_{GS} continues to increase (the effect is, however, simply a matter of electrostatics and is observed in drift/diffusion simulations as well.). In comparison, with a higher delta-doping of $5 \times 10^{12}\,\mathrm{cm}^{-2}$, the carrier sheet density at the top of the barrier is $2.3 \times 10^{12}\,\mathrm{cm}^{-2}$ at the same $V_{GS} = 0.38\,\mathrm{V}$, and the larger barrier in the channel ensures the proper function of the transistor at increased gate bias. The doping effect on the HEMT's I_d–V_{DS} characteristics is further shown in Fig. 3.8b, where it is noted that with other conditions remaining the same, higher delta-doping HEMT has larger current than that of the lower doping one. These simulations illustrate the importance of achieving high carrier densities in the source of III-V FETs.

3.3.6 Role of S/D Tunneling

Source-drain tunneling degrades transistor performance by increasing the off-current and sub-threshold swing. It is an important limiting factor in devices with low transport effective mass and short gate lengths. The S/D tunneling effect in III-V HEMTs is explored by examining the energy-resolved current density for a

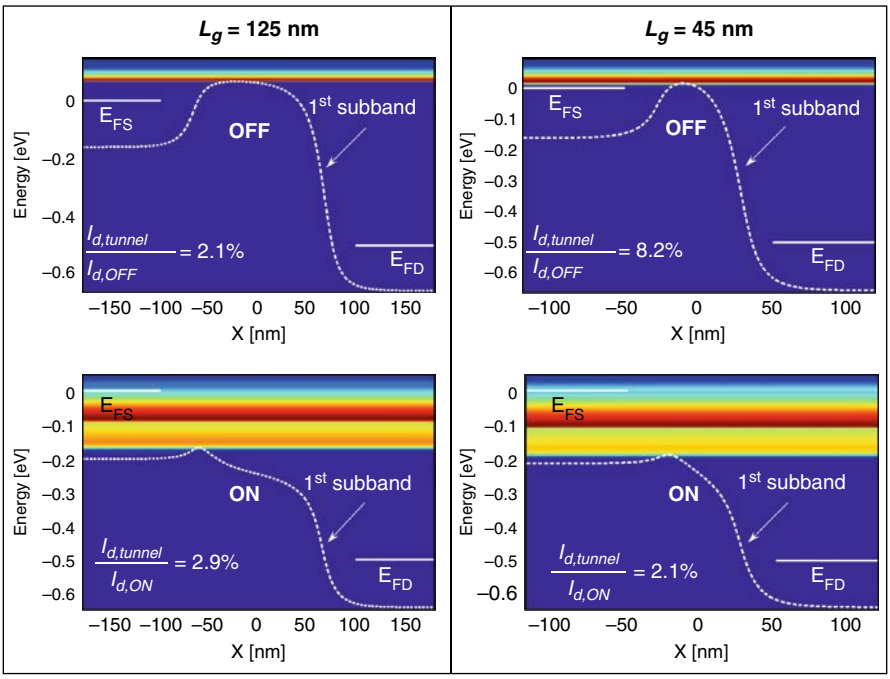

Fig. 3.9 The S/D tunneling is illustrated by the energy-resolved current density in the short and long gate length HEMTs at off and on states. The S/D tunneling effect is larger in shorter HEMTs at off state due to short gate length and larger DIBL

long (L_g = 125 nm) and a short (L_g = 45 nm) gate length HEMT under both off and on states. Figure 3.9 plots the energy-resolved current density for the HEMTs at off (V_{GS} = 0 V, V_{DS} = 0.5 V, intrinsic) and on (V_{GS} = V_{DS} = 0.5 V, intrinsic) states. The first subband along the device is also shown. The S/D tunneling current component is the fraction of the current contributed by carriers with energy below the top of the barrier for each subband. It is observed that under on state conditions, S/D tunneling is an insignificant fraction of the total current for both HEMTs—the current is mainly contributed by carriers with energy larger than the small barrier under high gate bias. Under off state conditions, the S/D tunneling current accounts a larger fraction of the total current than in the on state for L_g = 45 nm device, and the fractional contribution is more in the L_g = 45 nm device than in the L_g = 125 nm device. The tunneling distance in shorter gate length HEMT is further reduced under off state conditions due to the larger drain-induced barrier lowering (DIBL) in the shorter devices, which is indicated by the Fermi level, top of the potential barrier, and the barrier thickness in this energy range in Fig. 3.9. For the III-V HEMTs being examined here, S/D tunneling is not significant; but it can be foreseen that as a target device with superior performance over Si at the 15 nm gate length regime and beyond, the III-V compound semiconductor channel transistors will have a larger S/D tunneling besides the gate leakage at off-state.

3.3.7 Back of the Envelope Calculations

As device dimensions continue to scale well into the nanoscale regime, rigorous treatment of transport using quantum mechanical simulations is necessary to quantitatively predict and benchmark their performance. Simple theoretical calculations, however, often provide a more intuitive understanding of the device operations and estimates of key figures of merit like charge, mobility, and velocity at the top of the barrier. In this section, we analyze the performance of the $L_g = 45\,\text{nm}$ intrinsic ballistic HEMT using analytical calculations, and compare them with NEGF simulation results discussed in the previous sections. We will use a top of the barrier model with a single parabolic band in these equations, and assume temperature $T = 0\,\text{K}$ to keep the mathematics as simple as possible.

The charge at the top of the barrier can be expressed as $Q_i = C_G(V_{GS} - V_T)$, where C_G is the gate capacitance. The gate capacitance consists of the insulator (dielectric) capacitance ($C_{ins} = \varepsilon_{ins}/t_{ins}$) and semiconductor (channel) capacitance ($C_S = -dQ_i/d\psi_s$) in series (see Eq. (3.1)). The semiconductor capacitance has contributions from the density of states (quantum capacitance C_Q) and the modulation of subband energies (Eq. (3.2)). In general, a numerical simulation is required. For our back of the envelope estimate, however, we will replace C_S by its upper limit C_Q which at $T = 0\,\text{K}$, can be expressed as

$$C_Q = \frac{q^2 m^*}{\pi \hbar^2} = \frac{\varepsilon_{ins}}{\Delta t_{ins}} \tag{3.12}$$

Using the material parameters provided in Sect. 3.2.3, Δt_{ins} and C_G are calculated to be 3.2 nm and 1.66 μF/cm^2, reasonably close to the $\Delta t_{ins} = 4.4\,\text{nm}$ $C_G = 1.41\,\mu\text{F/cm}^2$ obtained from the simulations. The result is actually closer than expected. From simulation, we know that two subbands are occupied. But we also know that the subband-modulation term in Eq. (3.2) is approximately 0.5 at high V_{GS} for both subbands from Fig. 3.4b. The two factor-of-two errors cancel, which is why the final result is rather close to the simulations.

With this C_G and an estimated threshold voltage $V_T = 0.057\,\text{V}$ (at $V_{DS} = 0.05\,\text{V}$), the carrier density at the top of the barrier is $N_S = 4.5 \times 10^{12}\,\text{cm}^{-2}$ at $V_{GS} = 0.5\,\text{V}$, compared with simulation results of $N_S = 3.1 \times 10^{12}\,\text{cm}^{-2}$ mainly due to the difference in the capacitance. Under on-current conditions ($V_{DS} = 0.5\,\text{V}$), the density of states at the top of the barrier is only filled by carriers with positive momentum (going from source to drain), thus reducing C_Q by half, and the corresponding gate capacitance decreases to $C_G = 1.1\,\mu\text{F/cm}^2$. The threshold voltage is also reduced to $V_T = -0.008\,\text{V}$ due to effects of 2D electrostatics ($DIBL = 145\,\text{mV/V}$). The charge under on-state conditions ($V_{GS} = V_{DS} = 0.5\,\text{V}$) is $3.5 \times 10^{12}\,\text{cm}^{-2}$, compared to $3.2 \times 10^{12}\,\text{cm}^{-2}$ from the simulations. The conclusion is that estimating the inversion charge in the on state by integrating the equilibrium C–V curve as in Eq. (3.5) will over-estimate the charge because the semiconductor capacitance decreased under high drain bias.

Although there is no scattering in a ballistic conductor, it has finite conductance, and hence a ballistic mobility can be extracted. This ballistic mobility μ_B is related to the ballistic channel resistance as (see Eq. (3.7)):

$$\mu_B = \frac{1}{R_{CH}W}\frac{L_g}{q_0 N_S} \tag{3.13}$$

where R_{CH} is inversely related to the conductance ($G_{CH} = 1/R_{CH}$). The conductance of a ballistic conductor is proportional to the number of transverse propagating modes M, the proportionality constant being the quantum of conductance $2q^2/h$ (with spin). As the transverse modes are separated by $(2\pi/W)$ in the momentum (k) space, the number of modes for a maximum transverse wave vector k_F is given by $M = 2k_F/(2\pi/W) = Wk_F/\pi$ [48]. Here, k_F is the maximum wave vector filled by carriers at $T = 0\,\mathrm{K}$, and is determined by the Fermi energy with respect to the top of the barrier. For a 2D electron gas, the density of states in momentum space is given by $A/4\pi^2$, hence the carrier density is related to k_F as

$$N_S = 2 \times \frac{1}{A}\frac{A}{4\pi^2}\pi k_F^2 = \frac{k_F^2}{2\pi}. \tag{3.14}$$

For $N_S = 4.5 \times 10^{12}\,\mathrm{cm}^{-2}$ (back of the envelope calculation at $V_{DS} = 0.05\,\mathrm{V}$, $V_{GS} = 0.50\,\mathrm{V}$), the number of transverse propagating modes per unit length is $169\,\mu\mathrm{m}^{-1}$, which corresponds to a channel resistance of $R_{CH}{\cdot}W = 76\,\Omega\,\mu\mathrm{m}$. For $N_S = 3.1 \times 10^{12}\,\mathrm{cm}^{-2}$ (simulation results at $V_{DS} = 0.05\,\mathrm{V}$, $V_{GS} = 0.50\,\mathrm{V}$), the channel resistance is $R_{CH}{\cdot}W = 92\,\Omega\,\mu\mathrm{m}$. For comparison, the channel resistance extracted directly from the slope of linear I_d–V_{DS} at the same gate and drain biases at 300 K is $R_{CH}{\cdot}W = 77\,\Omega$-μm, which shows a close matching for analytical calculations. The ballistic mobility is then computed from Eq. (3.13) to be $\mu_B = 822\ \mathrm{cm}^2/\mathrm{V\,s}$, and the corresponding $\mu_{app} = 760\ \mathrm{cm}^2/\mathrm{V\,s}$ (using $\mu_0 = 10{,}000\ \mathrm{cm}^2/\mathrm{V\,s}$, as in Sect. 2.3.4), compared with the simulation results $\mu_B = 1178\ \mathrm{cm}^2/\mathrm{V\,s}$ and $\mu_{app} = 1054\ \mathrm{cm}^2/\mathrm{V\,s}$.

The injection velocity at the top of the barrier (average carrier velocity) is given by $\upsilon_{inj} = 4\upsilon_F/3\pi$ [48], where υ_F is the maximum carrier velocity corresponding to the maximum occupied wave-vector k_F ($\upsilon_F = \hbar k_F/m^*$). Note that at high V_{DS}, N_S at the top of the barrier is dominantly from source-injected carriers, therefore $N_s = k_F^2/4\pi$. Using the equations above, υ_{inj} can be readily obtained for a given carrier density. Under on-current conditions, the υ_{inj} at 0 K corresponding to the back of the envelope calculation of $N_S = 3.5 \times 10^{12}\,\mathrm{cm}^{-2}$ is $\upsilon_{inj} = 6.1 \times 10^7\,\mathrm{cm/s}$, compared to $4.9 \times 10^7\,\mathrm{cm/s}$ obtained with the simulations, which agree fairly well (note again that the abnormally high current, charge density, and injection velocity here are due to our intrinsic discussion without series resistance; in real device all these quantities are substantially lowered by the large series resistance as shown in previous sections).

3.4 Conclusions

In this chapter we have investigated the performance as well as the device physics of recently reported InGaAs HEMTs by using a self-consistent quantum ballistic NEGF model based on effective masses in mode space. Good quantitative agreement between simulation and experimental data indicates that the III-V HEMTs with gate length ~40 nm operate rather close to the ballistic limit. Compared to the simulation results, the smaller drive current reported from experiments at either higher gate bias or longer gate length devices is probably due to phonon scattering degradation. Note that the large series resistance severely limits the III-V HEMTs performance; optimizing the source/drain contacts structure to minimize the series resistance will be critical for future III-V transistors designing, and may amplify the difference between theory and experiment under high gate bias.

The small effective mass in the III-V compound semiconductors has both positive and negative effects on the device performance. The direct positive effect is that the III-V HEMTs ballistic injection velocity is as high as $\sim 3 \times 10^7$ cm/s, as determined from both simulation and experiments. The DOS bottle-neck is a negative effect that degrades the gate capacitance by effectively increasing the upper barrier layer thickness by almost 100%. The resulting electron density at the virtual source is comparably small at on-state, which limits the drive current.

We also found that the apparent channel mobility in III-V HEMT devices is significantly degraded from its very large bulk mobility due to the comparably very small "ballistic mobility", which becomes important as the device channel length scales down to the ballistic limit regime. The δ-doping effects on the source designing were also investigated. Lower δ-doping will improve *S* and *DIBL*, but the current is smaller due to the smaller energy range between the source Fermi level and the top of the barrier. Besides, the top of the barrier tends to disappear at relatively smaller intrinsic gate bias, after which the device will become dysfunctional. Next the S/D tunneling in III-V HEMTs was found insignificant at gate length of 40 nm; it is however, foreseen to become severe when the gate length approaches 15 nm and beyond. Finally, the intrinsic simulation results can be well explained by theoretical calculations with simple device physics based on a top-of-the-barrier model, which helps the understanding of the device operational mechanism as a reference to the 2D simulation.

The next challenge to address is the lowering of the series resistance, because Fig. 3.3 shows that if the series resistance can be decreased to values typical of silicon MOSFETs, then III-V FETs would offer high drive current at power supply of one-half of silicon.

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