Measurement of Channel Temperature in GaN High-Electron Mobility Transistors

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***Abstract*—In this paper, a simple and reliable method to estimate the channel temperature of GaN high-electron mobility transistors (HEMTs) is proposed. The technique is based on electrical measurements of performance-related figures of merit ($I_{\mathrm{D\,max}}$ and R_{ON}) with a synchronized pulsed I–V setup. As our technique involves only electrical measurement, no special design in device geometry is required, and packaged devices can be measured. We apply this technique to different device structures and validate its sensitivity and robustness.**

***Index Terms*—Channel temperature, GaN, high-electron mobility transistors (HEMTs), junction temperature, measurement.**

I. Introduction

AN ACCURATE estimation of the channel temperature of GaN high-electron mobility transistors (HEMTs) is essential for extrapolation of time constants associated with temperature-activated failure mechanisms as well as for understanding the physics behind device degradation. Channel-temperature estimation is particularly complicated in high-power-density devices such as GaN HEMTs because self-heating and channel-to-base-plate temperature gradients are large.

A few methods have been proposed for temperature estimation in GaN HEMTs [1]–[3]. Theoretical modeling is widely used to estimate the channel temperature of a device [1]. However, modeled data can differ from reality due to inaccuracies in material parameters and their dependence on temperature and stress, and heat source distributions. Thus, it is essential to verify the model with physical measurements on an actual device under operation.

Optical temperature-measurement techniques such as infrared thermal imaging and micro Raman spectroscopy [2] are often used but they have several limitations. First, they usually impose special requirements on device geometry, such as large gate-to-drain gap and limited field plate and air bridge configuration for a direct access to the device from the top, and it is difficult to measure a fully packaged device [4]. In addition, the experimental setup is not commonly available in an electrical characterization environment. Finally, optical techniques measure vertically averaged temperature of the GaN layer [5]. As a result, the temperature right at the channel is difficult to measure.

Several electrical measurements have been proposed to estimate channel temperature. The temperature dependence of the gate Schottky diode characteristics has been useful for temperature measurements in GaAs devices [4]. However, it is difficult to apply this technique to GaN devices due to degradation of the Schottky barrier with any sizeable gate current [6]. Using dc characteristics to measure channel temperature has also been proposed in GaN HEMTs [7], [8]. However, we have found that a dc measurement technique becomes problematic at high voltage because it can be cumbersome to remove the change in I_D induced by current collapse in GaN HEMTs. Additionally, finite output conductance due to channel length modulation makes the measurements hard to analyze.

An optimal measurement technique for estimating channel temperature should pose the following characteristics: 1) simple; 2) with no special requirement on device layout and geometry; 3) reproducible; 4) sensitive to circuit design variables such as finger width, gate-to-gate pitch, and substrate thickness; 5) robust to device degradation (e.g., current collapse); and 6) able to measure packaged devices. In this paper, we present a simple yet powerful method for estimation of channel temperature in GaN HEMTs that meets all these requirements.

II. Proposed Technique

Electrical transport properties of semiconductors such as mobility and saturation velocity of electrons are strong functions of temperature. As they are integral parts of critical device parameters, these figures of merit are also affected by channel temperature. This connection provides a unique opportunity to estimate channel temperature through $I_{\mathrm{D\,max}}$ and R_{ON}. The channel temperature of a device can be changed by either external heating or self-heating. In our technique, we calibrate temperature dependence of device parameters through external heating, and then, we measure device temperature under operation by measuring the same electrical-device parameters pulsing from the operating conditions.

The key enabler of this technique is a pulsed I–V system that is capable of pulsing drain and gate bias simultaneously in submicrosecond time scale. This allows sampling electrical

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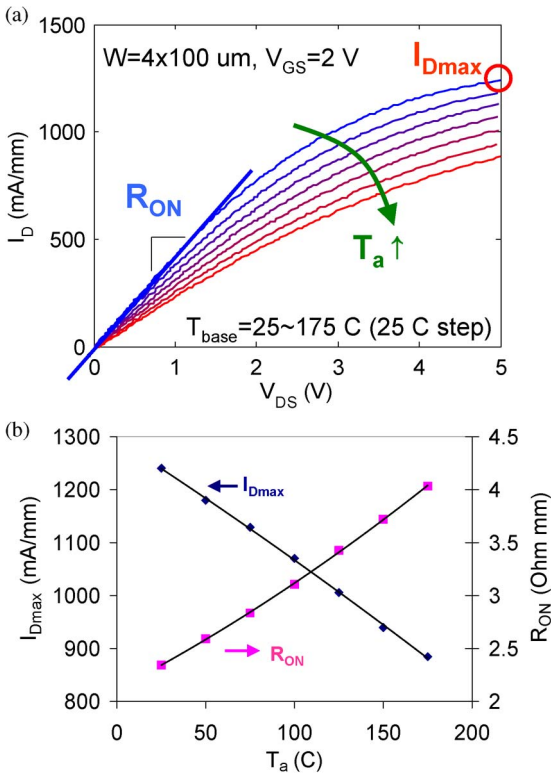

Fig. 1. (a) Pulsed I–V characteristics ($V_{\rm GS} = 2$ V) from zero power quiescent bias point ($V_{\rm DS} = V_{\rm GS} = 0$) at different base-plate temperature (25 °C–175 °C). The definitions of $I_{\rm D\,max}$ and $R_{\rm ON}$ are shown in the figure. As temperature increases, $I_{\rm D\,max}$ decreases and $R_{\rm ON}$ increases. (b) Extracted pulsed $I_{\rm D\,max}$ and $R_{\rm ON}$ as a function of base-plate temperature T_a.

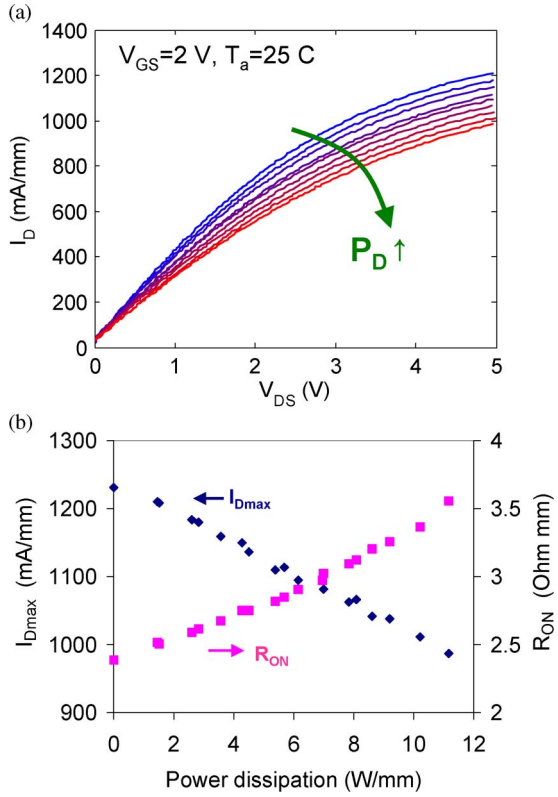

Fig. 2. (a) Pulsed I–V characteristics ($V_{\rm GS} = 2$ V) from various quiescent bias points ($V_{\rm GS} = 2$ V, $V_{\rm DS} = 2$–10 V) with nonzero power dissipation ($P_D = 1.5$–11.2 W/mm). The same device is used as in Fig. 1. The base-plate temperature is 25 °C. As quiescent power dissipation increases, $I_{\rm D\,max}$ decreases and $R_{\rm ON}$ increases. (b) Extracted pulsed $I_{\rm D\,max}$ and $R_{\rm ON}$ from different bias points with different power dissipation. Additional data points are used from those shown in (a).

parameters from different quiescent conditions. By using submicrosecond pulses for $I_{\rm D\,max}$ and $R_{\rm ON}$ measurement, the channel temperature remains that of the quiescent condition. Our technique consists of two steps: a calibration step and a measurement step. In the calibration step, we measure $I_{\rm D\,max}$ and $R_{\rm ON}$ as a function of base-plate temperature. These electrical parameters are measured by pulsing from $V_{\rm GS} = 0$ V and $V_{\rm DS} = 0$ V. At this condition, there is no dissipated power, and the channel temperature is the same as the base-plate temperature. From this measurement, we create a lookup table ($I_{\rm D\,max}$ and $R_{\rm ON}$ as a function of T_j). In the measurements step, we measure $I_{\rm D\,max}$ and $R_{\rm ON}$ by pulsing from different quiescent conditions. At each quiescent condition, the device dissipates a different amount of power ($V_{\rm DSQ} \times I_{\rm DQ}$). As a result, we can measure $I_{\rm D\,max}$ and $R_{\rm ON}$ at different channel temperatures that are set by the quiescent biases. With the lookup table, these electrical measurements can be translated into the channel temperature.

The devices used in this paper are 0.25-μm GaN HEMTs with a field plate [9], [10]. Unless otherwise stated, the devices are fabricated on a SiC substrate. For pulsed I–V measurements, an Accent Optical Technologies Dynamic I–V Analyzer system was used. The pulsewidth and duty cycle for $I_{\rm D\,max}$ and $R_{\rm ON}$ measurements were 0.2 μs and 0.02%, respectively. Fig. 1(a) shows pulsed I–V characteristics of a 4 × 100-μm GaN HEMT on a 3-in wafer at different base-plate temperatures. The quiescent bias point was $V_{\rm DS} = V_{\rm GS} = 0$ (zero power dissipation). The wafer is placed on the prober chuck of which the temperature is set to 25 °C to 175 °C. In this figure, we define $I_{\rm D\,max}$ as I_D at $V_{\rm DS} = 5$ V and $V_{\rm GS} = 2$ V and $R_{\rm ON}$ as the drain-to-source resistance in the linear region at $V_{\rm GS} = 2$ V. It is noted that these parameters are pulsed values that are different from dc values. One can see that $I_{\rm D\,max}$ decreases and $R_{\rm ON}$ increases as the temperature increases. From this calibration step, two lookup tables to convert $I_{\rm D\,max}$ and $R_{\rm ON}$ measurements to the temperature are created [Fig. 1(b)].

In the temperature-measurement step, we used the same pulse condition but used various bias conditions (e.g., $V_{\rm DS} = 8$ V, $V_{\rm GS} = 2$ V) that dissipate different amounts of power. Fig. 2 shows I–V characteristics pulsed from various bias points at 25 °C with different levels of power dissipation for the same device in Fig. 1. By comparing the change in electrical characteristics due to self-heating (Fig. 2) to that due to external heating (Fig. 1), we can estimate the channel temperature when a device is in operation. In order to prevent device degradation and introduction of current collapse, in all our measurements, $V_{\rm DS}$ was limited to 10 V—a value that has been separately tested to be adequately benign in these devices [11]. Typical values for $V_{\rm GS}$ were from -2 to 2 V. Fig. 2(b) shows the measured $I_{\rm D\,max}$ and $R_{\rm ON}$. Different quiescent bias points with a wide range of $V_{\rm DS}$ and $V_{\rm GS}$ produced different power dissipation in the device. This was calculated as $V_{\rm DSQ} \times I_{\rm DQ}$. As expected, $I_{\rm D\,max}$ and $R_{\rm ON}$ are only functions of power dissipation and do not depend on the specific bias conditions.

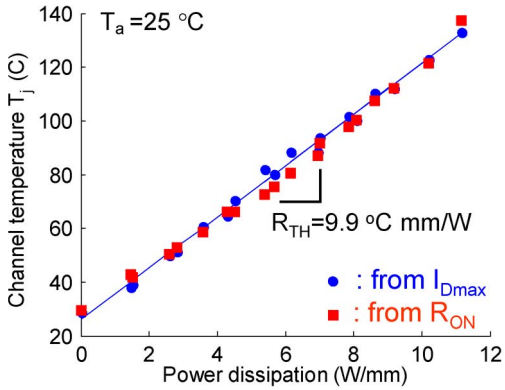

Fig. 3. Estimated channel temperature from data in Figs. 1 and 2 as a function of power dissipation. (●) Data obtained through $I_{\mathrm{D\,max}}$ measurement. (■) Data obtained through R_{ON} measurement.

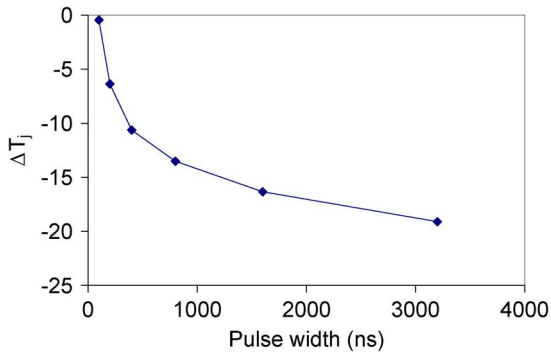

Fig. 4. Simulation of the decrease in channel temperature during a measurement of $I_{\mathrm{D\,max}}$ as a function of the pulsewidth. The quiescent bias condition dissipates 11 W/mm.

In order to translate $I_{\mathrm{D\,max}}$ and R_{ON} changes into channel temperature, the lookup tables that were created in the calibration step [Fig. 1(b)] are used. The final result is shown in Fig. 3 which gives a relation between the channel temperature and power dissipation. The channel temperature extracted from $I_{\mathrm{D\,max}}$ measurement agrees well with that extracted from R_{ON} measurement, showing the consistency of this technique. Although the thermal conductivity is, in general, temperature dependent, an almost linear relationship between temperature and power dissipation up to $T_j = 140\ ^{\circ}\mathrm{C}$ was observed presumably due to a weak dependence [12]. The thermal resistance R_{TH} of the device can be calculated from the slope of the line in Fig. 3. For the device in that figure, the value is $9.9\ ^{\circ}\mathrm{C}\cdot\mathrm{mm/W}$.

A few channel-temperature evaluation techniques using pulsed I–V measurements have already been presented in the literature [13], [14]. These techniques use either gate pulse or drain pulse during the measurement, and the main reason for the pulsed measurement is to prevent self-heating. For this, the quiescent bias condition is a completely OFF-state in which no power is dissipated. The pulsed I–V characteristics are compared to dc characteristics where self-heating effects are inherent [14]. Because the temperature is estimated by rather complicated fittings to model, it is relatively easy to introduce errors in the result.

In our technique, we establish different channel temperatures at different quiescent bias conditions due to self-heating right before $I_{\mathrm{D\,max}}$ and R_{ON} are measured in a pulsed manner. As discussed earlier, it is assumed that the channel temperature does not change significantly during the pulse. For this, the duty cycle needs to be small enough to maintain the channel temperature due to self-heating. In addition, by using submicrosecond pulses, when $I_{\mathrm{D\,max}}$ and R_{ON} are sampled, the channel temperature remains almost unchanged through the measurement. For the measurement condition of $I_{\mathrm{D\,max}}$, the power dissipation is about 6 W/mm, whereas it is almost zero for R_{ON}. As a result, the amount and the sign of change in temperature during the pulse, if any, should be different for $I_{\mathrm{D\,max}}$ and R_{ON}, depending on the amount of power dissipation for the bias condition. In fact, $I_{\mathrm{D\,max}}$ and R_{ON} measurements give a consistent result (Fig. 3). In addition, we find that thermal-resistance values separately extracted from $I_{\mathrm{D\,max}}$ and R_{ON} measurements in 35 devices differ from each other by 5.7% of its value on average. These results show that the change in temperature during the pulse is minimal.

This is shown more clearly in Fig. 4, where the decrease in the channel temperature that takes place during the measurement of $I_{\mathrm{D\,max}}$ is evaluated as a function of the pulsewidth. These results are obtained from transient temperature simulations from ANSYS thermal analysis system (TAS). It can be seen that for the pulsewidth of 0.2 μs used to measure $I_{\mathrm{D\,max}}$ in this paper, the channel temperature is no less than 6 °C below the temperature set by self-heating due to the quiescent bias. This small error can be minimized by using a shorter pulse ($< 0.1\ \mu$s). However, as shown in Fig. 4, it can be problematic when longer pulsewidth is used, and thus, the channel temperature changes significantly during the pulse [15]. In that case, another calibration step may be needed (e.g., from transient thermal simulation).

Our techniques assume that all the changes in $I_{\mathrm{D\,max}}$ and R_{ON} that occur during the pulse measurements under self-heating bias conditions result from channel-temperature change, not from other effects such as trapping. This assumption will be discussed in the following section.

III. Discussion

A. Reproducibility

In order to test the reproducibility of the technique, we have measured a single device for four times independently. Independent calibration and temperature measurements were performed. Those measurements were repeatable with a difference in R_{TH} smaller than 0.2%. Separately, we measured nine nominally identical devices on the same wafer. The standard deviation of R_{TH} for these devices was found to be less than 5% of its mean value for data obtained from both $I_{\mathrm{D\,max}}$ and R_{ON} measurements.

B. Sensitivity: Device Geometry

In order to confirm the sensitivity of the technique to different device designs, first, we have measured devices with different gate-finger widths. These devices have a single gate finger. As shown in Fig. 5, the thermal resistance per unit width increases with gate width. This is because, in narrower devices,

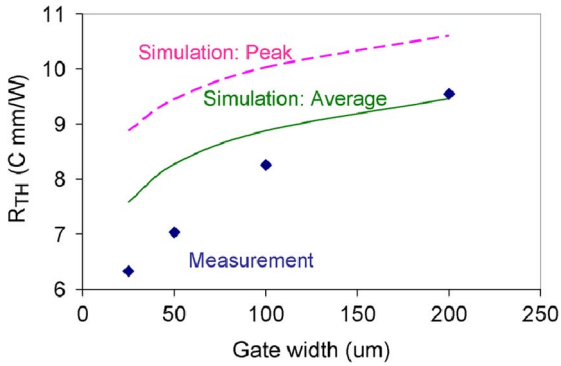

Fig. 5. Measured and simulated thermal resistance of GaN HEMTs with different gate widths. Devices have one gate finger. Dashed line represents R_{TH} calculated from peak channel temperature while solid line represents R_{TH} calculated from averaged channel temperature under the gate region.

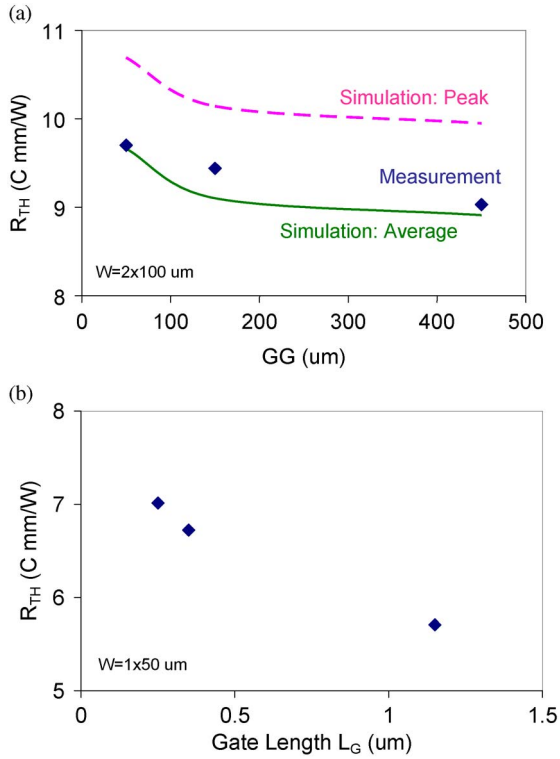

Fig. 6. (a) Measured and simulated thermal resistance of 2×100-μm GaN HEMTs with different gate-to-gate pitch. Dashed line represents R_{TH} calculated from peak channel temperature while solid line represents R_{TH} calculated from averaged channel temperature under the gate region. (b) Measured thermal resistance of 1×50-μm GaN HEMTs with different gate length.

a significant amount of heat dissipation takes place along the third dimension of the device.

We have also applied our proposed technique to various devices with different geometries (gate width, gate length, gate-to-gate pitch) on different substrates (SiC and Si) and have confirmed the sensitivity of our technique to these design parameters. Some of the results are shown in Fig. 6 together with thermal simulations. As shown in Fig. 6(a), R_{TH} of two-finger devices decreases as the gate-to-gate pitch increases. In addition, in Fig. 6(b), longer gate-length devices show smaller R_{TH}.

TABLE I
MEASURED AND SIMULATED THERMAL RESISTANCE OF 4×100 GaN HEMTs ON SiC. IN THE SIMULATIONS, AN IDEAL THERMAL CONTACT AT THE BOTTOM OF THE SUBSTRATE WAS ASSUMED

	R_{TH} ($^{\circ}$C mm/W)
Chip on chuck	18.3
Chip on brass plate with AuTn solder	10.7
Chip on PGA with AuTn solder	10.3
Chip on RF fixture with AuTn solder	10.5
Whole wafer on chuck	8.63
Simulation	11.5 (peak) 9.51 (channel average)

C. Sensitivity: Thermal Contact

In order to study the effects of thermal contact at the back of the wafer, we have measured the thermal resistance of devices with different thermal contact to the base plate. The devices have 4×100-μm gate fingers with 50-μm gate-to-gate spacing. These devices are either in a chip size of 10 mm^2 or in a whole 3-in wafer. Table 1 summarizes the results.

First, with the chip directly on the chuck, it can be seen that it is hard to make a good thermal contact. The thermal resistance (18.3 °C · mm/W) was the highest. However, if the chip is mounted on a good thermal conductor such as brass plate, pin grid array (PGA), or RF fixtures using AuTn solder, the thermal resistance is almost as good as the thermal resistance of a device on a 3-in wafer (8.63 °C · mm/W) directly on the chuck. In the latter case, the measured thermal resistance should be close to the intrinsic thermal resistance of the device because the entire area of the wafer is in direct contact with the chuck. All these results were close to thermal simulation (peak temperature of 11.5 °C · mm/W and channel average of 9.51 °C · mm/W).

In addition, we have measured R_{TH} of a device on a GaN on Si chip mounted on a PGA, and we obtained 23.1 °C · mm/W. The devices have 2×130-μm gate fingers with 32-μm gate-to-gate spacing. Simulated R_{TH} for the GaN on Si device was 22.5 °C · mm/W, which was close to the measured value.

D. Immunity to Current Collapse and Degradation

As our technique is based on the change in pulsed I–V characteristics under self-heating, any effects which cause changes in pulsed I–V characteristics may contaminate the temperature measurement. In GaN HEMTs, trapping behavior such as current collapse becomes significant when the device is biased at high voltage [16]. Moreover, for GaN HEMTs, degradation usually involves an increase in current collapse [11], [17]. In our technique, the current collapse due to the pulse measurement is not a problem because the lookup table [Fig. 1(b)] is constructed under pulsed condition, i.e., the current collapse is built into the lookup table. However, the current collapse due to an application of high voltage can still affect the measurement. In order to study the impact of the current

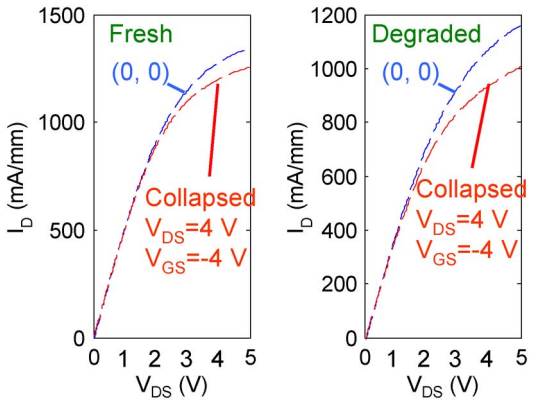

Fig. 7. Measurement of current collapse for a fresh device and a degraded device at room temperature. The lines represent the pulsed I_D–$V_{\rm DS}$ characteristics of 4×100-μm devices for $V_{\rm GS} = 2$ V after a quiescent bias point indicated in the figure. The base-plate temperature is 25 °C. $I_{\rm D\,max}$ compression due to current collapse is 6.7% and 11.7% for the fresh and degraded devices, respectively.

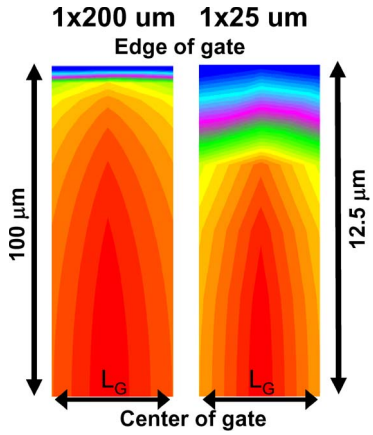

Fig. 8. Temperature distribution along the half gate finger for 200- and 25-μm devices. The color is normalized to the peak temperature at the center of the gate finger.

collapse on our technique, we compared devices with different degree of current collapse: a fresh device with small current collapse and a degraded device with high-current collapse. Device degradation was produced by stressing at $V_{\rm DS} = 40$ V and $I_D = 250$ mA/mm for 44 h at 112 °C. These chips were mounted on PGAs. As these two devices sit side by side on the same chip, they should have similar thermal resistance.

Fig. 7 shows the current-collapse measurements of both devices. Usually, current collapse is measured at room temperature in a pulsed I–V setup by comparing I–V characteristics that are pulsed from different bias condition: $V_{\rm DS} = V_{\rm GS} = 0$ (uncollapsed I–V) and OFF-state with high $V_{\rm DG}$ (collapsed I–V). As the maximum $V_{\rm DG}$ in our measurement was 8 V ($V_{\rm GS} = 2, V_{\rm DS} = 10$ V), $V_{\rm DS} = 4$ V and $V_{\rm GS} = -4$ V was used as the bias condition for the collapsed I–V measurement. The pulsing condition was the same as before.

As can be seen, the degraded device shows almost twice as much current collapse than the fresh device. In spite of this large difference in current collapse, the thermal resistance obtained for these two devices are 15.2 °C · mm/W and 15.4 °C · mm/W, respectively. This is not surprising, since separate calibrations were performed on each individual device, and the technique remains applicable. Also, the amount of change in $I_{\rm D\,max}$ due to current collapse at room temperature resulting from the maximum voltage that we apply in our technique is much less than that due to self-heating. In addition, we have found that the current-collapse effect almost disappears at around 125 °C, which is lower than the typical channel temperature under high-power dissipation. The small impact of current collapse on our thermal-resistance measurement is further justified by the fact that current collapse is known to be minimal when pulsing $V_{\rm DS}$ in the ON-state [18], which is the case in our measurement.

Our proposed technique does not provide spatial information about temperature on the plane of the device. Instead, it averages the temperature along the channel, which is normally nonuniform in a transistor [2]. However, it has good vertical resolution, since only electrons in the channel participate in $I_{\rm D\,max}$ and $R_{\rm ON}$, and any type of device—even a device in a package—can be measured with minimal complications. These aspects represent a great advantage over all optical techniques.

IV. Comparison to Simulation

We have simulated the thermal resistance of these devices using ANSYS TAS. The 3-D simulation did not take electrothermal coupling into account, and uniform power dissipation across a gate finger was assumed. Although the simulation result was in good agreement with the measurement as shown earlier, the measured thermal resistance was slightly lower than the simulated thermal resistance that is calculated from the peak temperature of the device at the channel. However, the experimental data were close to the simulated value that is calculated from the average temperature in the channel region (60-nm region in depth just under the 0.25-μm gate-finger area). This is consistent with the fact that our measurement technique averages the temperature in the channel area.

However, it was found that the simulated result sometimes show discrepancy with the measurement data. For example, the thermal resistance per unit width decreases with width faster in our measurements than in thermal simulations (Fig. 5). In order to investigate this discrepancy, we have studied the simulated temperature profile along the gate finger.

Fig. 8 shows the temperature distribution of a 1×200- and a 1×25-μm device. In the figure, half of the gate finger is shown. As mentioned before, we assume that heat dissipation is uniform across a gate finger. As shown, the relative portion of the device where the temperature is lower than at the center is bigger in the narrow device. As a result, in a narrower device, electric current and power dissipation are expected to be higher in the periphery of the device. For the narrower the device, the more pronounced this nonuniformity effect is expected, as shown in Fig. 8. As a result, less power per unit length is dissipated at the center of the device, resulting in an overall smaller thermal resistance. This is why the thermal simulations that do not account for electrothermal coupling effect are bound to overestimate the thermal resistance in narrow devices. This result shows the limitation of thermal simulations and the importance of a direct measurement of the thermal resistance.

V. Conclusion

We have demonstrated a new method to estimate the channel temperature of GaN HEMTs. This technique can be applied to any field-effect transistor. We have shown that this method is simple yet robust and powerful and links the components of thermal resistance (temperature and power) to performance-relevant electrical parameters such as $I_{\mathrm{D\,max}}$ and R_{ON}.

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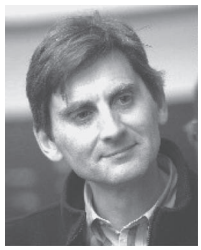

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