Modeling Frequency Response of 65 nm CMOS RF Power Devices

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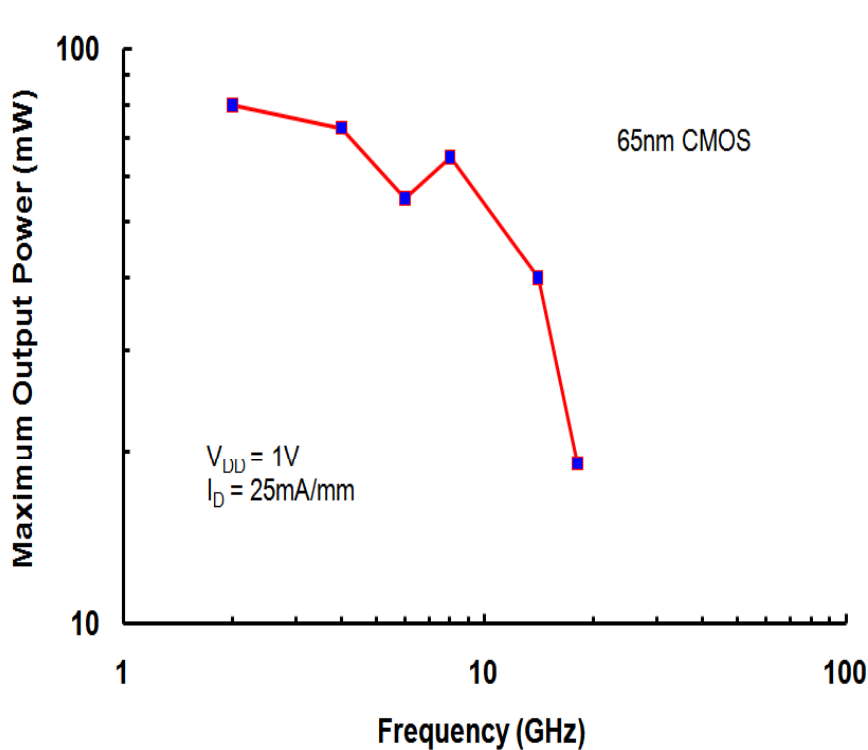
Theme /Task: 1661. 002

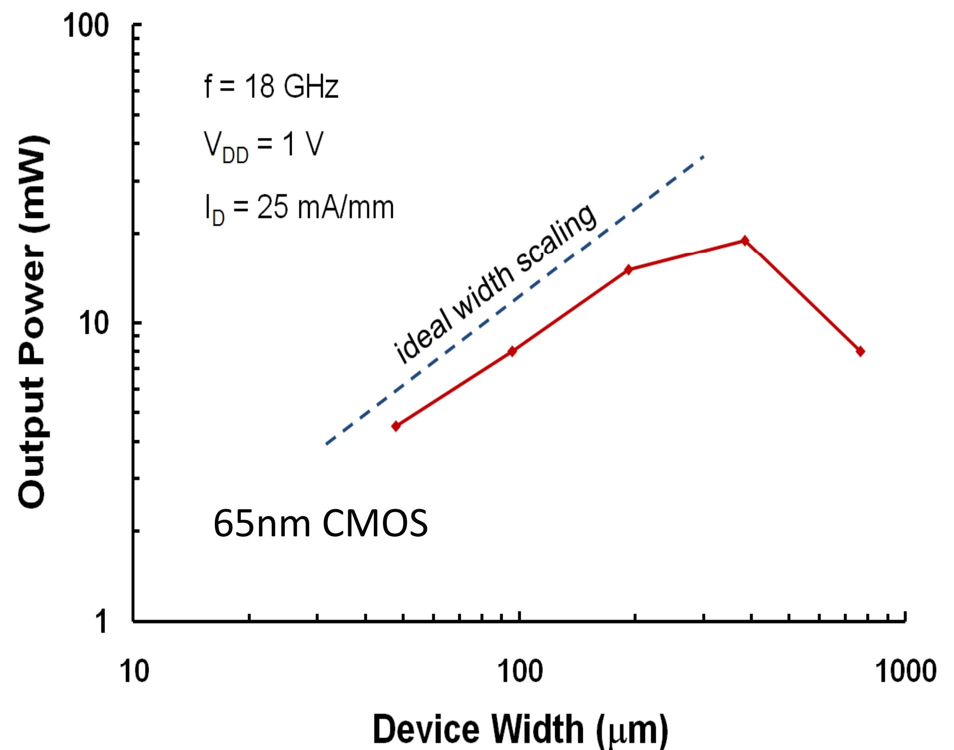
Outline

- Motivation
- Measured Data on 65 nm CMOS
  - f_T, f_{max} as a function of device width
- Small-signal Equivalent Circuit Extraction
- Analytical Model for f_T and f_{max}
- Conclusions

Motivation

- Great interest in using CMOS for mm-wave power applications
- However, P_{out} < 20 mW at 18 GHz [1]
- Output power does not scale with width in wide devices





1. J. Scholvin, IEDM 2006

Motivation

- Why doesn't output power scale in wide devices?
- High frequency power performance correlates with f_{max}

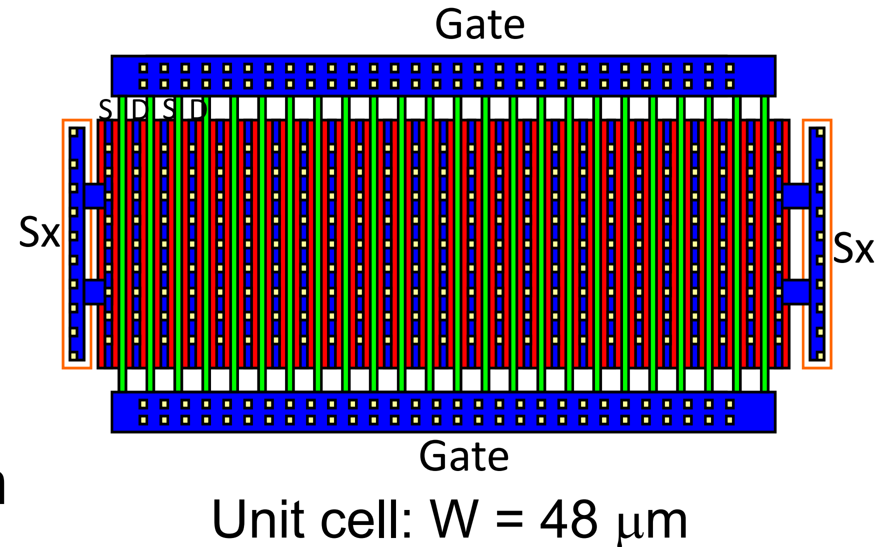
Key Questions:

✓ How does f_{max} scale in wide devices?

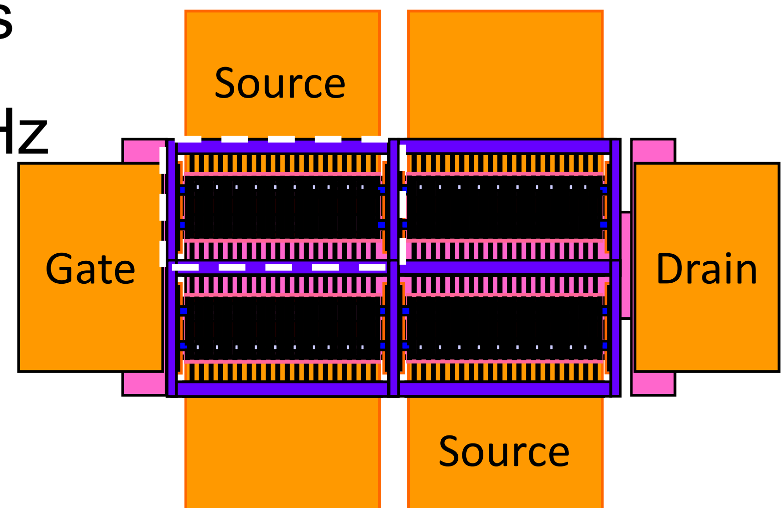
✓ Can we predict f_T, f_{max} for a given device layout?

Technology and Layout Details

- 65 nm CMOS from IBM
- Gate Length = 50 nm
- Gate Width = 96 μm to 1536 μm
- Unit Cell: 24 fingers of 2 μm width
- W ↑ by parallelizing multiple unit cells
- S-parameters from 0.5 GHz to 40 GHz
- Open and short de-embedding

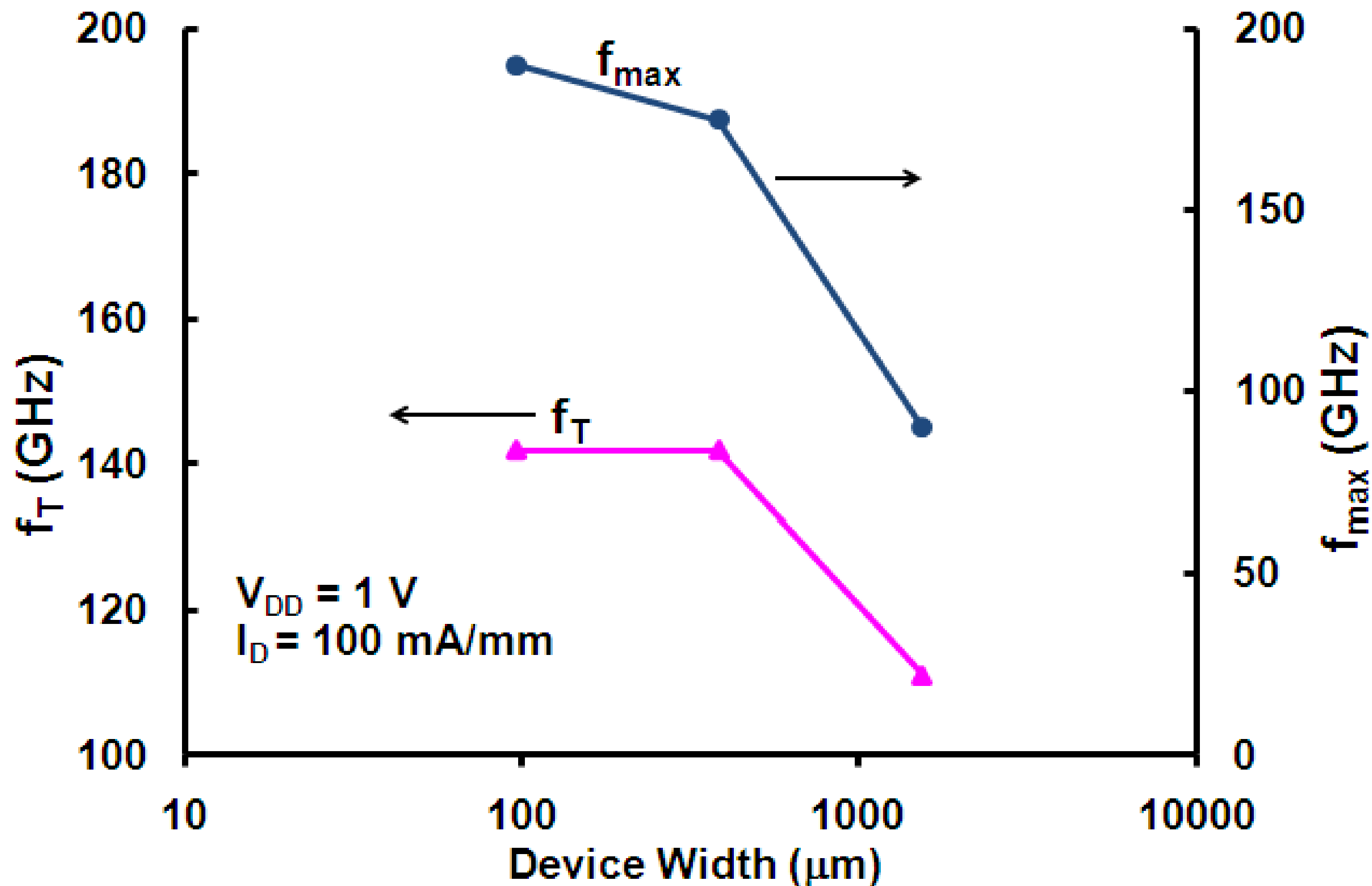


Unit cell: W = 48 μm



4 Unit cells: W = 192 μm

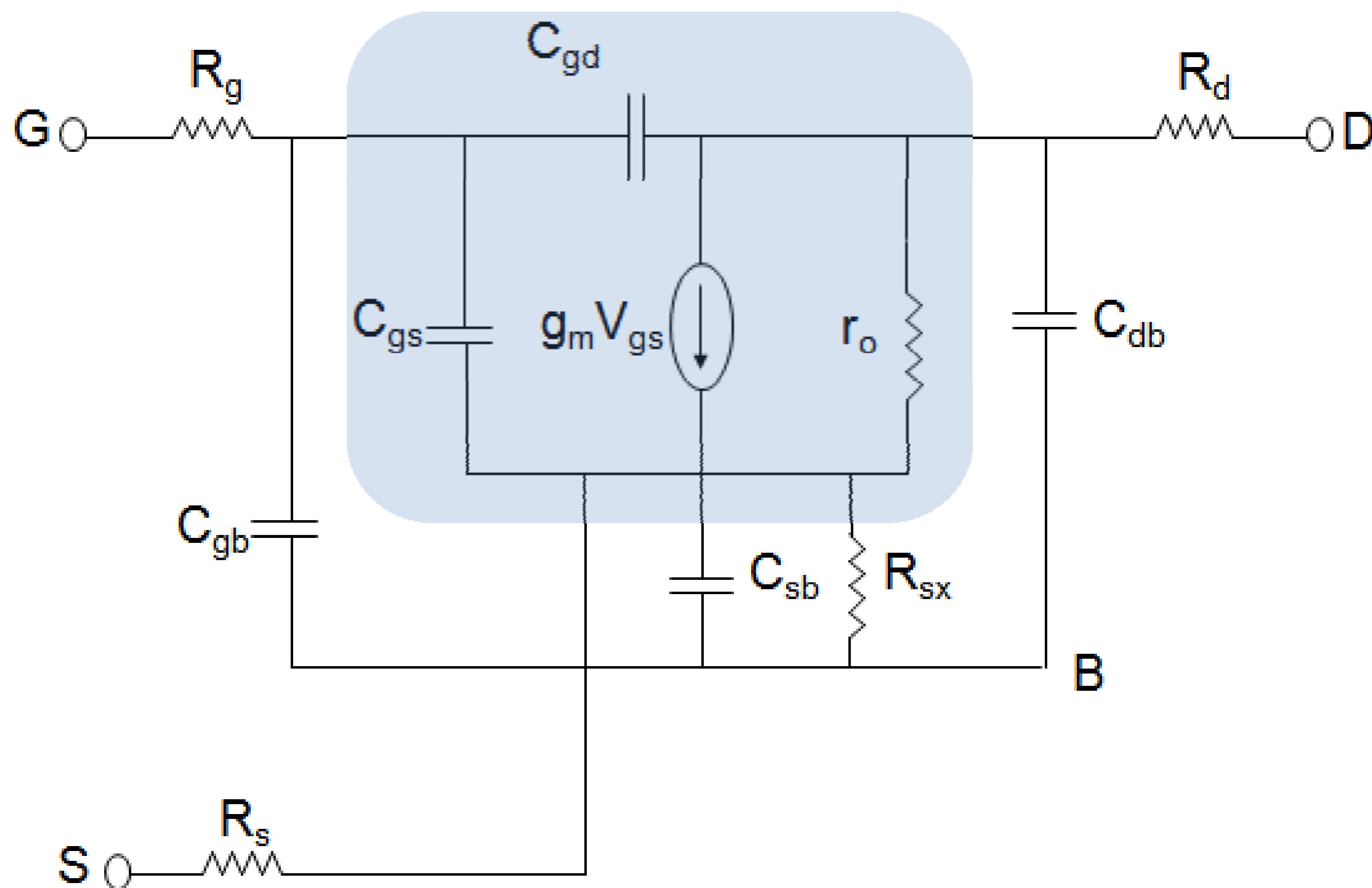
Measured Data - f_T, f_{max}



$f_T \downarrow$ and $f_{max} \downarrow$ as $W \uparrow$

Small-signal Equivalent Circuit

To understand f_T, f_{max} width scaling: construct small-signal equivalent circuit



Small-signal Parameter Extraction

1. Measure S-parameters @ $V_{GS}=V_{DS}=0$ V

   Convert to Z-parameters

$$R_G = \mathrm{Re}(Z_{11} - Z_{12})$$

$$R_S = \mathrm{Re}(Z_{12})$$

$$R_D = \mathrm{Re}(Z_{22} - Z_{12})$$

2. Measure S-parameters @ $V_{DS}=1$ V, $I_D=100$ mA/mm

   Convert to Z-parameters

   Subtract R_G, R_S, R_D

   → Intrinsic Z-parameters

3. Convert to Y-parameters

$$g_m = \mathrm{Re}(Y_{21})$$

$$r_o = \frac{1}{\mathrm{Re}(Y_{22})}$$

$$R_{sx} = \frac{\mathrm{Re}(Y_{22} + Y_{12})}{(\mathrm{Im}(Y_{22} + Y_{12}))^2}$$

$$C_{gs} = \frac{\mathrm{Im}(Y_{11} + Y_{12})}{\omega}$$

$$C_{gd} = -\frac{\mathrm{Im}(Y_{12})}{\omega}$$

$$C_{db} = C_{sb} = \frac{\mathrm{Im}(Y_{22} + Y_{12})}{\omega}$$

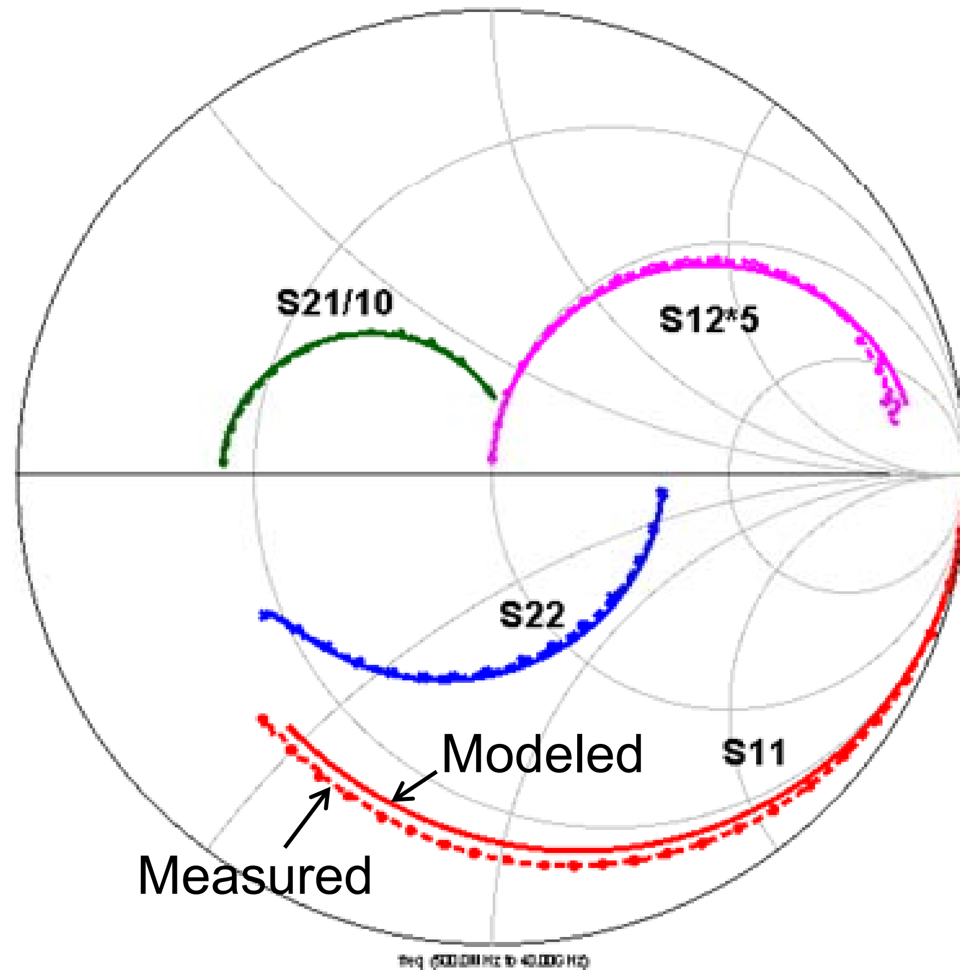
   C_{gb} by fitting in ADS

Ref: D. Lovelace, Microwave Symposium, 1994

Measured vs Modeled s-parameters

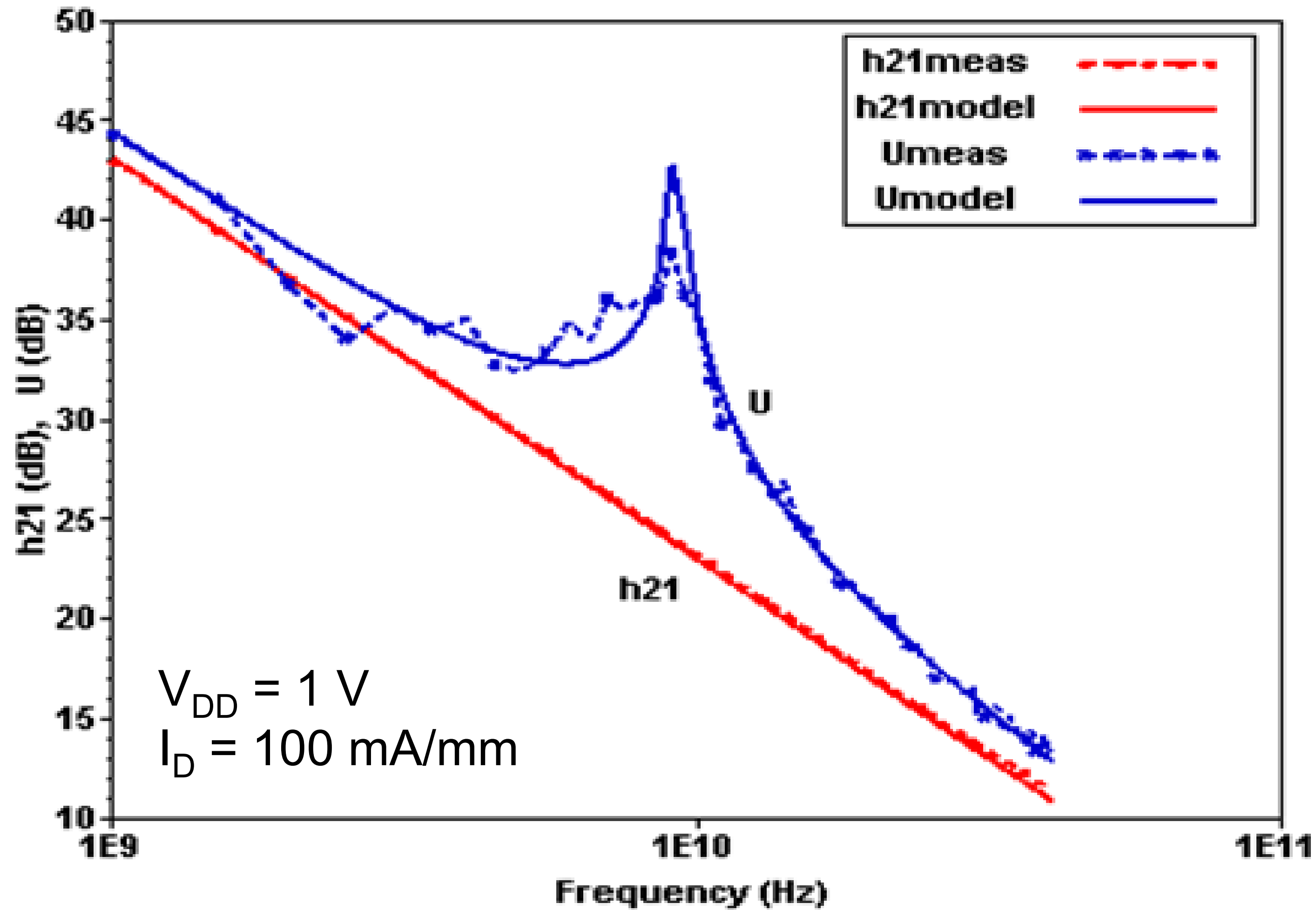
$W = 96\ \mu m$

$V_{DD} = 1\ V$
$I_D = 100\ mA/mm$



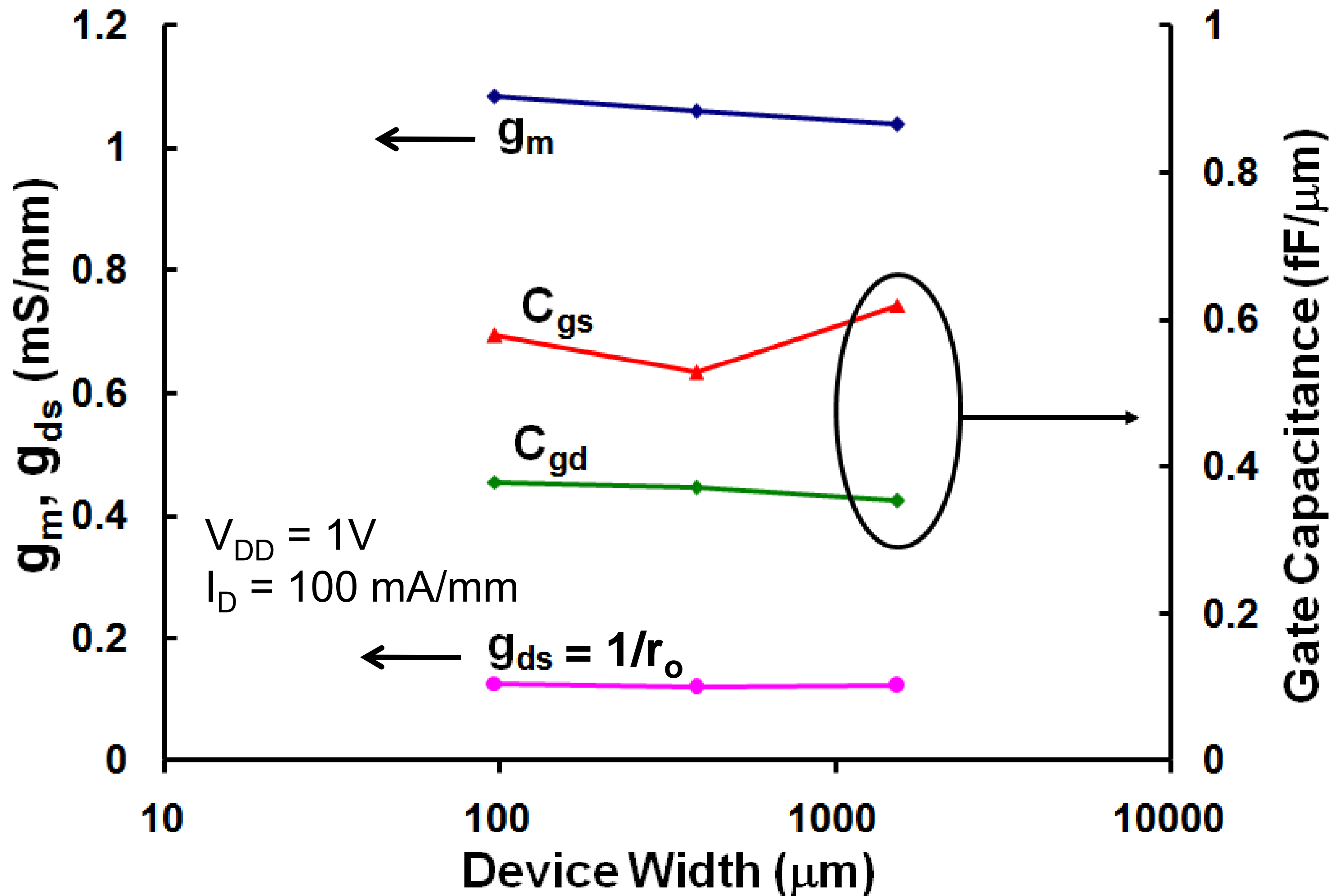
Model fits measured s-parameters well

Measured vs Modeled f_T, f_{max}



Model fits measured h_{21} and U at all frequencies

Width Dependence of Intrinsic Parameters



Intrinsic parameters scale ideally with W

Width Dependence of Parasitic Resistances

Parasitic R (Ω-µm)

800
700
600
500
400
300
200
100
0

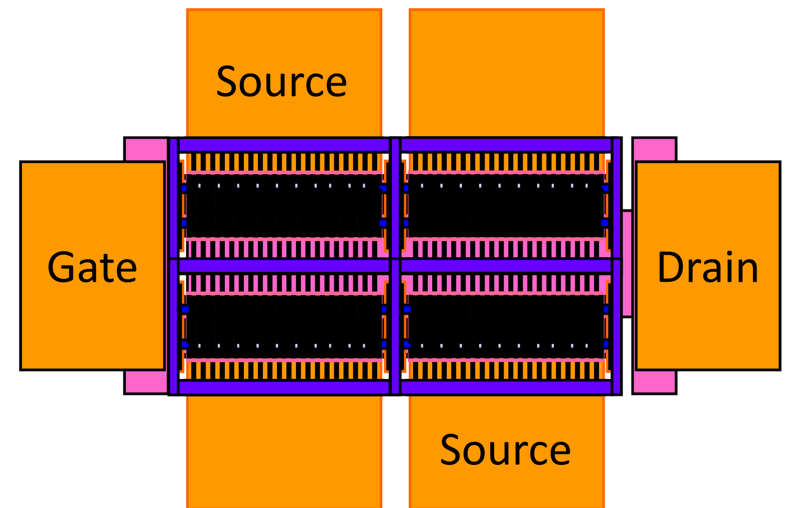
V_{DD} = 1V
I_D = 100 mA/mm

R_D
R_G
R_S

2 cells
8 cells
32 cells

10
100
1000
10000

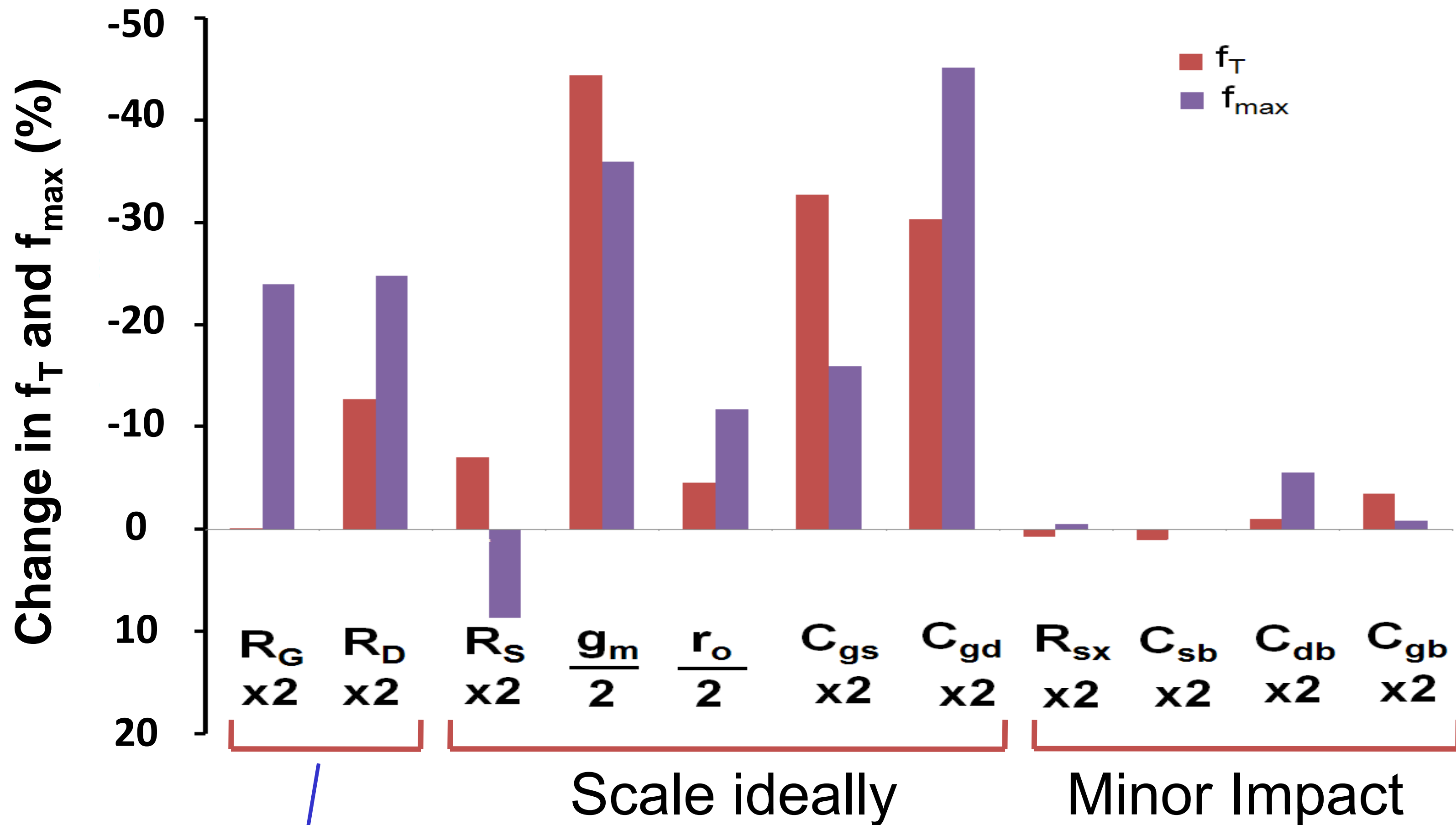
Device Width (µm)



R_S constant, R_G ↑ and R_D ↑ as W ↑

f_T, f_{max} sensitivity

f_T, f_{max} sensitivity to 100% change in small-signal parameters:



R_G, R_D have big impact on f_{max} and do not scale well

Reason for f_{max} degradation

Does poor scalability of R_G, R_D alone explain f_{max} degradation?

Use small-signal model for W = 96 μm device in ADS

$R_G \uparrow$ 120% and $R_D \uparrow$ 180% keeping all else constant

	f_T			f_{max}		
Modeled W: 96 μm. R_G, R_D ↑	142 GHz	→	112 GHz	180 GHz	→	95 GHz
Measured W: 96 μm -1536 μm	142 GHz	→	110 GHz	190 GHz	→	90 GHz

$W \uparrow \Rightarrow f_T \downarrow$ because $R_D \uparrow$

$W \uparrow \Rightarrow f_{max} \downarrow$ because R_G and $R_D \uparrow$

Analytical Expressions for f_T, f_{max}

- Useful to have simple expressions for f_T and f_{max}
- Substrate parameters (R_{sx}, C_{db}, C_{sb}, C_{gb}) ignored
- ω^2 and higher order terms ignored
- Traditional derivations for f_{max} only include R_G

Tasker's [2] expression:

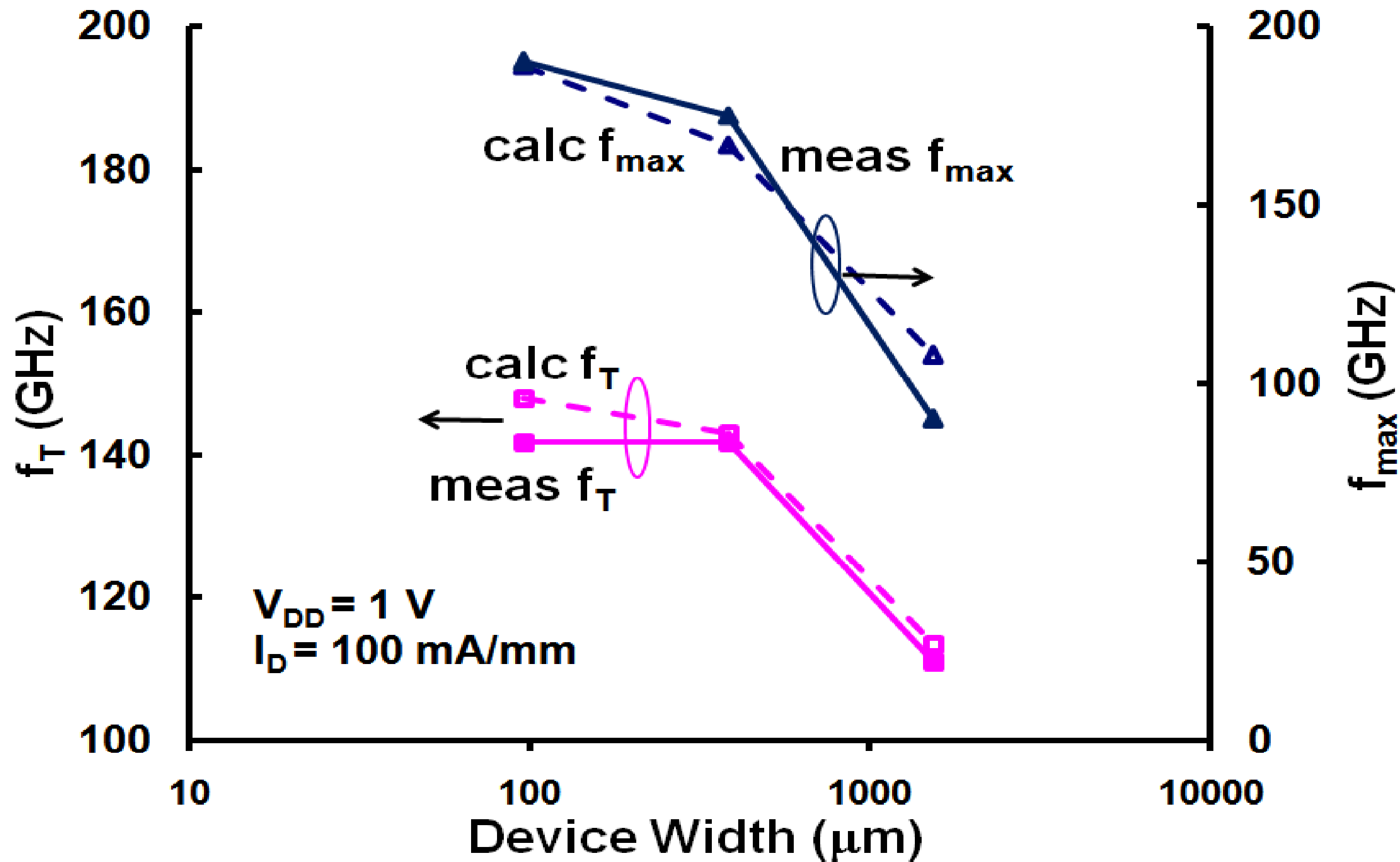
$$f_T \approx \frac{g_m}{2\pi\left[C_{gs}(1+\frac{R_D+R_S}{r_o})+C_{gd}(1+(R_D+R_S)(g_m+\frac{1}{r_o}))\right]}$$

New expression:

$$f_{\max} \approx \frac{g_m\sqrt{1+g_mR_S+g_{ds}(R_D+R_S)}}{\begin{aligned}4\pi[&C_{gs}^2(R_G+R_S)g_{ds}(1+g_mR_S)+C_{gd}^2((R_G+R_D)(g_m+g_{ds})\\&+(g_m+g_{ds})^2(2R_GR_S+R_GR_D+2R_SR_D))+C_{gs}C_{gd}(R_G(g_m+2g_{ds})\\&+g_mg_{ds}(5R_GR_S+3R_GR_D+2R_SR_D)+g_m^2R_GR_S)]\end{aligned}}$$

2. Tasker, EDL '89

Measured and Analytical f_T, f_{max}



- Excellent agreement between analytical and measured data
- Model useful to understand impact of width scaling on high frequency characteristics

Conclusions

- Studied frequency response of 65 nm CMOS devices
- f_T and f_{max} decrease with increasing device width
- Accurate small-signal circuit parameters extracted
- f_T, f_{max} ↓ because R_G and R_D ↑ as W ↑
- Analytical model of f_T, f_{max} models width behavior well

Key to enabling CMOS for mm-wave applications is a parasitic-aware approach when designing wide devices

Technology Transfer

Liaison Interactions:

- Industrial Liaisons: David Greenberg, Alberto Valdes Garcia (IBM Microelectronics)
- Several teleconferences with liaisons over academic year
- More frequent interaction during internships
- Device designs done with input from Liaisons

Internships:

- Summer 2007 and summer 2008 at IBM Microelectronics
- Design work carried out at IBM Microelectronics
- 65 nm and 45 nm designs manufactured by IBM

Publications / Presentations:

Task reports published on SRC website regularly

SiRF 2010: 45 nm power and frequency response