nanoHUB online simulation and more — an NCN project

Performance Analysis of Ultra-Scaled InAs HEMTs

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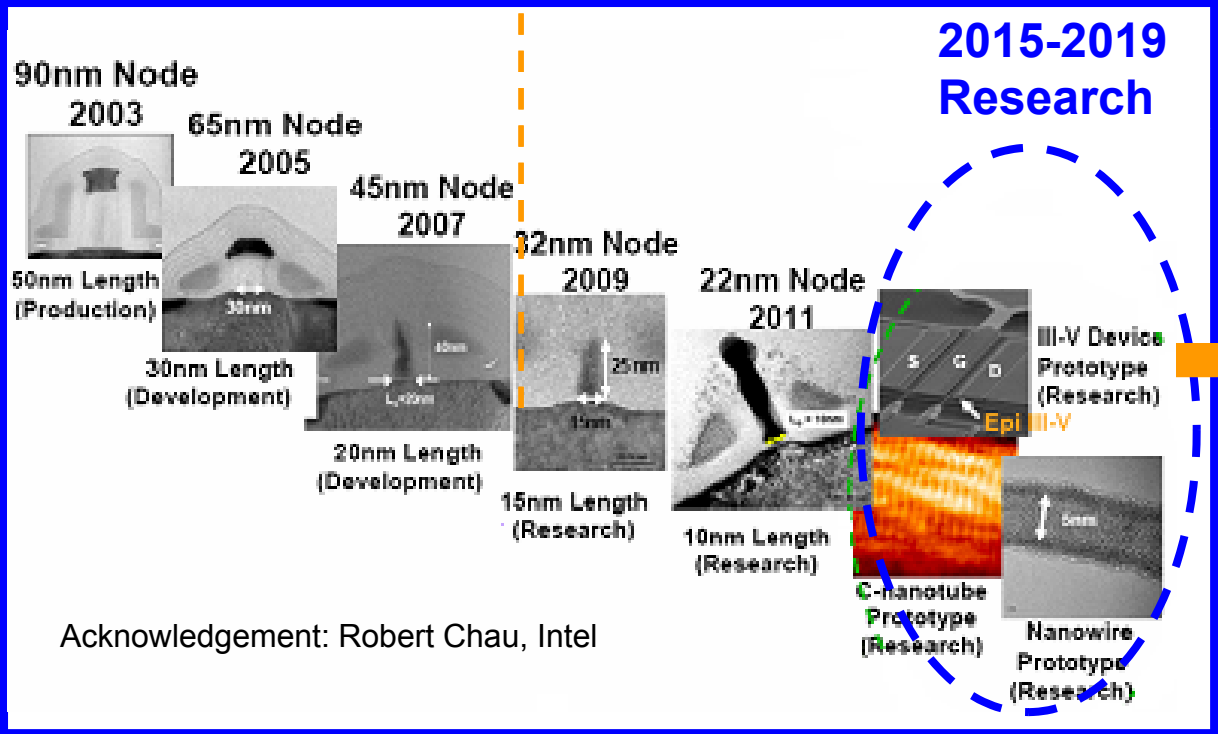
PURDUE UNIVERSITY

NCN NSF

Motivation: Towards III-V MOSFET

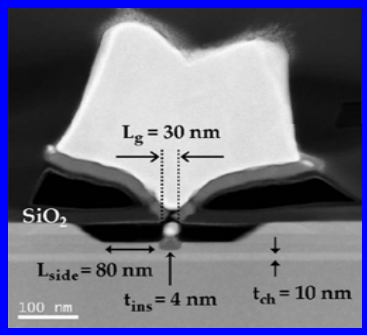
- Strained channel
- New gate dielectrics

- Device geometries
- Channel materials
- High-k dielectrics



Acknowledgement: Robert Chau, Intel

III-V channel devices

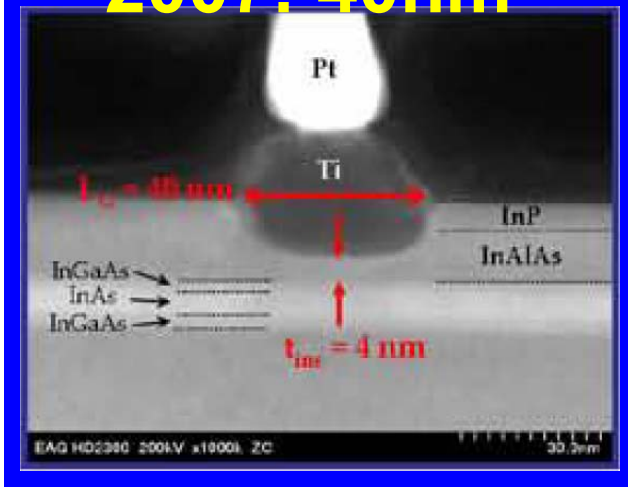


Low-power & high-speed

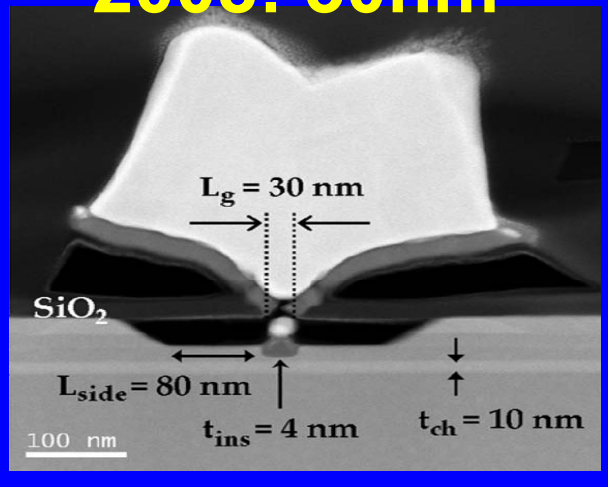
Motivation: Why III-V HEMTs?

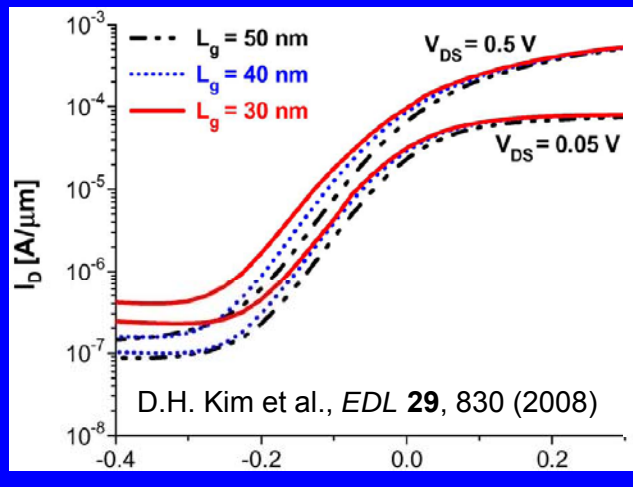
- **III-V**: Extraordinary electron transport properties
- **HEMTs**: Very similar structure to MOSFETs except high-κ dielectric layer
- **Excellent to Test Performances** of III-V material without interface defects
- **Excellent to Test Simulation Models**
  - Develop simulation tools and benchmark with experiments
  - Predict performance of ultra-scaled devices

2007: 40nm



2008: 30nm





Outline

- **Motivation**
- **Modeling Approach**
  - **Real-space EM simulator including gate leakage**
  - **Atomistic tight-binding m***
  - **Realistic description of simulation domain (gate geometry)**
- **Comparison to Experiments L_g=30, 40, 50nm**
  - Material **parameters, I_d-V_{gs}, I_d-V_{ds}**
- **Scaling Considerations for L_g=20nm**
  - **Channel thickness, Insulator thickness, Gate metal work function**
- **HEMT Simulator on nanoHUB.org**
- **Conclusion and Outlook**

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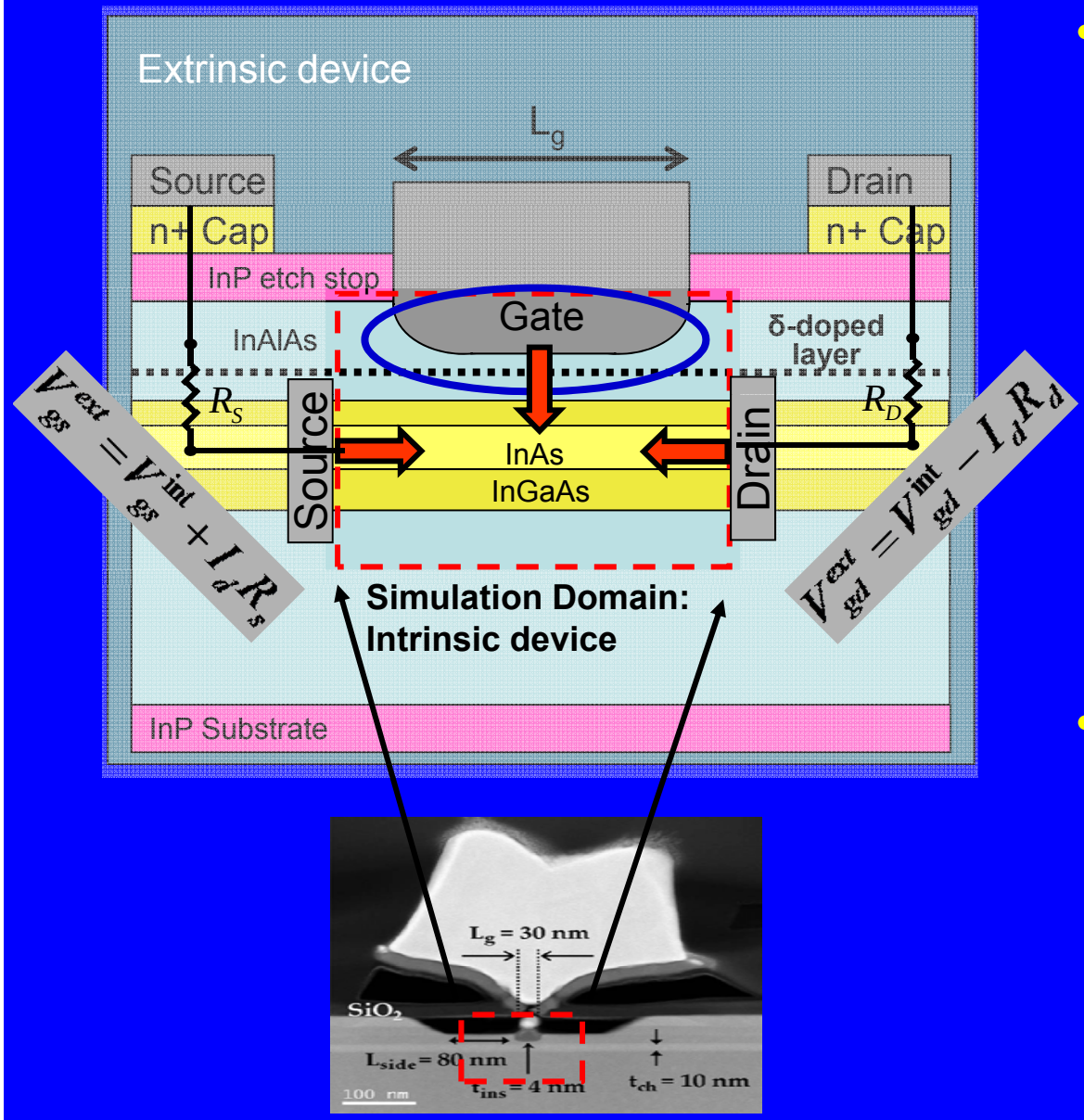
Device Geometry and Simulation Domain



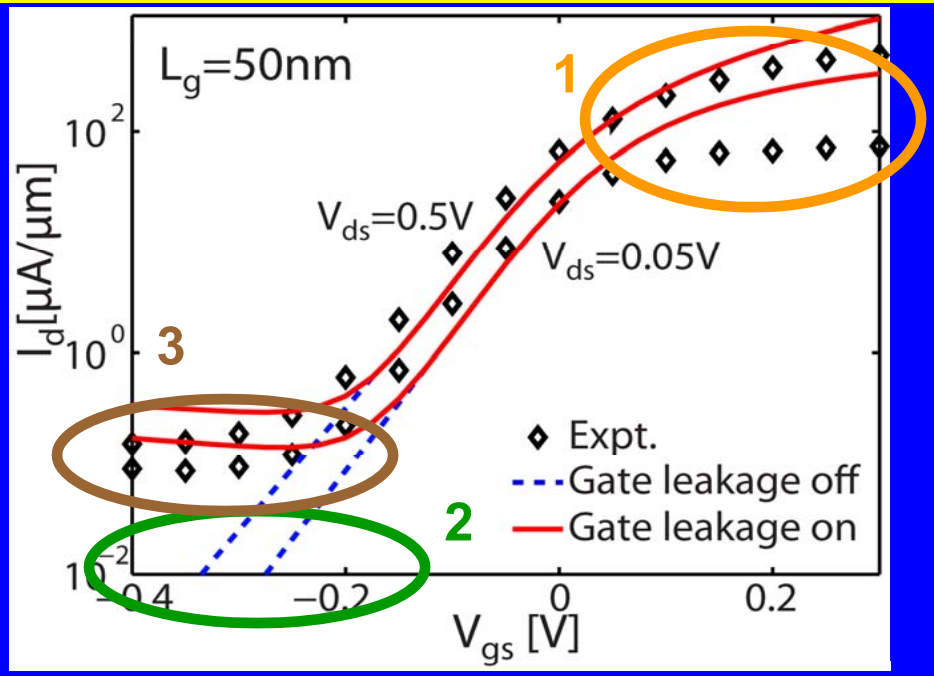
- **Intrinsic device**
  - Near gate contact
  - Self consistent 2D Schrodinger-Poisson
  - Electrons injected from all contacts

M. Luisier et. al., IEEE Transactions on Electron Devices, vol. 55, p. 1494, (2008).

- Extrinsic source/drain contacts
  - Series resistances R_S and R_D

R. Venugopal et.al., Journal of Applied Physics, vol. 95, p. 292, (2004).

Gate Geometry and Gate Leakage Current



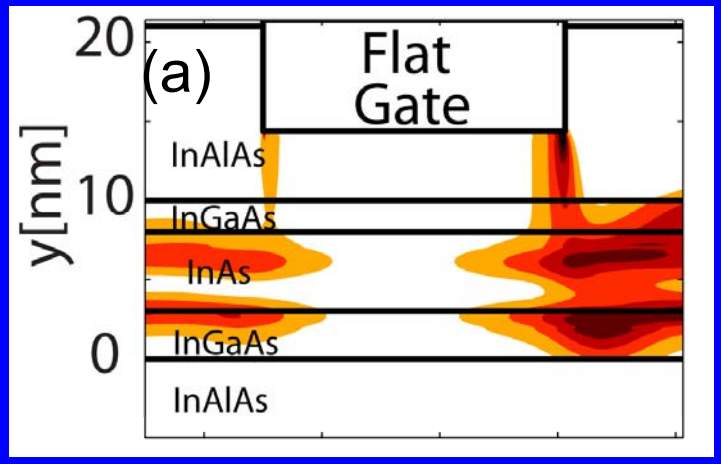
1) **Include series resistances**

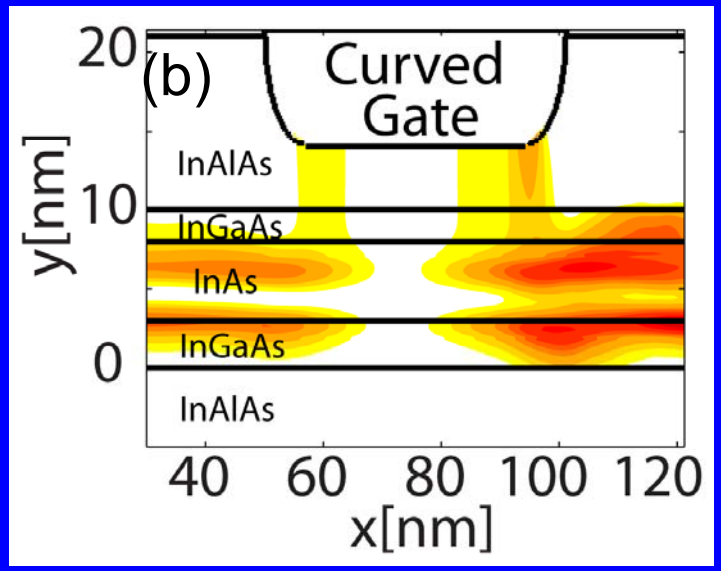
$$V_{gs}^{ext} = V_{gs}^{\text{int}} + I_d R_s \quad V_{ds}^{ext} = V_{ds}^{\text{int}} + I_d (R_s + R_d)$$

2) **Include gate leakage current**

$$(E - H - \Sigma^S - \Sigma^D - \Sigma^G) \bullet C = (S^S + S^D + S^G)$$

3) **Include the proper gate geometry flat (a) or curved (b)**





Gate leakage reduced in curved gate device

Accurate Effective Mass Calculation

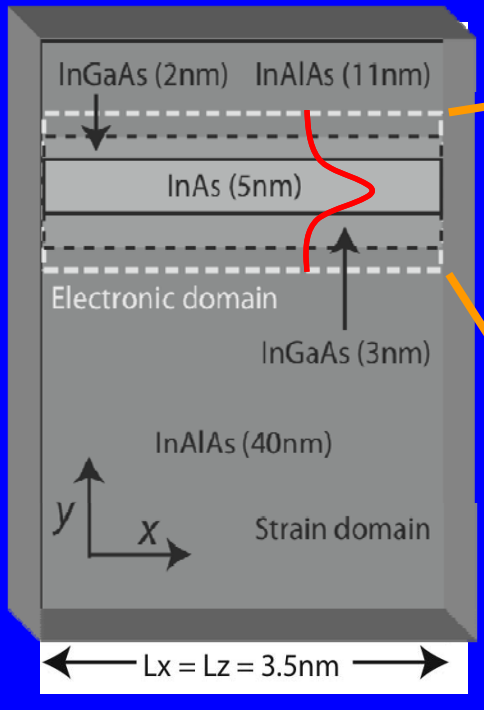
Full-Band Transport:

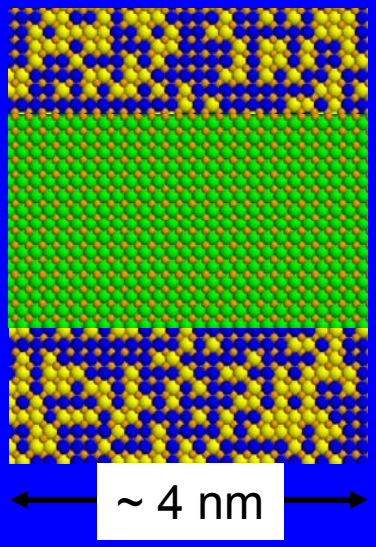
- Strain, Disorder, Non-parabolicity, BTBT
- No gate leakage, Computationally very intensive

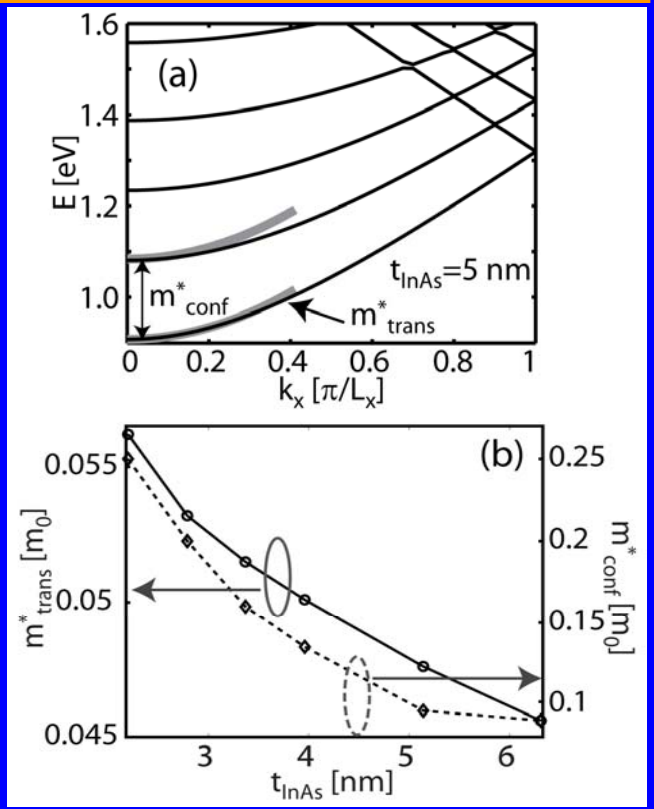
Import m*

Effective Mass Transport:

- Gate leakage, Computationally efficient
- Parabolic bands, No disorder, Wrong quantization levels







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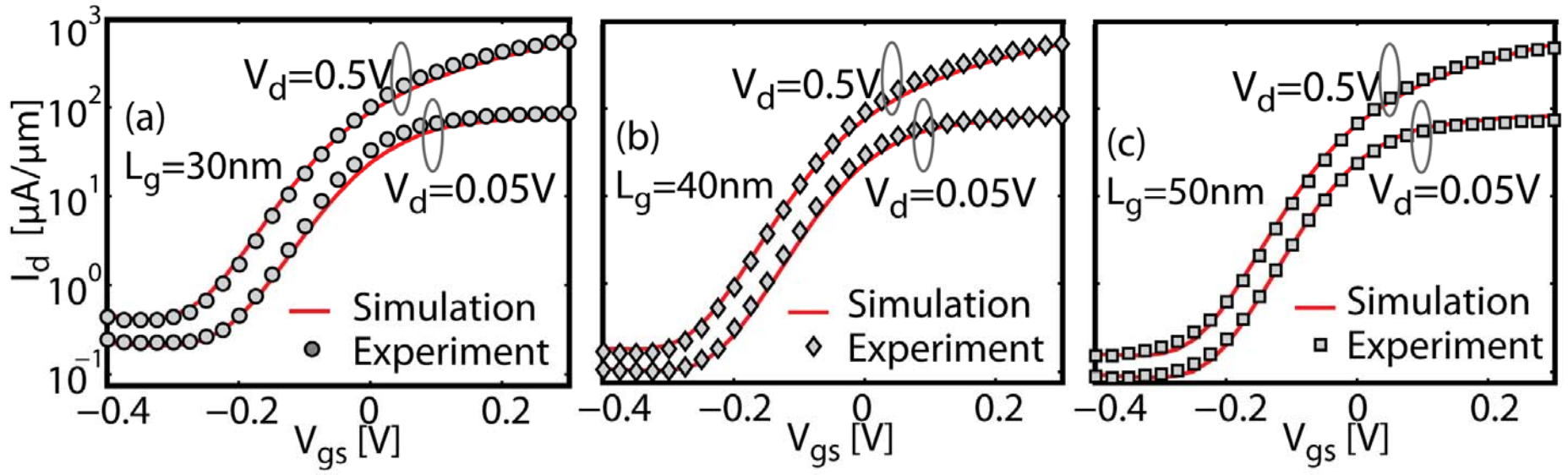
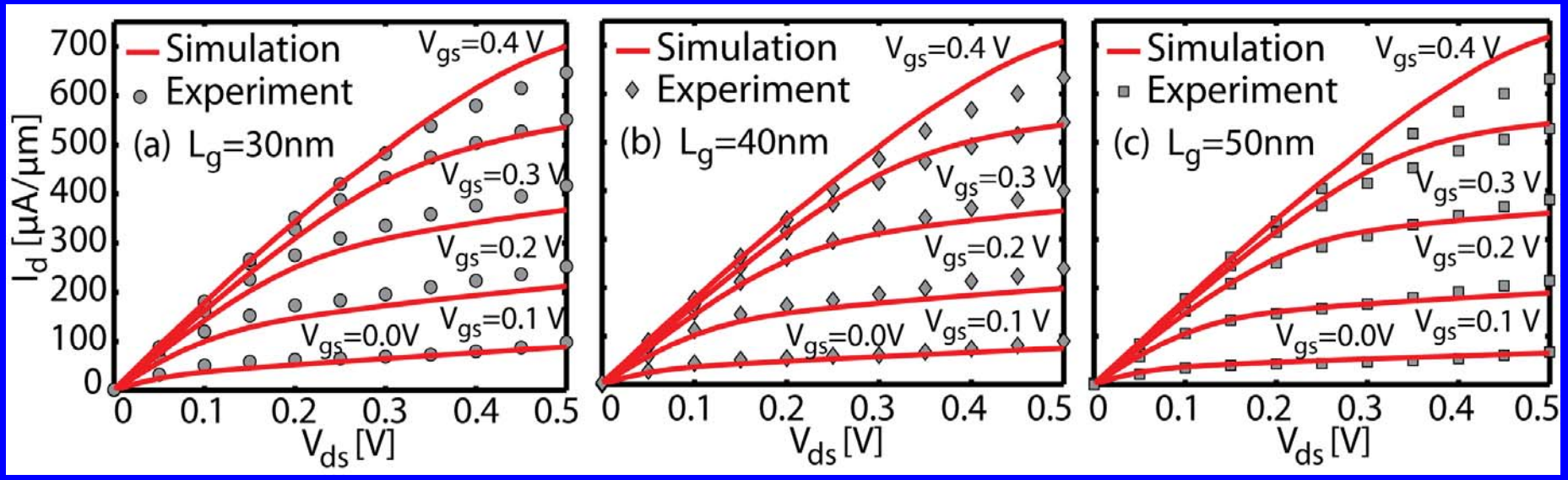
Transfer Characteristics: I_d-V_{gs}



Parameter	Initial	Final parameter set		
		30	40	50
L_g [nm]	30, 40, 50	34.0	42.0	51.25
t_{ins} [nm]	4	3.6	3.8	4.0
Φ_M [eV]	4.7	4.66	4.69	4.68
m^*_{ins} (InAlAs)	0.075	0.0783	0.0783	0.0783
m^*_{buf} (InGaAs)	0.041	0.0430	0.0430	0.0430

Output Characteristics: I_d-V_{ds}



Conclusion:

- **Good agreement for all L_g's**
- **Less ballistic at L_g=50nm**
- **Use models and material parameters to design ultra-scaled devices (L_g=20nm)**

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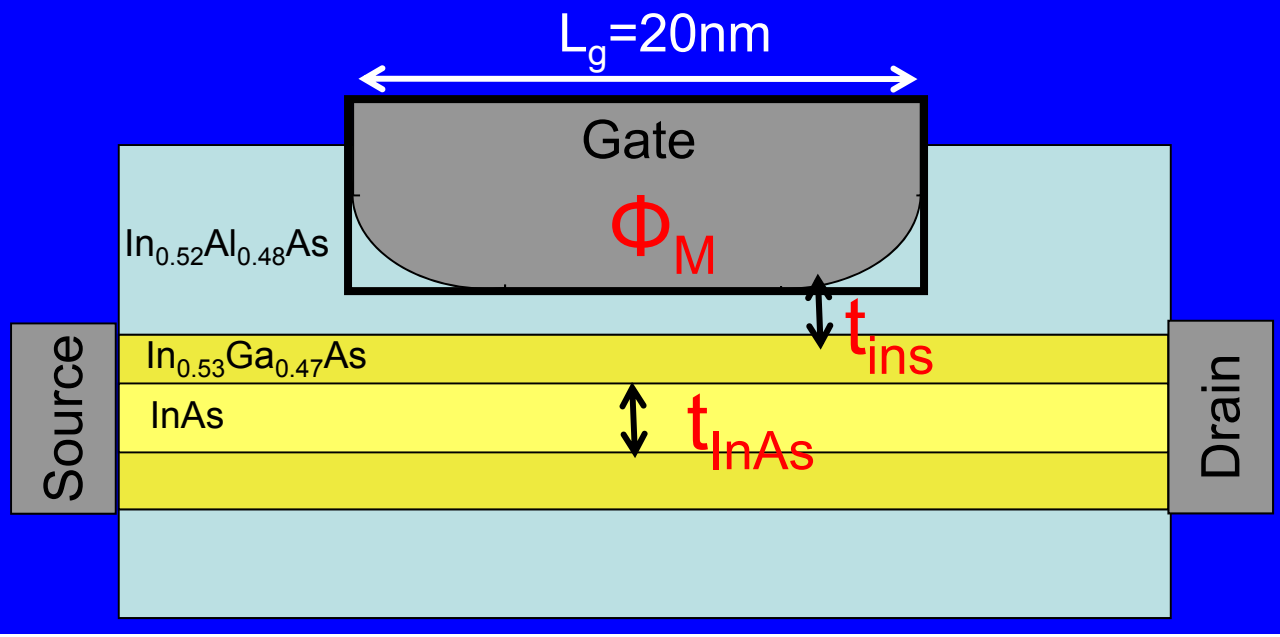
What can be changed?

- Gate geometry
- Channel thickness scaling: t_{InAs}
- Insulator thickness scaling: t_{ins}

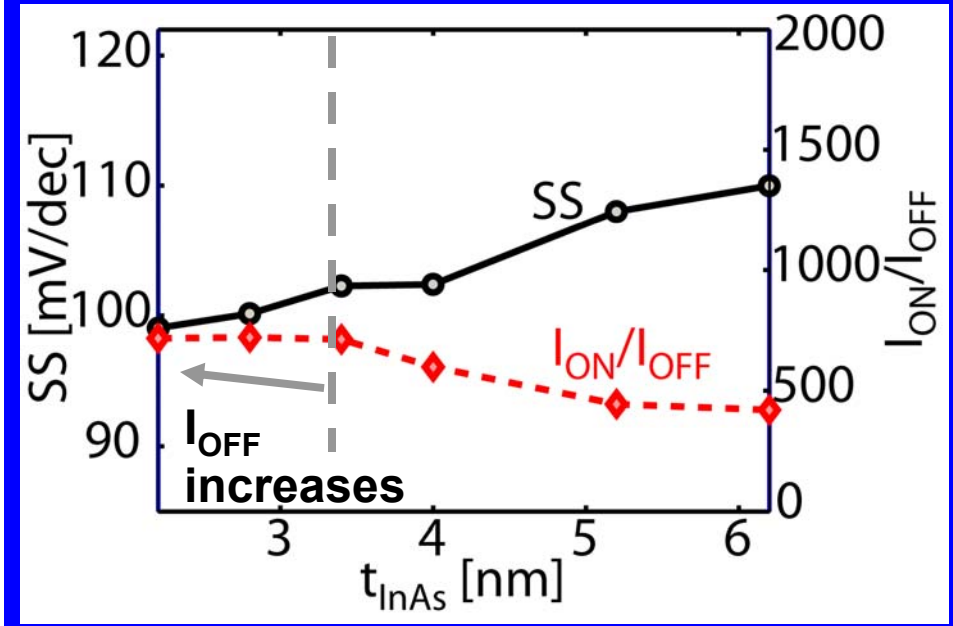
Better control of surface potential

- Metal work function engineering: Φ_M

Gate leakage reduction and E-mode operation

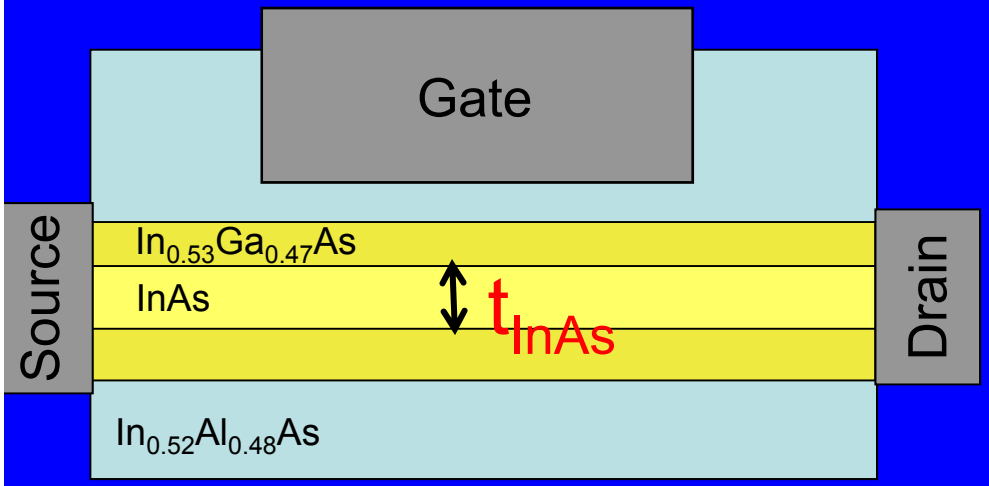


InAs (Channel) Layer Thickness

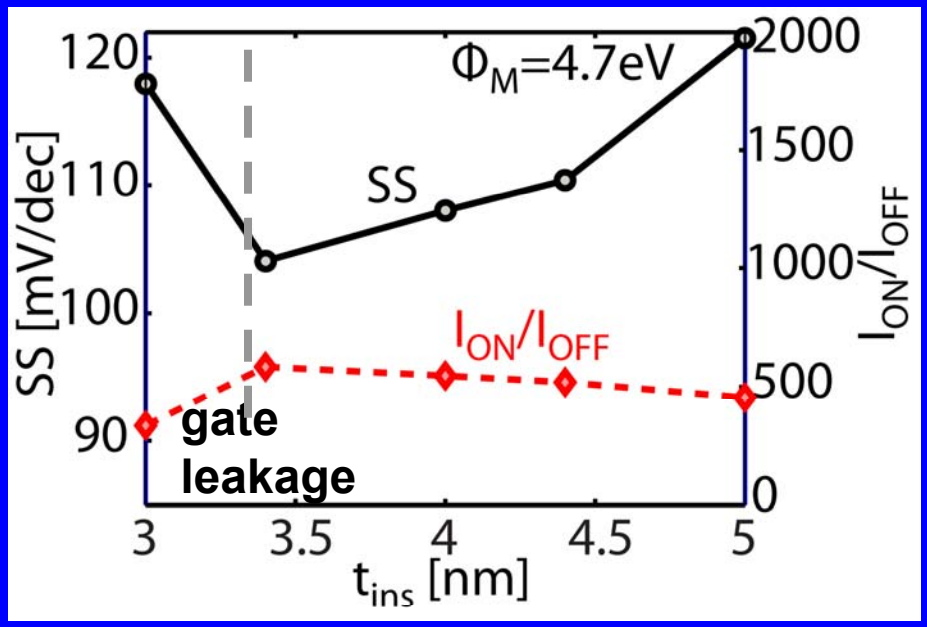


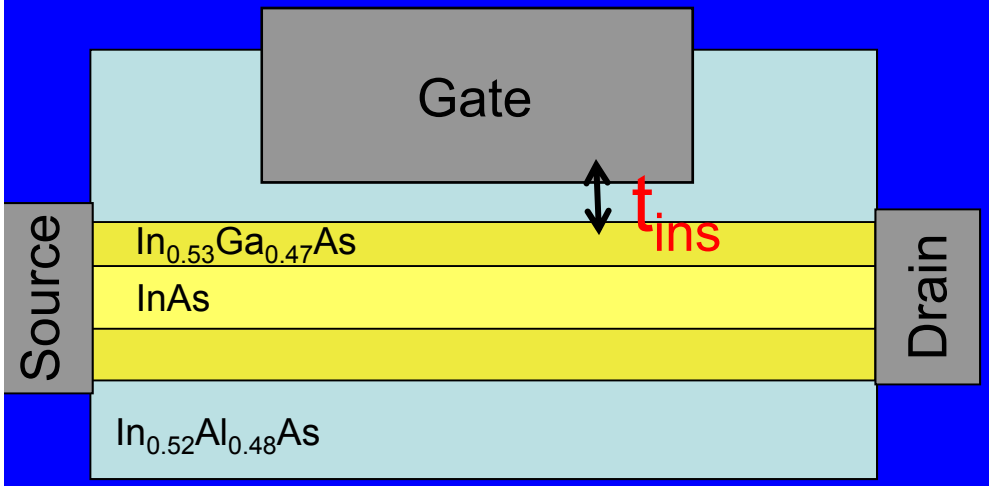
InAs Channel Scaling:

- Better electrostatic control
  - lower SS
  - larger I_{ON}/I_{OFF} ratio
- Increase of transport m*
  - reduced v_{inj}, higher N_{inv} => higher I_{ON}
- Increase of gate leakage current
  - I_{ON}/I_{OFF} ratio saturates



InAlAs (Insulator) Layer Thickness

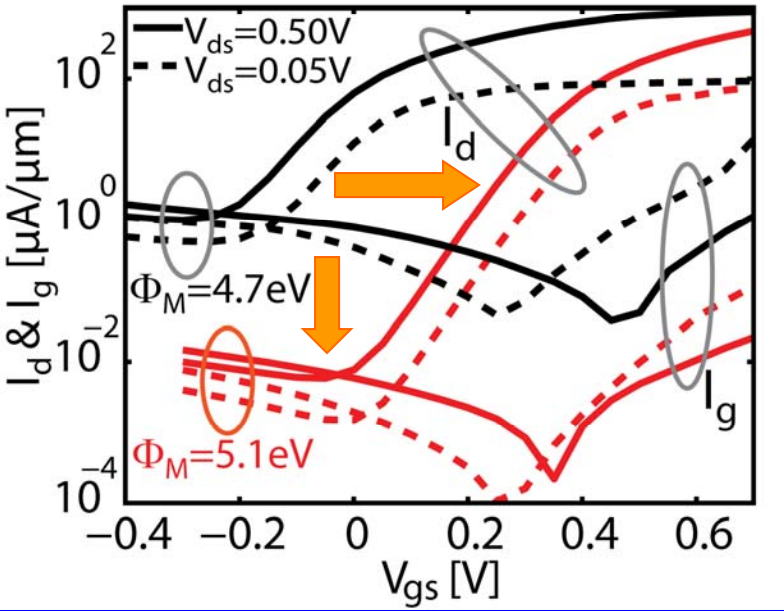




InAlAs Insulator Scaling:

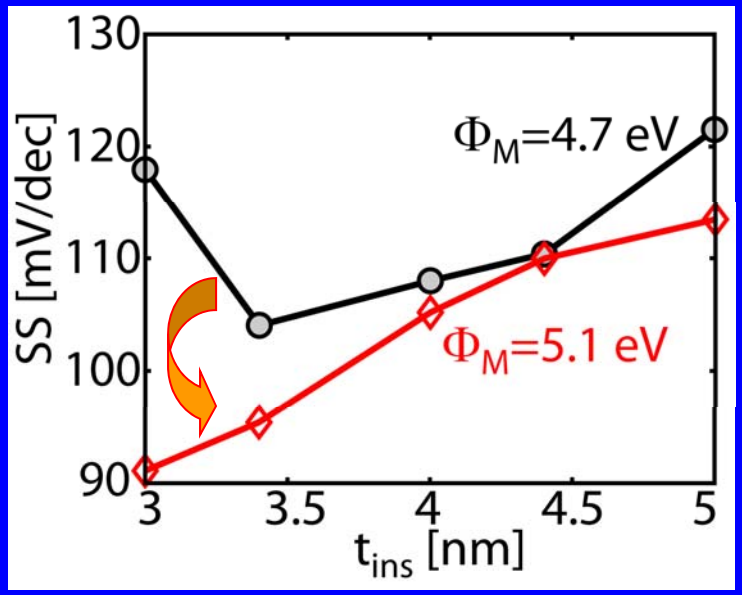
- Better electrostatic control (due to larger C_{ox})
- Increase of gate leakage current
  - larger I_{OFF}
  - larger SS
  - smaller I_{ON}/I_{OFF} ratio

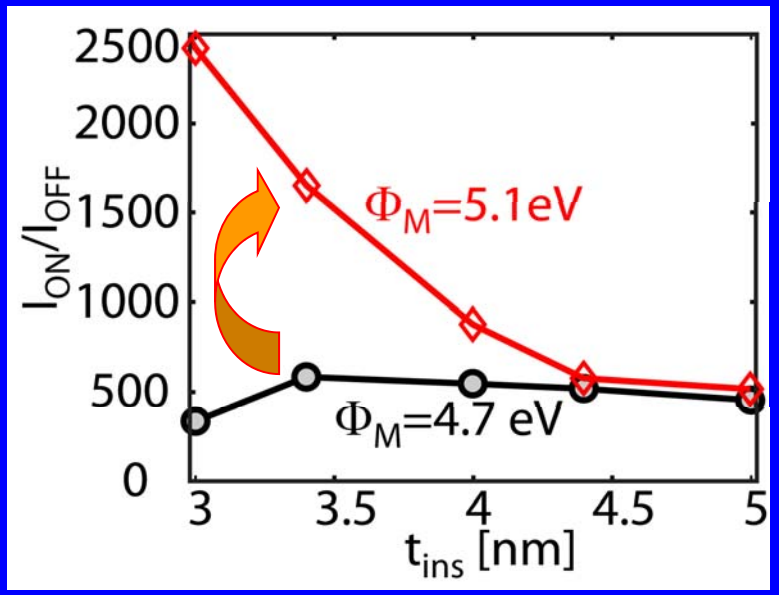
Work Function Engineering



Work Function Increase:

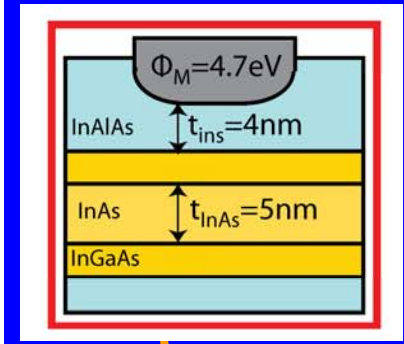
- Shift towards enhancement mode
- Decrease of gate leakage current
- Allows for thinner insulator layer
  - steeper SS
  - larger I_{ON}/I_{OFF} ratio





Parameters and Performances Summary

(1) Gate geometry (2) Channel thickness (3) Insulator thickness (4) Metal work function

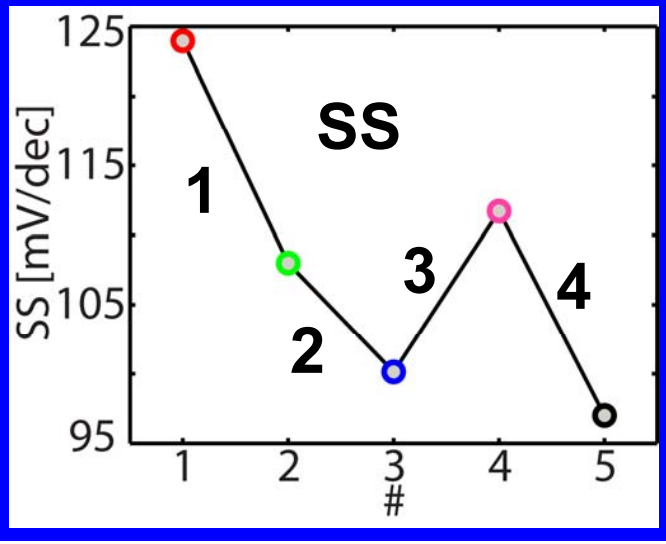


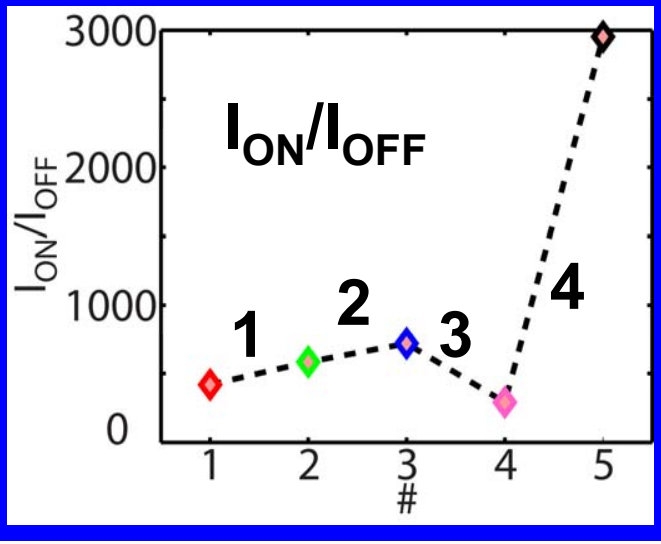
Improved gate control

Higher gate leakage

Gate leakage reduction

L_g=20nm





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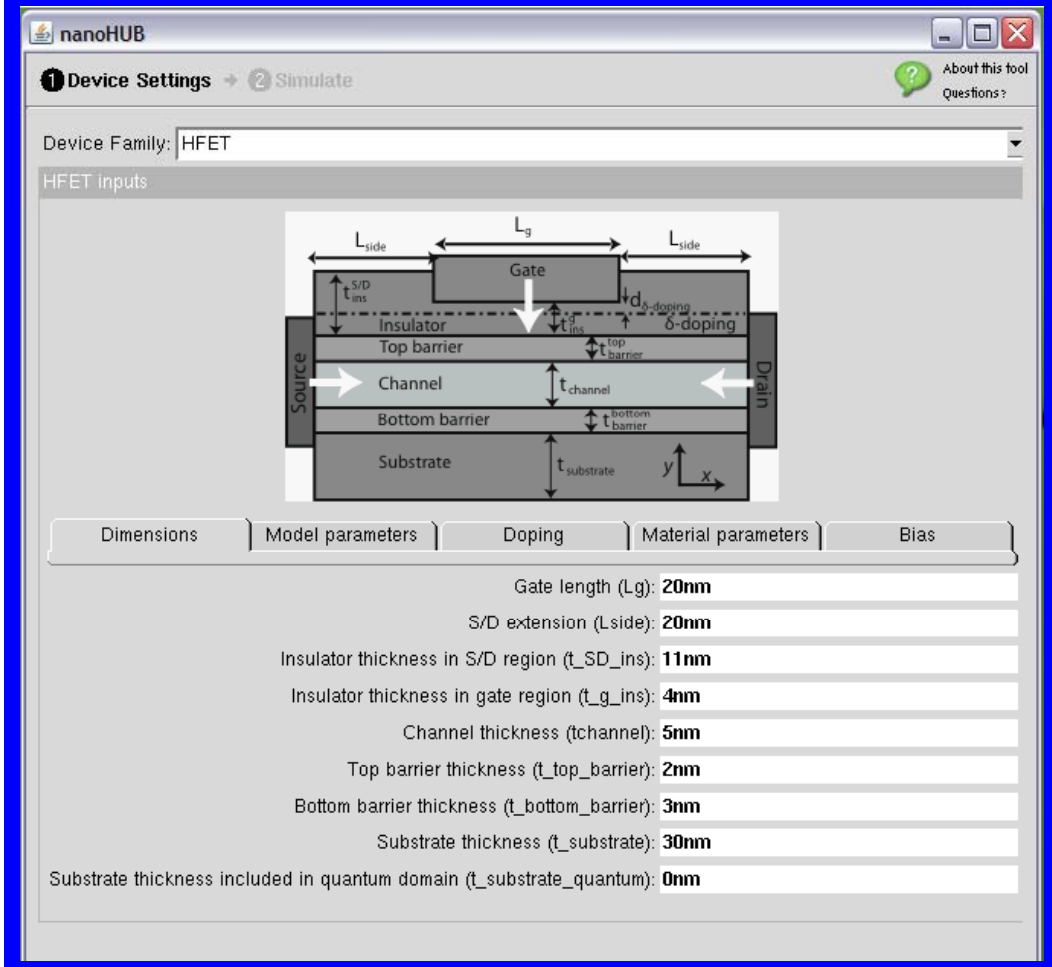
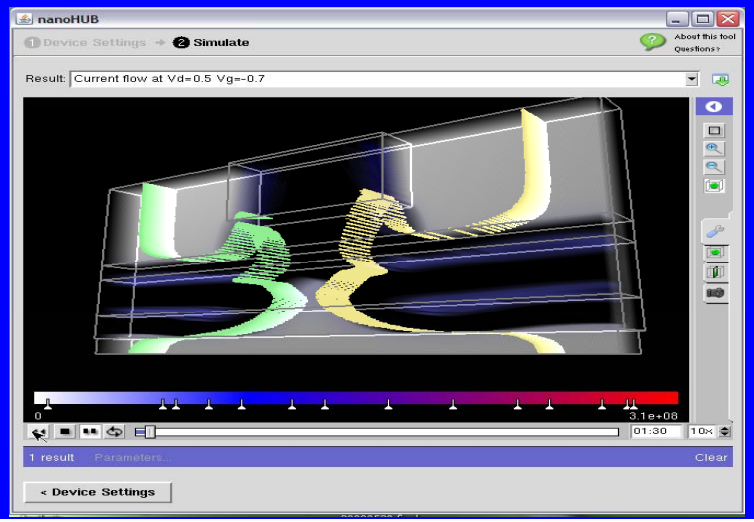
HEMT Simulator on nanoHUB.org



OMEN_FET:

- 2-D Schrödinger-Poisson solver
- Real-space effective mass quantum transport model
- Injection (white arrows) from Source, Drain, and Gate contacts
- HEMTs, Single- and Double-Gate devices
- Electron transport in Si and III-V
- Ballistic transport (no Scattering)
- **Current Flow Visualization**

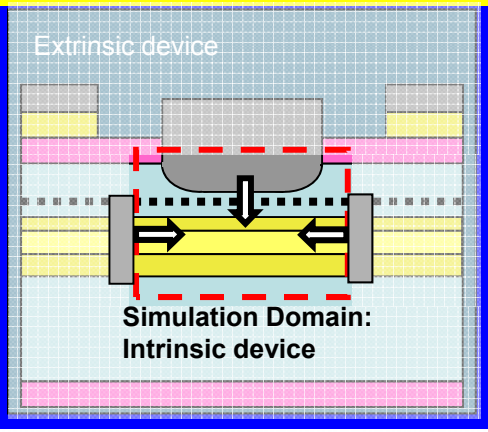


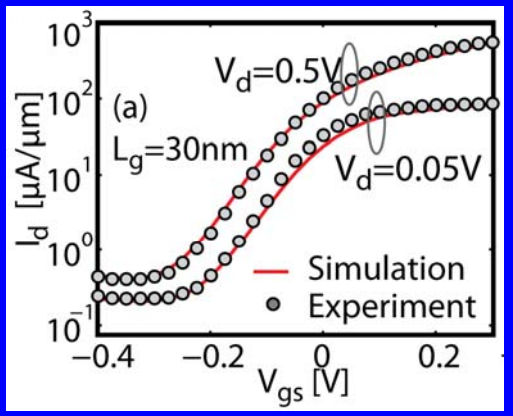
http://nanoHUB.org/tools/omenhfet

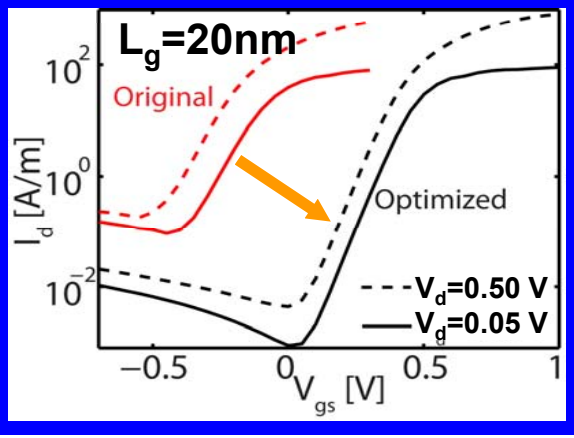
Run your own simulations!

Conclusion and Outlook

- **Multiscale Modeling Approach**
  - EM transport including gate leakage
  - m* from tight-binding
- **Good Agreement with Experiments**
- **Scaling Considerations for 20nm Device**
- **HEMT Simulator Deployed on nanoHUB.org**
- **Challenges and Future Directions**
  - S/D contacts, high-k insulator, scattering, interface traps

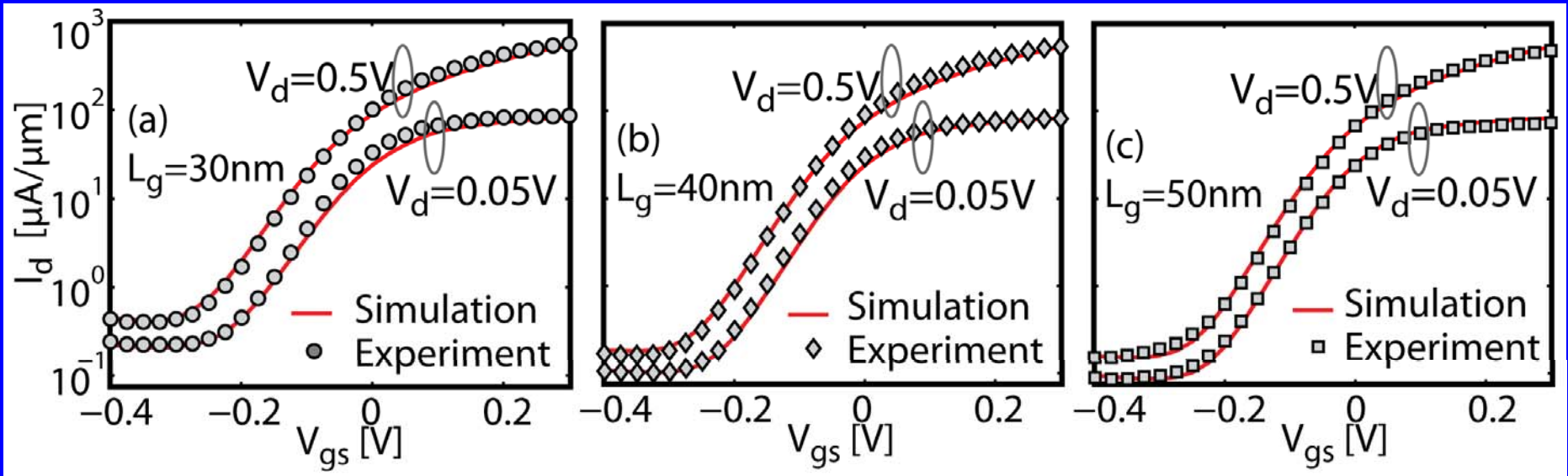






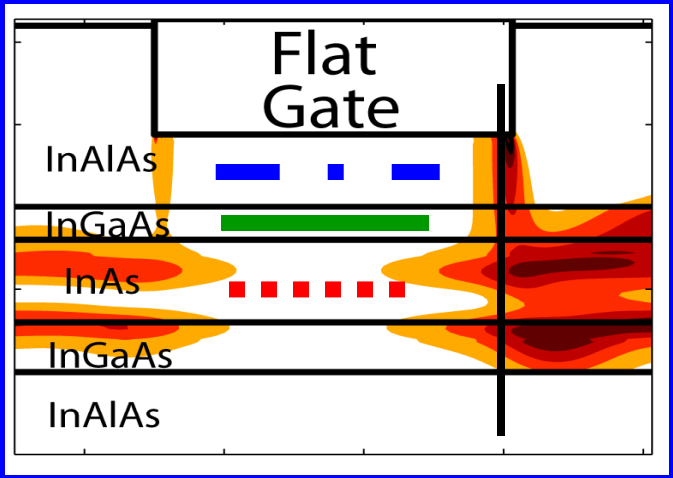
Thank You!

Transfer Characteristics: I_d-V_{gs} (2)

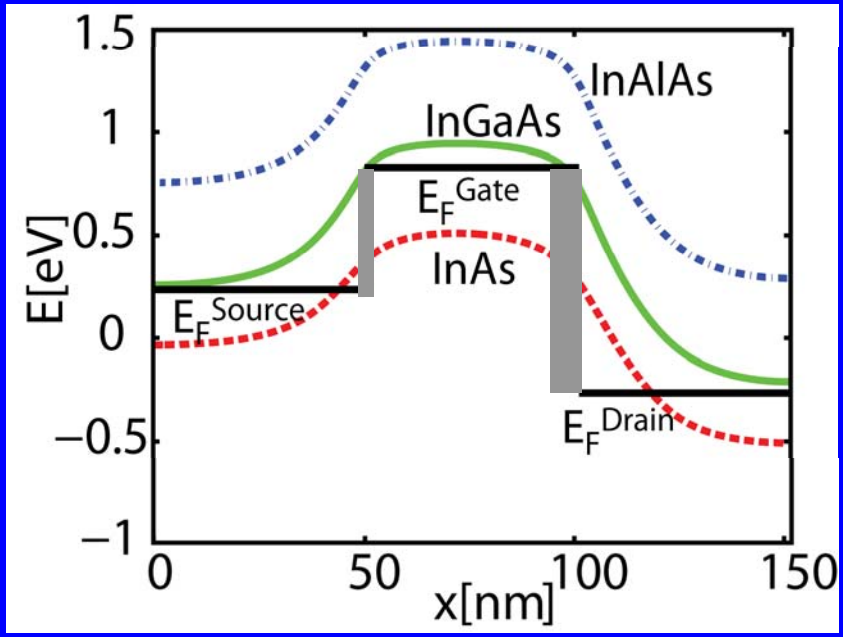


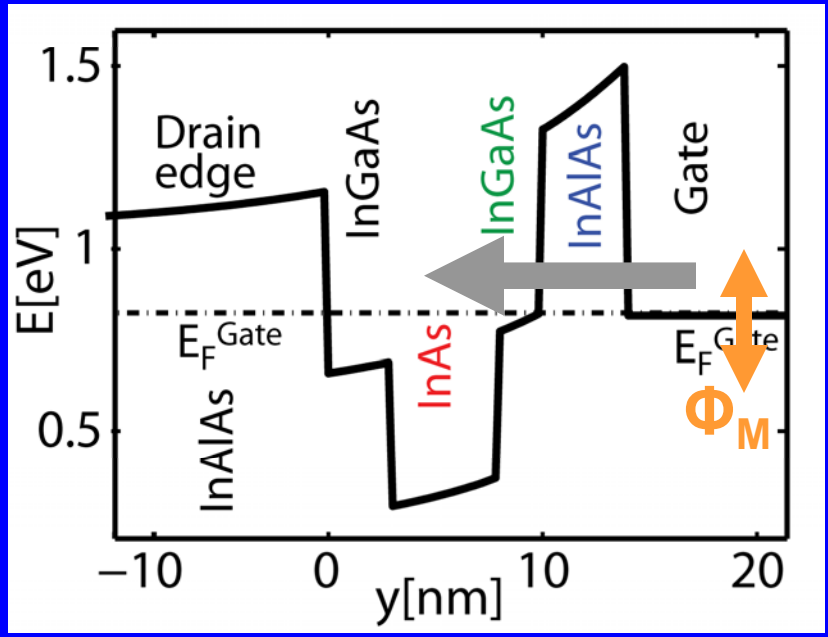
L_g [nm]		SS [mV/dec]	DIBL [mV/V]	I_{ON}/I_{OFF}	V_{inj} [cm/s]
30	Expt.	107	169	0.47×10^3	
	Sim.	105	145	0.61×10^3	3×10^7
40	Expt.	91	126	1.38×10^3	
	Sim.	89	99	1.86×10^3	3.11×10^7
50	Expt.	85	97	1.80×10^3	
	Sim.	89	91	1.85×10^3	3.18×10^7

Gate Leakage Mechanism



- **Electrons tunnel from gate into InAs channel**
- **Tunneling barriers**
  - InAlAs and InGaAs
  - Position dependent barriers
- Current crowding at edges (due to lower tunneling barriers)
- Barriers modulated by Φ_M

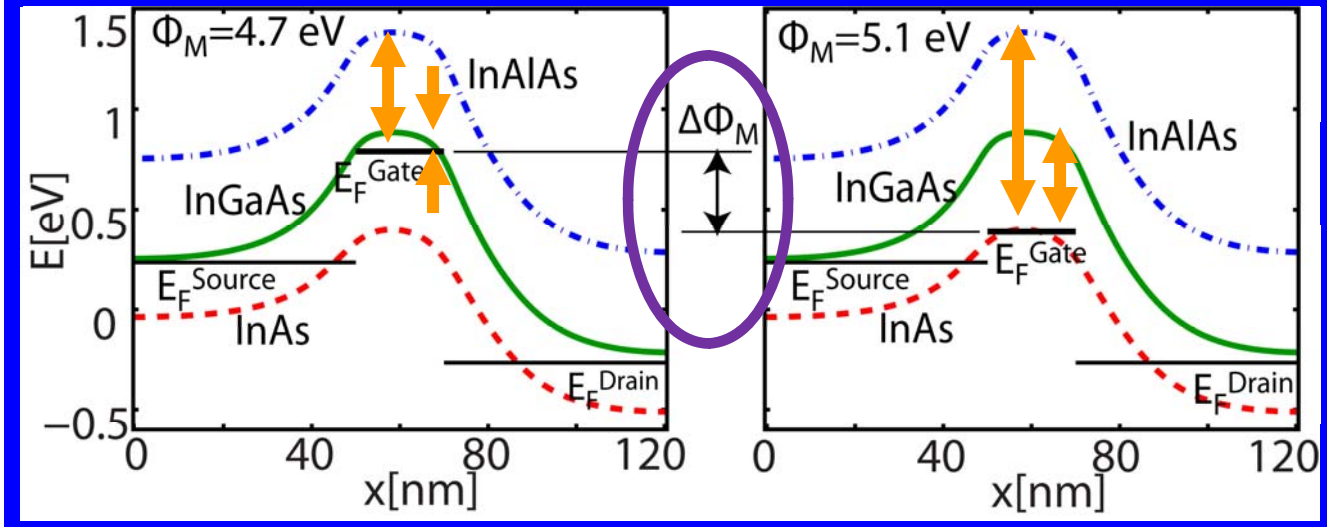


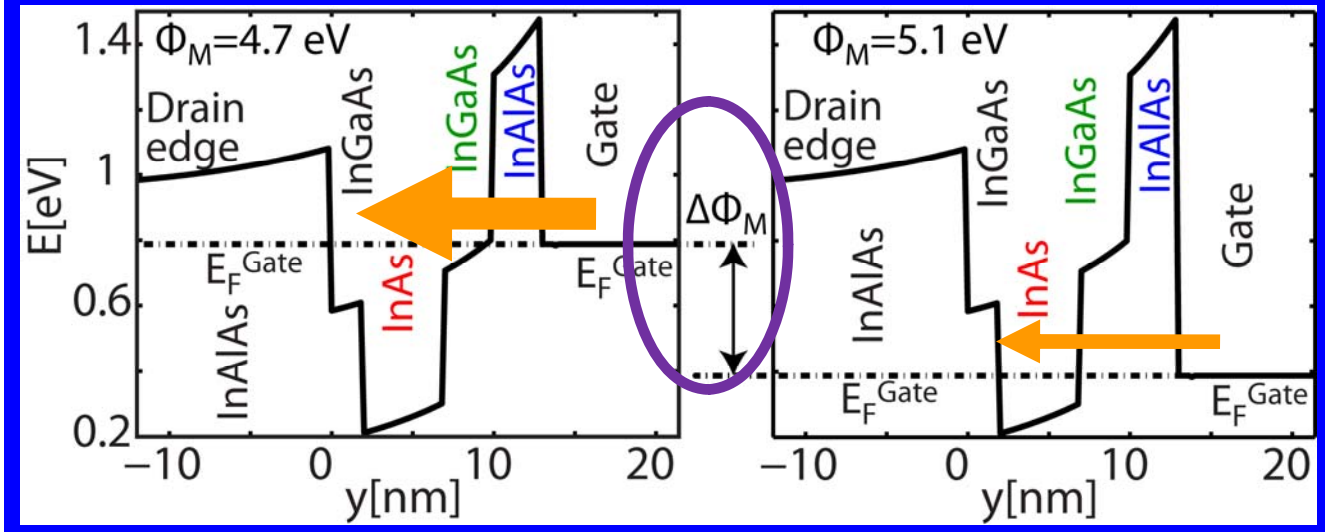


Work Function Engineering (2)

Φ_M =4.7 eV

Φ_M =5.1 eV





Characteristics:

- Same Gate Overdrive
  - same thermionic current (source to drain)
- Gate Fermi levels shifted by $\Delta\Phi_M$
  - different tunneling barrier height
- Φ_M =4.7 eV
  - tunnel through InAlAs only
  - larger I_g
- Φ_M =5.1 eV
  - tunnel through InAlAs and InGaAs
  - lower I_g