Quantum Capacitance in Scaled-Down III-V FETs

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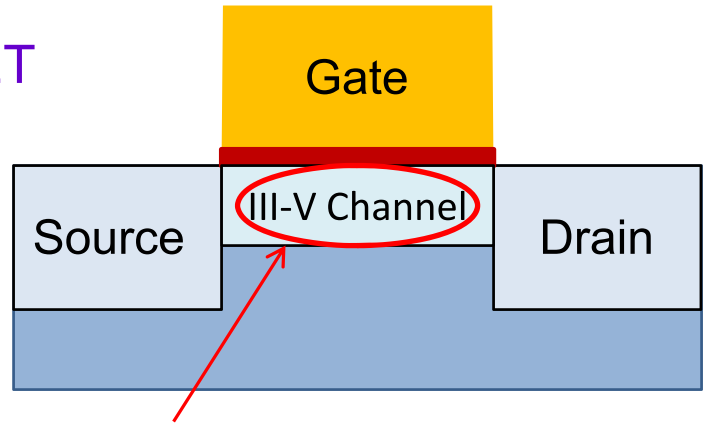
Overview

1. Motivation
2. Gate Capacitance Model for III-V FETs
3. Measurements of C_G on InGaAs HEMTs
4. Comparison of Model and Experiments
5. Projection for 10 nm III-V MOSFETs
6. Conclusions

1. Motivation : III-V CMOS

III-V MOSFET



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  - High electron velocity → Low effective mass (m^*)

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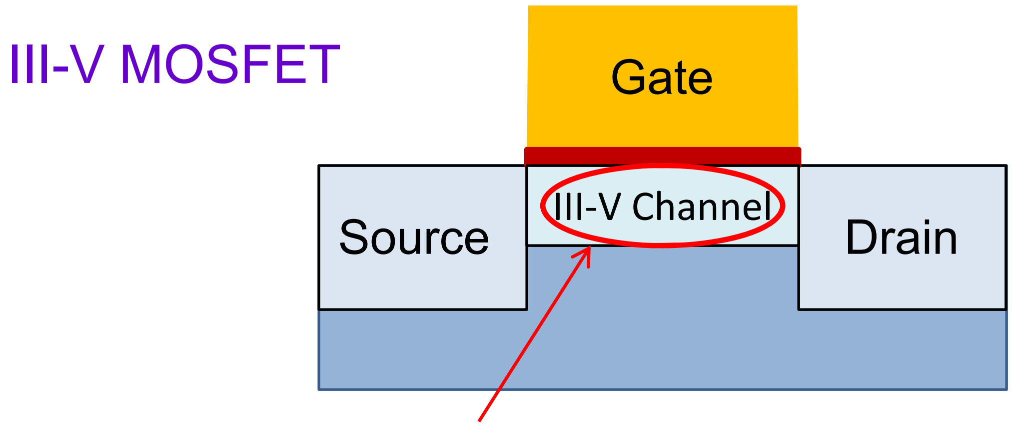
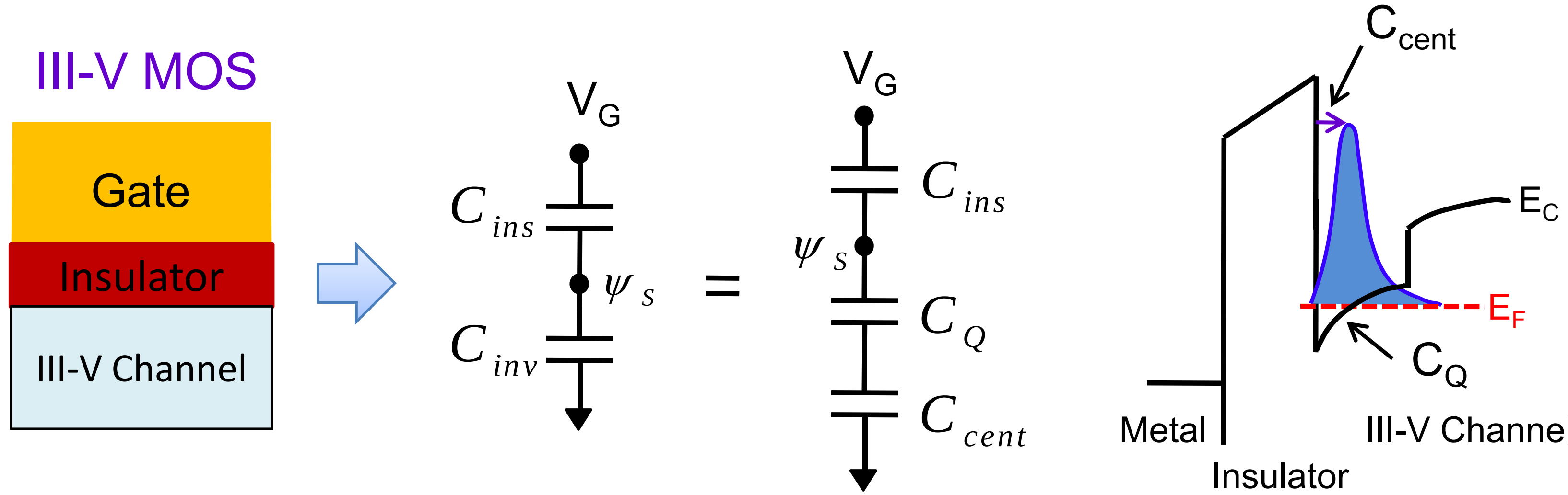


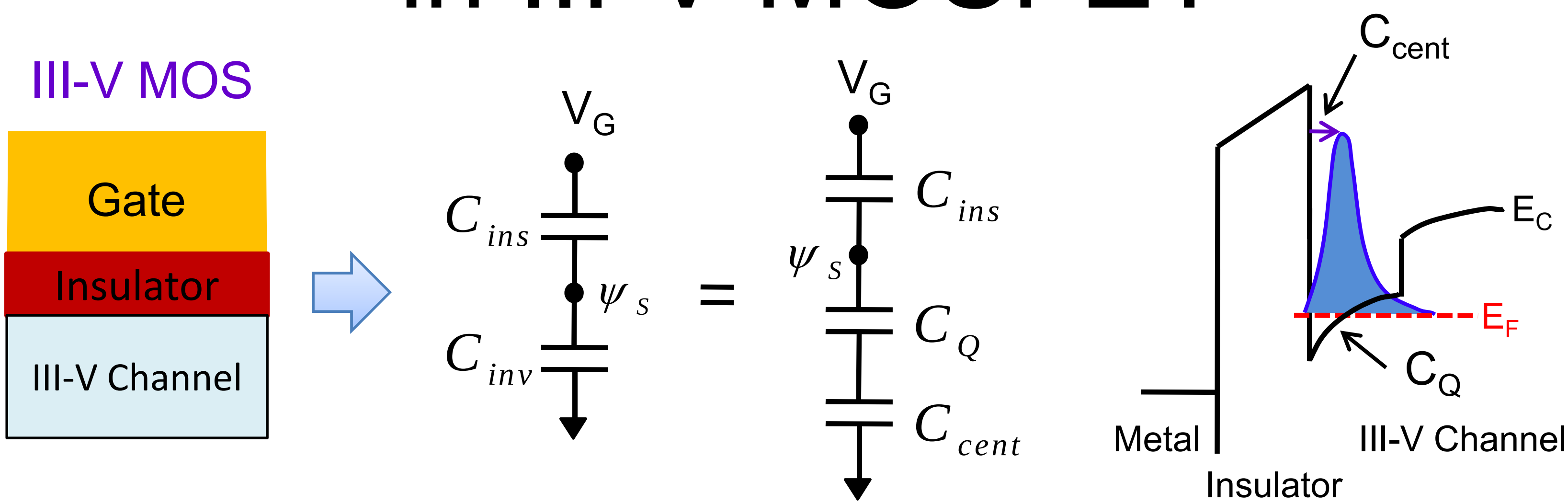
- III-V CMOS: III-V semiconductor in channel
  - High electron velocity → Low effective mass (m^*)
- Low m^* → small Density of States (DOS)
  → low sheet carrier concentration (N_S) in channel
- Will III-V CMOS attain required N_S at the 10 nm node?

Gate Capacitance in III-V MOSFET



- Inversion-layer capacitance (C_{inv}) is series of
  - Quantum capacitance (C_Q):
    → E_F penetration in CB, proportional to DOS
  - Centroid capacitance (C_{cent}):
    → Finite distance of electrons away from interface

Gate Capacitance in III-V MOSFET



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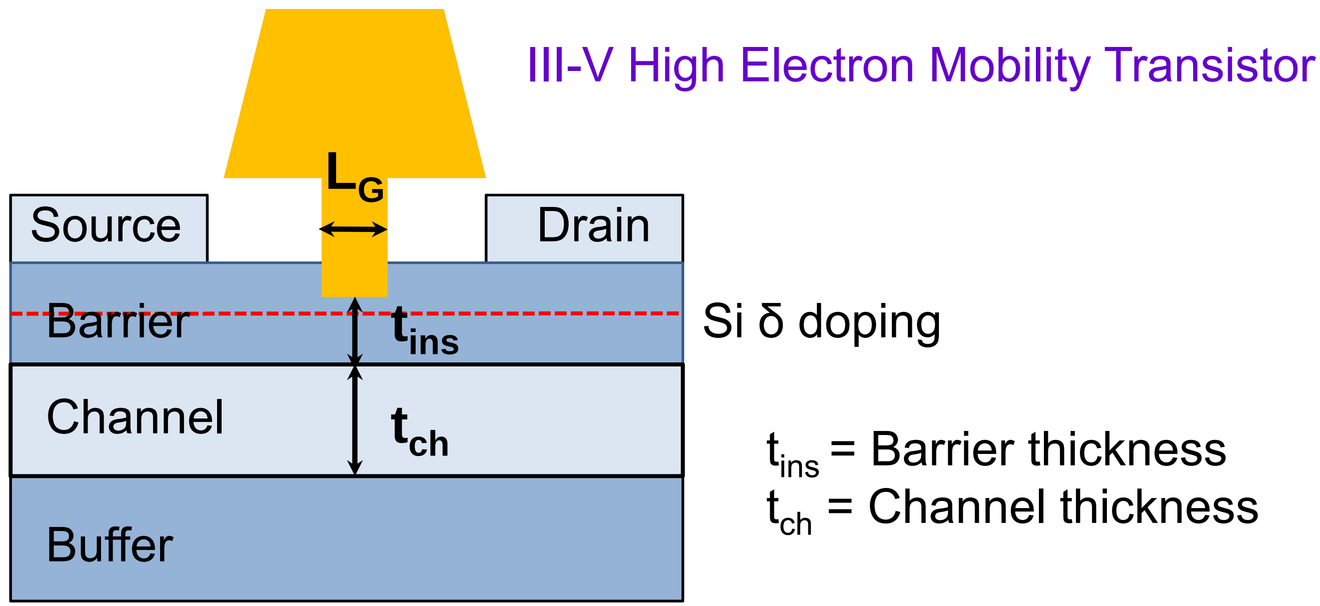
m*↓ → DOS↓ → C_Q↓ → Problem in III-V MOSFET?

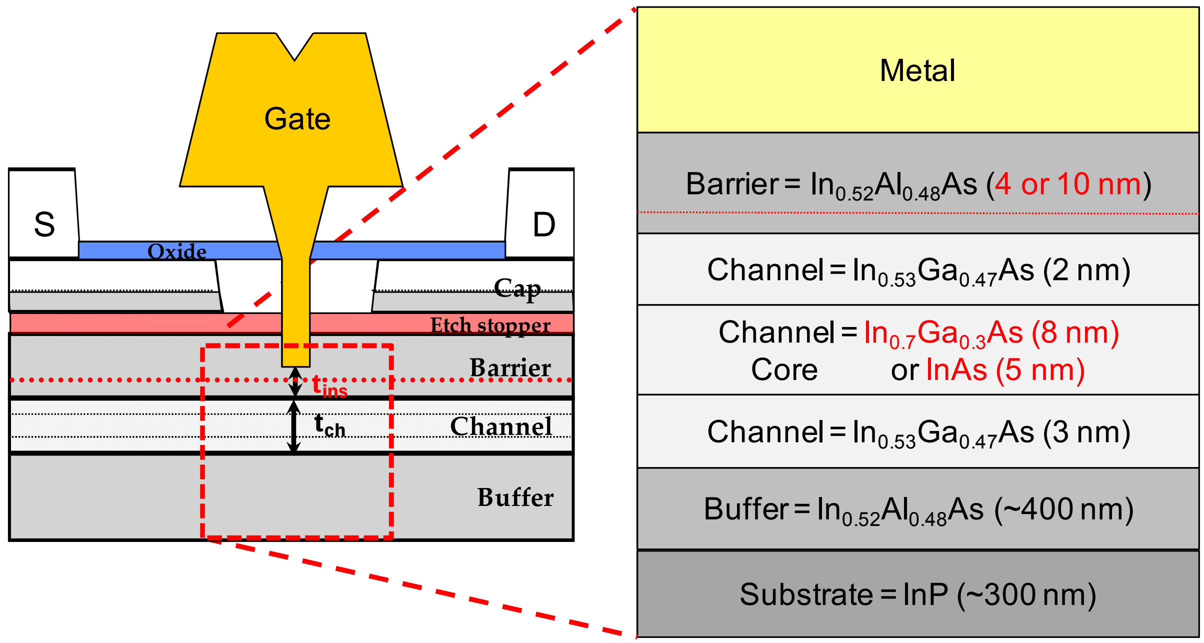
Gate Capacitance in III-V HEMTs

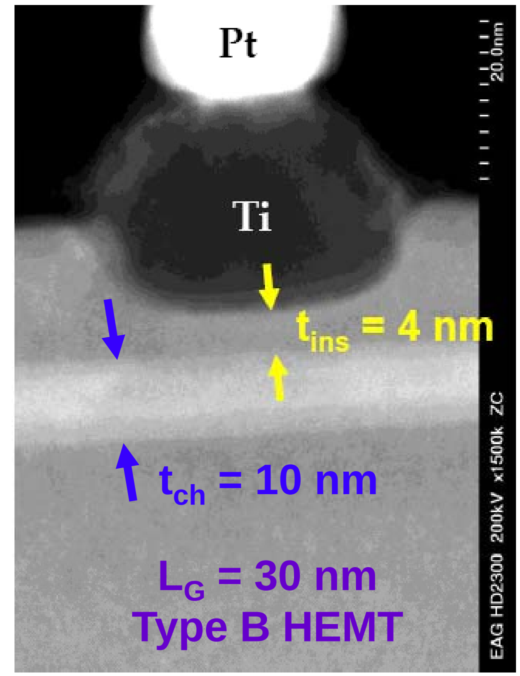
Goal: Experimental and theoretical study of C_G in III-V HEMTs



- Experimentally extract C_G for HEMTs with different t_{ins} and t_{ch}
- Build C_G model including DOS effect
- Project C_G and N_S of scaled down III-V FETs

Experimental HEMT Cross Section

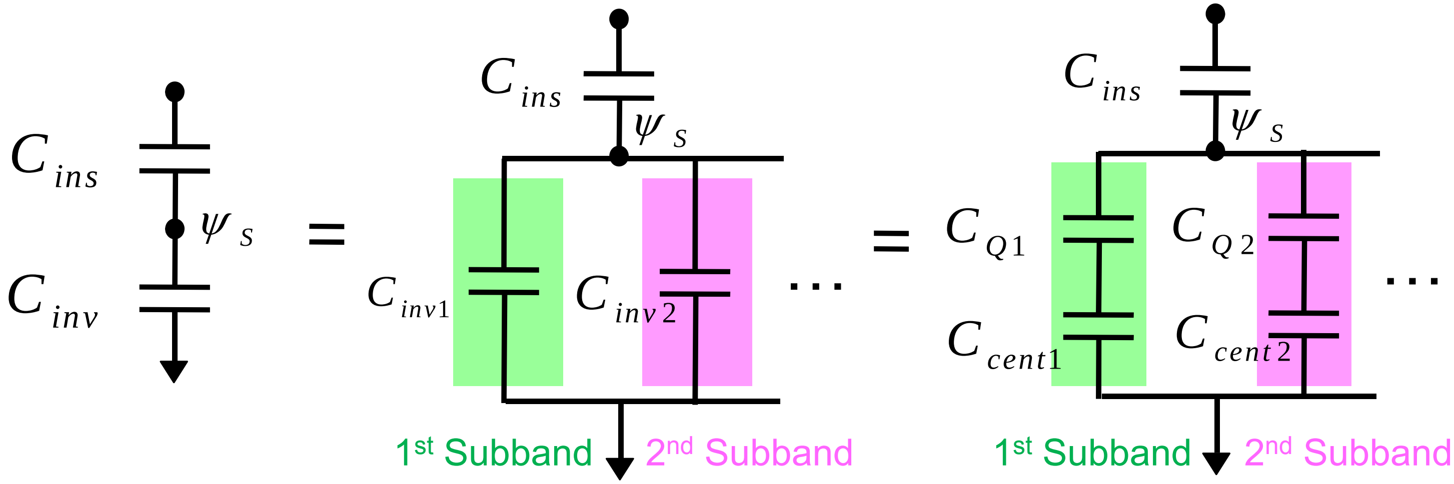




- Three different heterostructures explored :

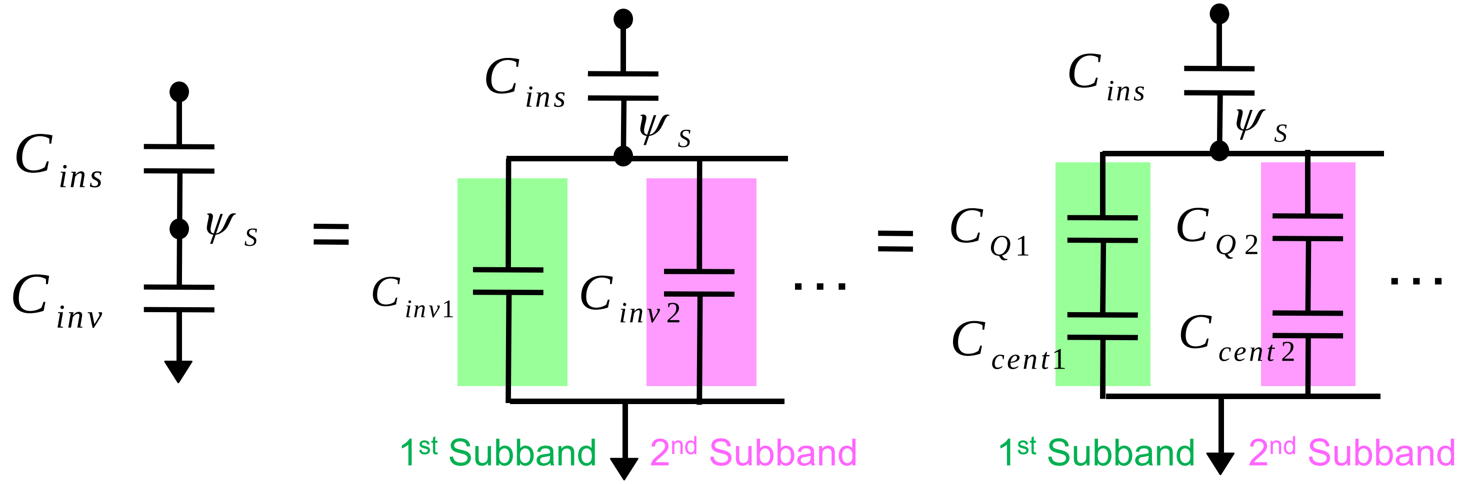
	t_{ins} (nm)	t_{ch} (nm)	Channel Core	Reference	L_G range (nm)
Type A	10	10	InAs (5 nm)	Kim, unpublished	40 ~ 100
Type B	4	10	InAs (5 nm)	Kim, IEDM 2008	30 ~ 200
Type C	4	13	$In_{0.7}Ga_{0.3}As$ (8 nm)	Kim, IEDM 2006	40 ~ 100

2. Gate Capacitance Model



$$C_{inv} = \frac{\partial(-Q_S)}{\partial \psi_S} = \sum_i \frac{1}{\dfrac{1}{C_{Q\_i}} + \dfrac{1}{C_{cent\_i}}}$$

2. Gate Capacitance Model



$$C_{inv} = \frac{\partial(-Q_S)}{\partial \psi_S} = \sum_i \frac{1}{\frac{1}{C_{Q\_i}} + \frac{1}{C_{cent\_i}}}$$

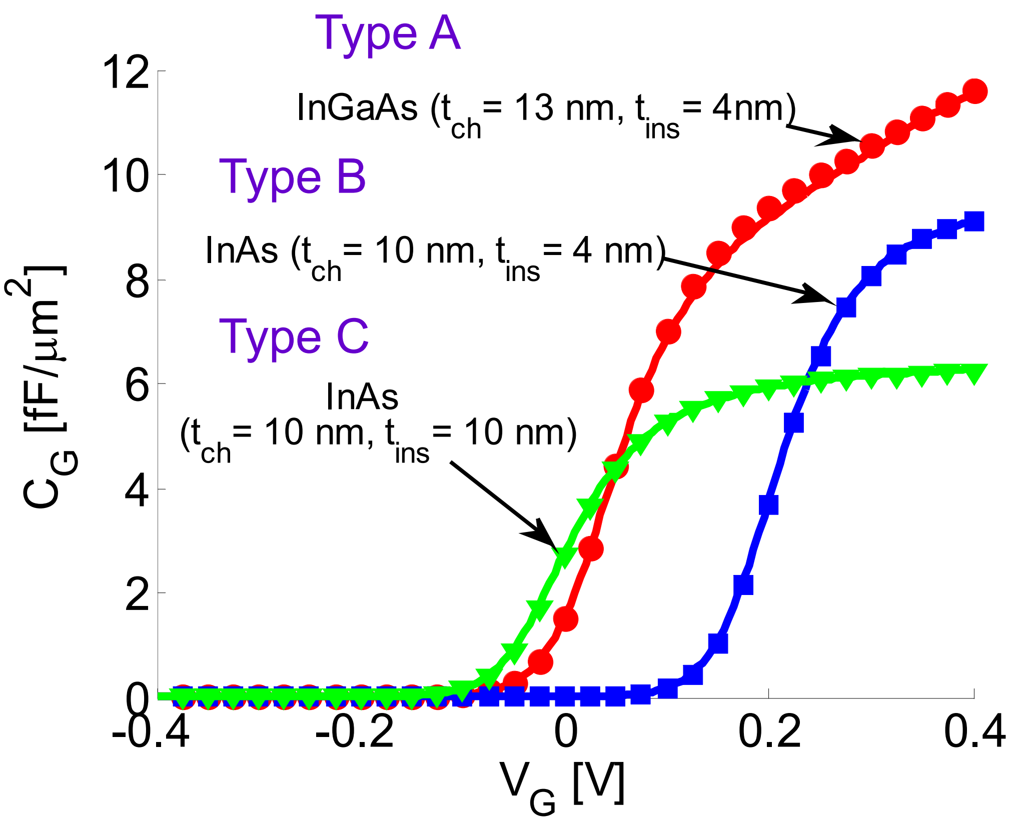
Quantum capacitance of subband *i* — 2D DOS

$$C_{Q\_i} = \frac{\frac{m_{\parallel}^{*} q^2}{\pi \hbar^2}}{1 + \exp(\frac{E_i - E_F}{kT})}$$

Centroid capacitance of subband *i*

$$C_{cent\_i} = C_{Q\_i} \cdot \frac{\partial(E_F - E_i)}{\partial(E_i - E_C)}$$

Verification of Physical Model



- Solid line :

Numerical simulation results from 1D Poisson-Schrodinger solver (Nextnano)

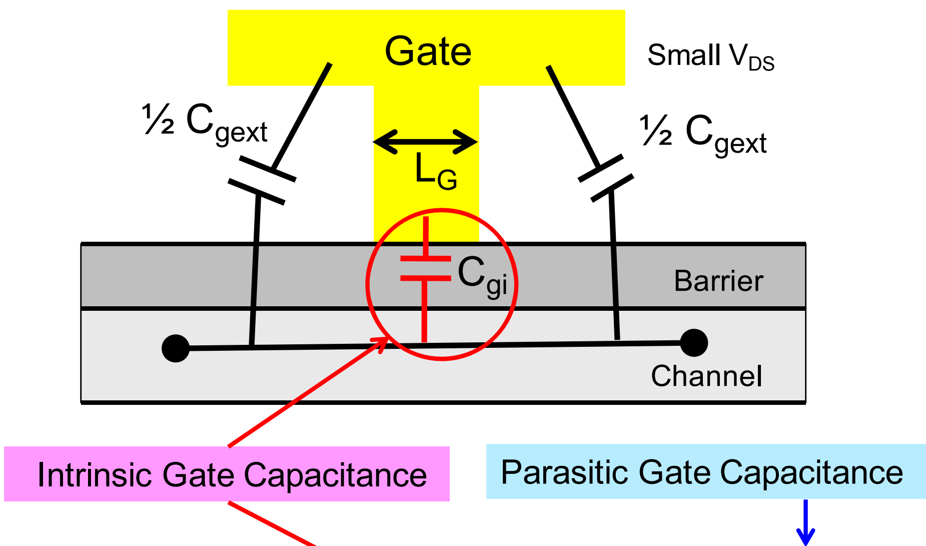
$$C_G = \frac{d(-Q_S)}{dV_G}$$

- Symbols :

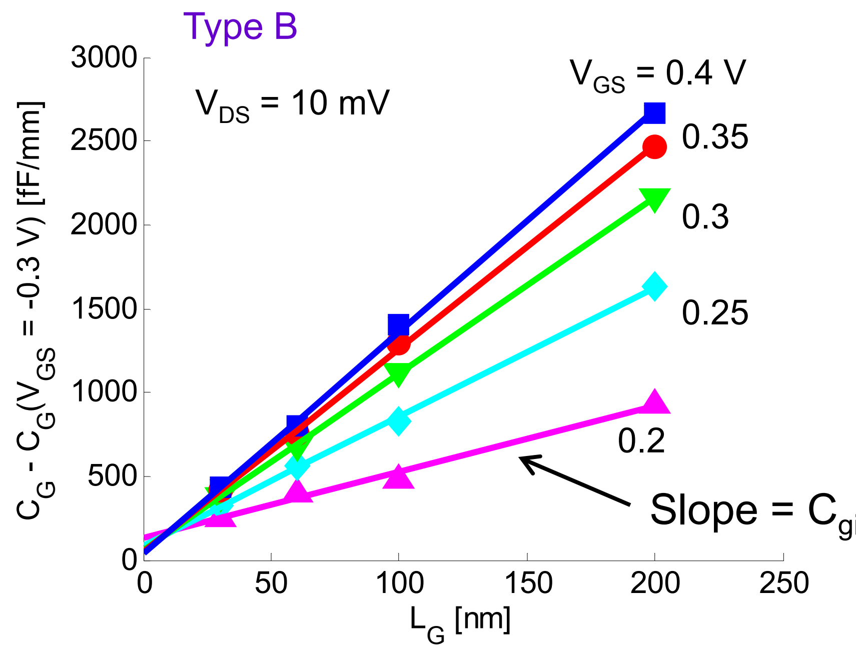
Physical model results (using Nextnano to extract E_i)

Good agreement between model and numerical simulations

3. Experimental C_G in a HEMT
obtained from S – parameter measurements

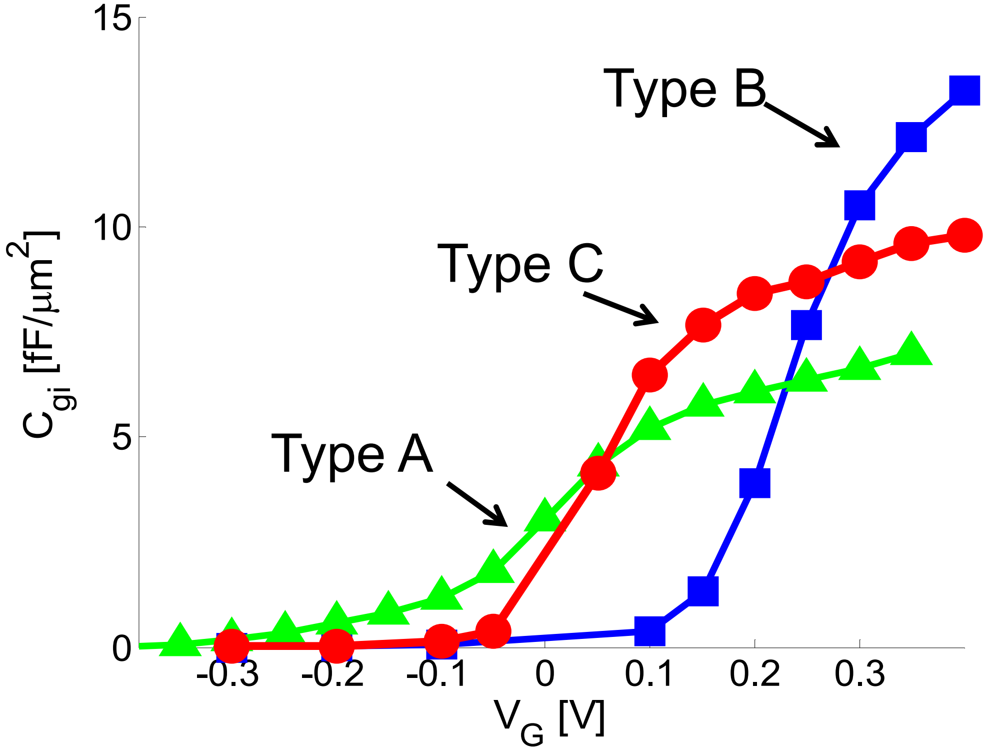


C_G (in fF/µm) = C_{gi} (in fF/µm^2) x L_G + C_{gext}



$$C_{gi} = \text{Slope of } C_G - C_G(V_G = -0.3V) \text{ with } L_G$$

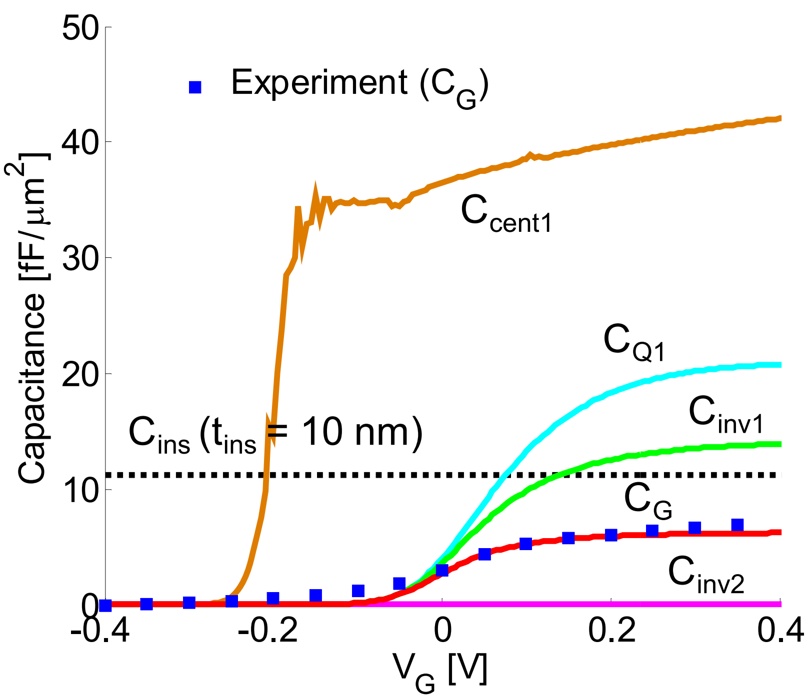
Experimental Intrinsic Gate Capacitance

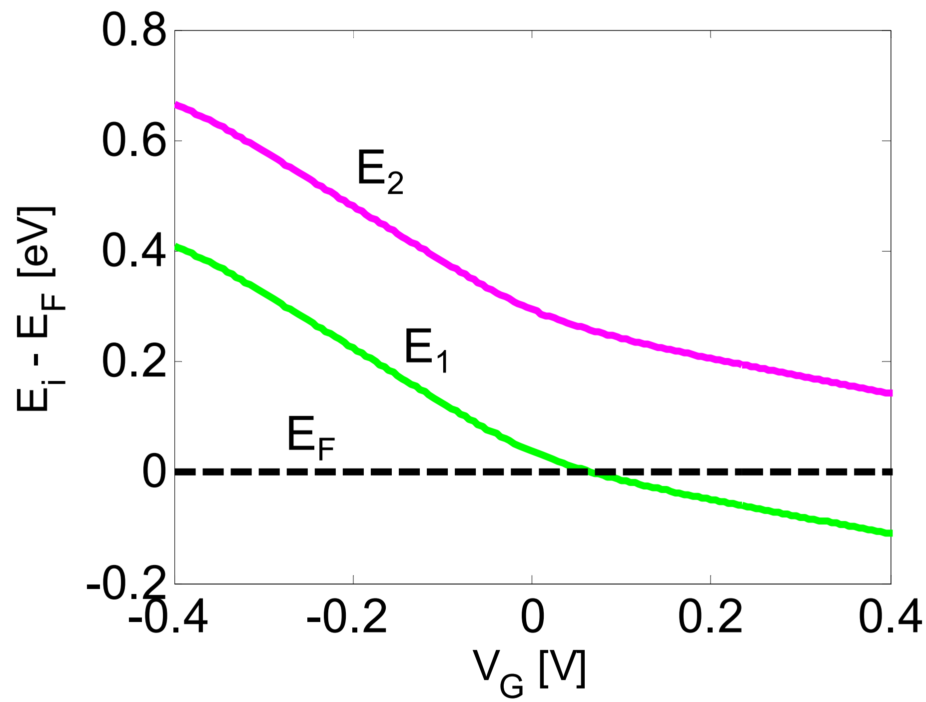


Comparison with physical model:

C_{ins} , C_Q , C_{cent} contribution to C_{gi}

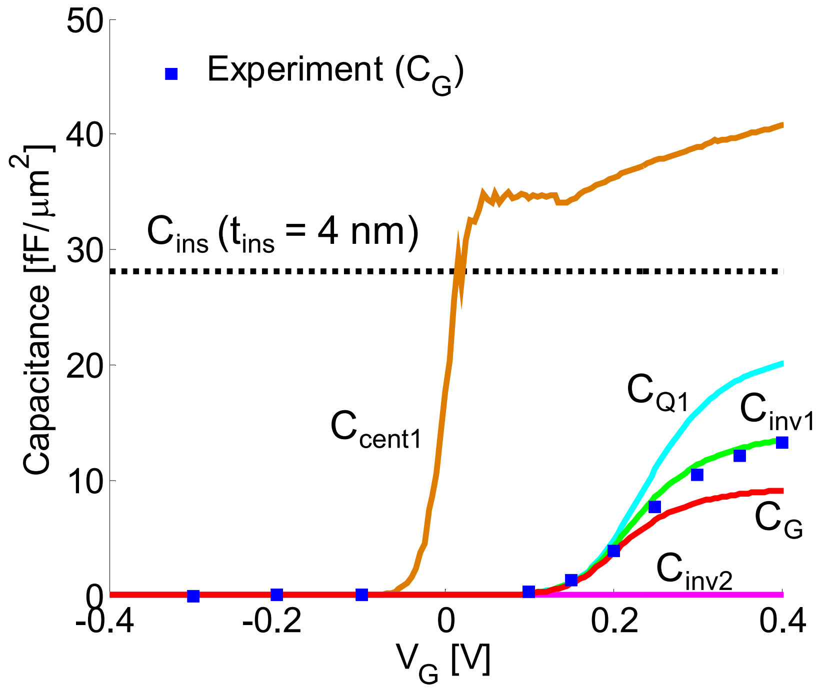
4. Comparison of measurements and model : Type A (InAs channel, t_{ch} = 10 nm, t_{ins} = 10 nm)

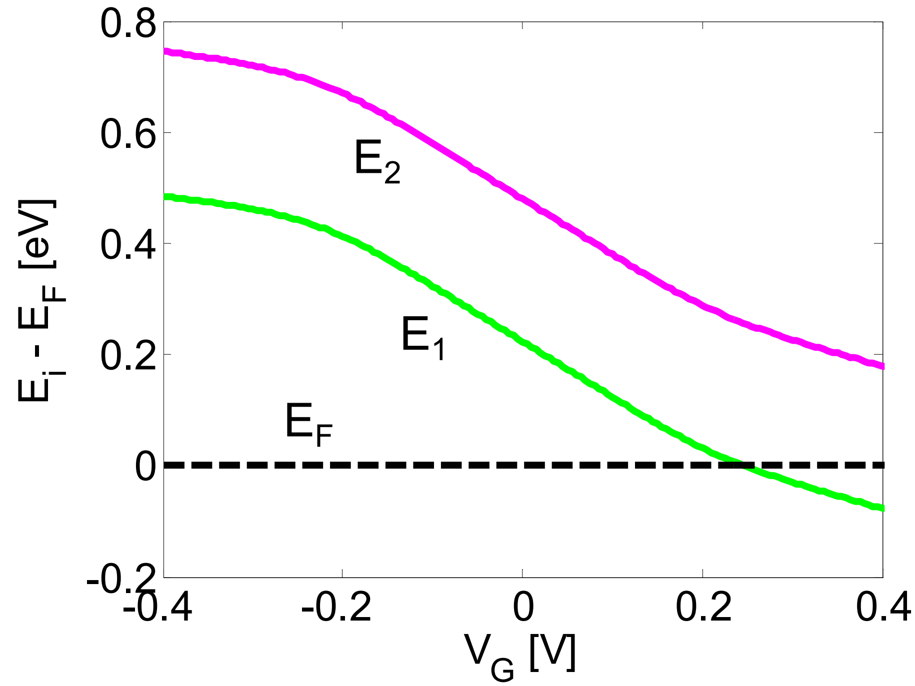




- Good agreement between measurements and model
- C_{ins} comparable to C_{inv} → C_G ~ 62% of C_{ins}
- Only 1st subband populated

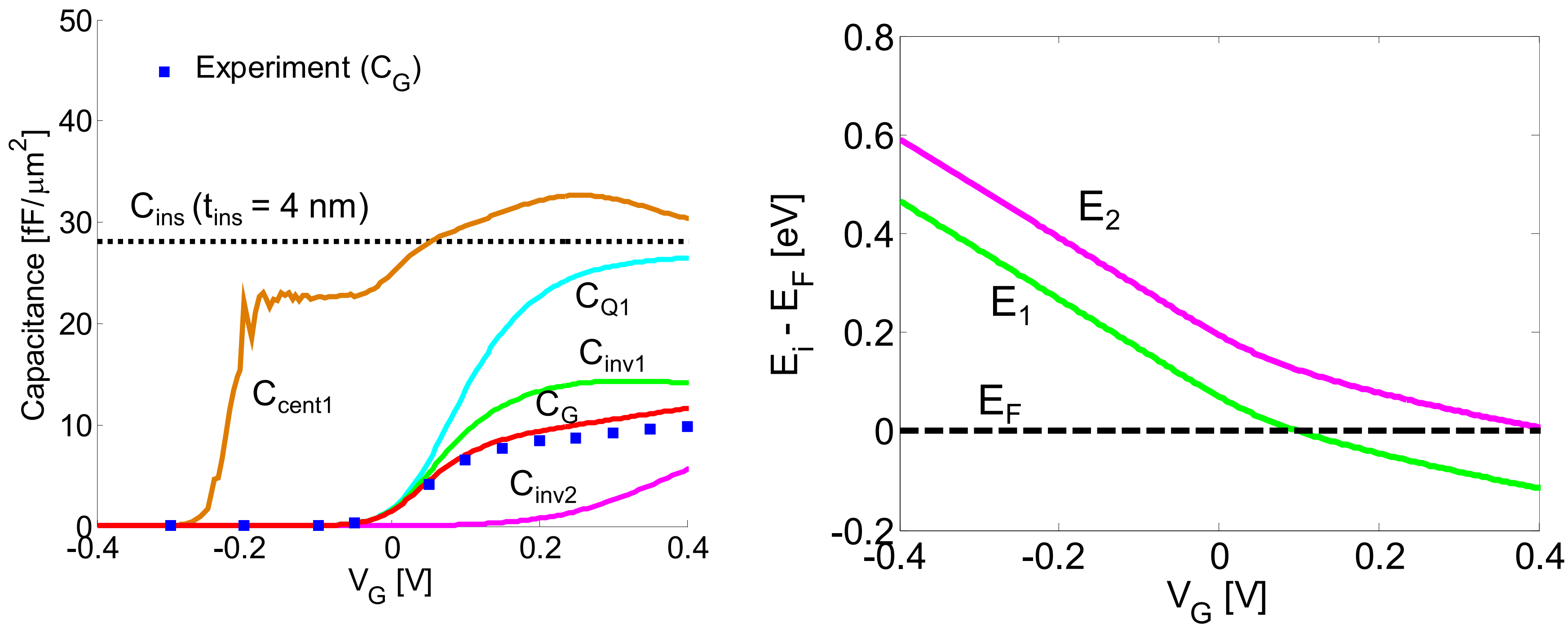
Comparison of measurements and model : Type B (InAs channel, t_{ch} = 10 nm, t_{ins} = 4 nm)





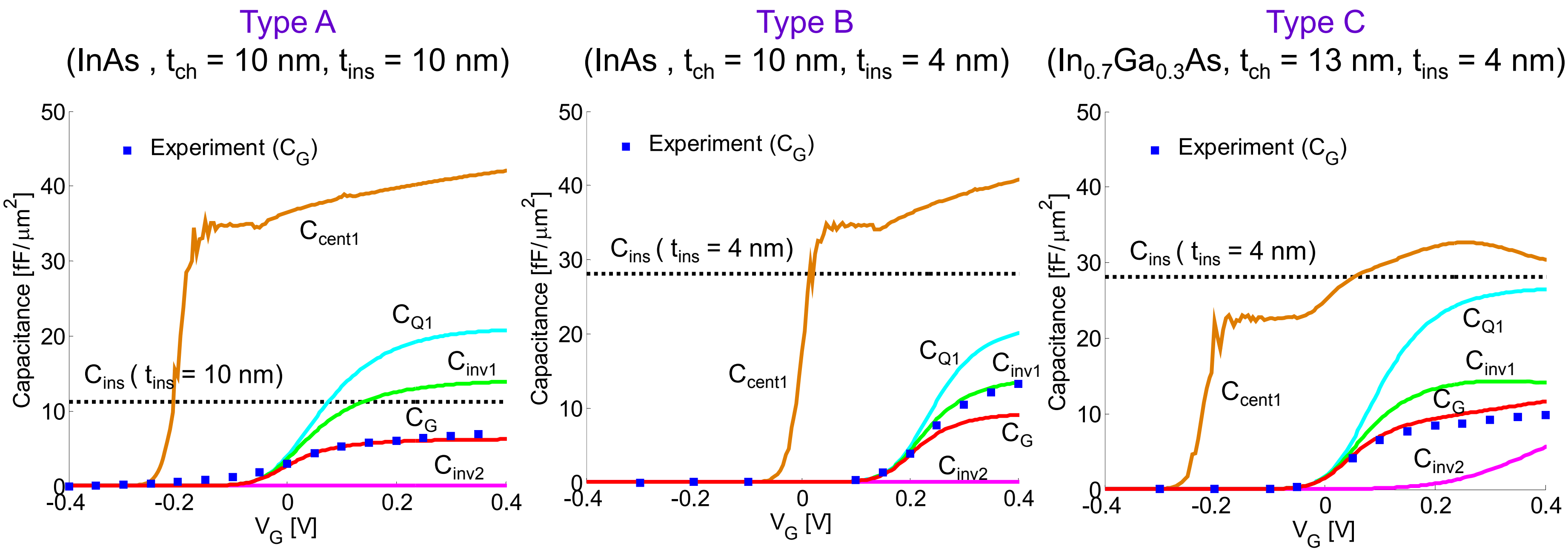
- Moderate agreement
- $C_{Q1} < C_{ins}$ → C_G limited by C_{Q1}: C_G ~ 47% of C_{ins}
- Only 1st subband populated

Comparison of measurements and model : Type C ($In_{0.7}Ga_{0.3}As$ channel, t_{ch} = 13 nm, t_{ins} = 4 nm)



- Good agreement
- Thicker channel: C_{cent1} comparable to C_{ins}
  → C_G ~ 35% of C_{ins}
- 1st subband dominant, 2nd subband minor

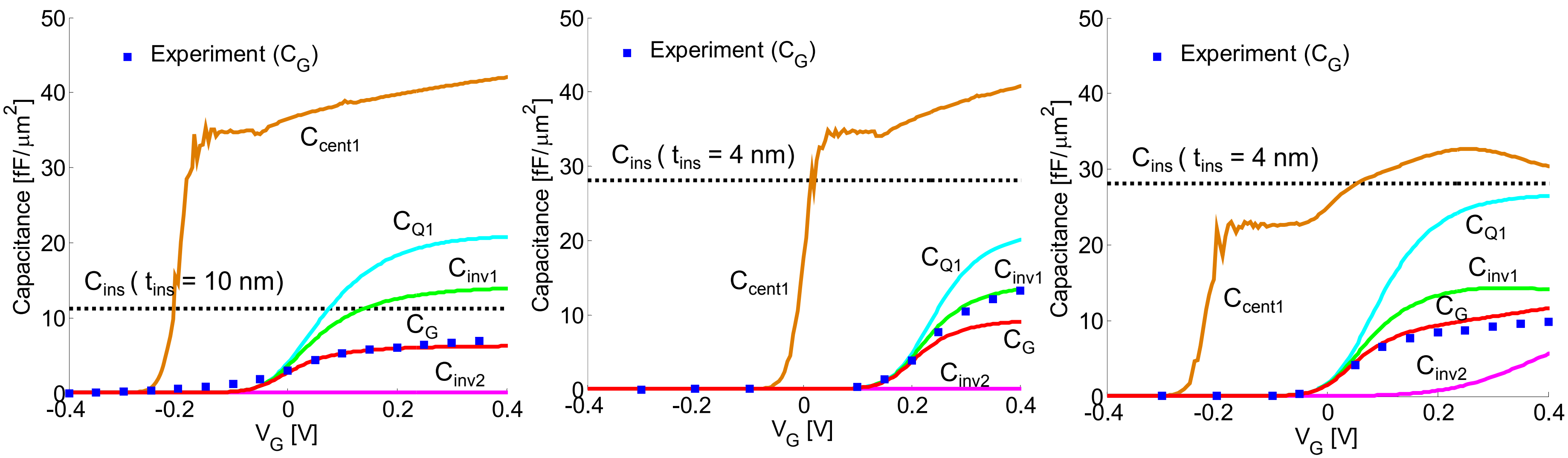
Summary of Key Findings



- Finite C_{inv} severely reduces C_G below C_{ins}
- C_{Q1} smallest in lower m* channel
- 1^{st} subband dominates
- C_{cent1} relevant: t_{ch} ↓ → C_{cent1} ↑

Summary of Key Findings

Type A (InAs , t_{ch} = 10 nm, t_{ins} = 10 nm) | Type B (InAs , t_{ch} = 10 nm, t_{ins} = 4 nm) | Type C ($In_{0.7}Ga_{0.3}As$, t_{ch} = 13 nm, t_{ins} = 4 nm)



- Finite C_{inv} severely reduces C_G below C_{ins}
- C_{Q1} smallest in lower m* channel
- 1[st] subband dominates
- C_{cent1} relevant: $t_{ch} \downarrow \rightarrow C_{cent1} \uparrow$

C_G (exp) > C_G (model) in Type B, Why?

→ C_{Q1} most relevant in Type B

Source of Discrepancy for C_G in Type B

1. Uncertainty in t_{ins}
   - ±0.5 nm error margin from TEM
2. Increase of in-plane effective mass ($m_{||}^*$)
   - Biaxial channel strain + Non-parabolicity + Quantization
     [Theory : Nag APL 1993; Experiment : Wiesner APL 1994]

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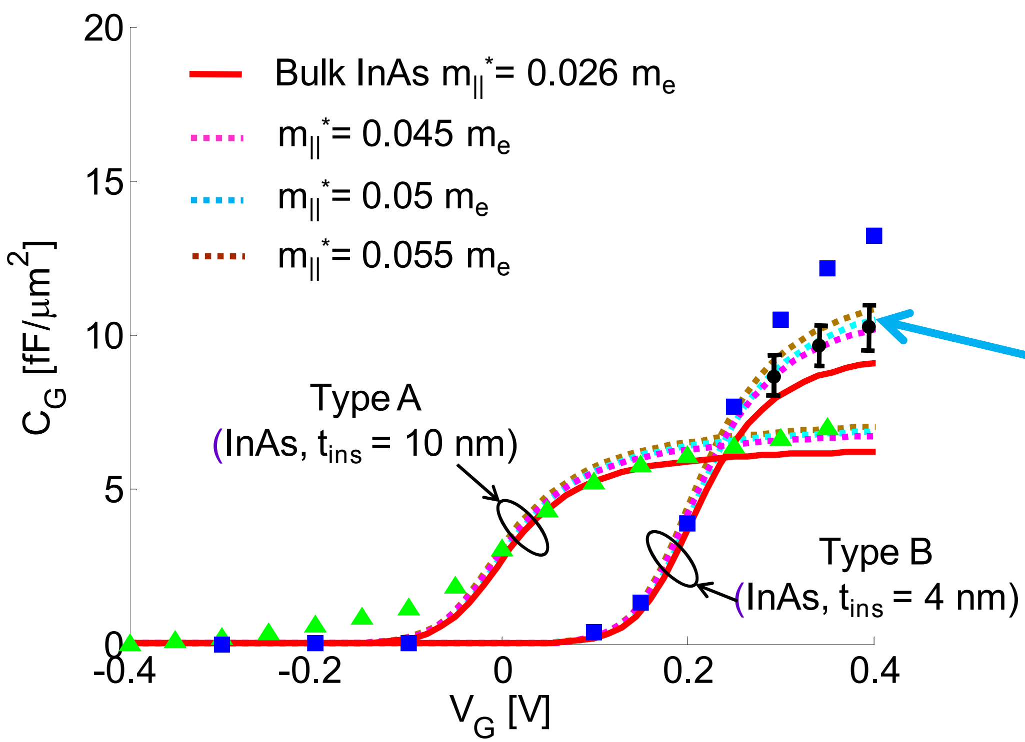

5 nm InAs thin channel
→ $m_{||}^*$ ≈ 0.05 m_e
suggested by N. Kharche at Purdue

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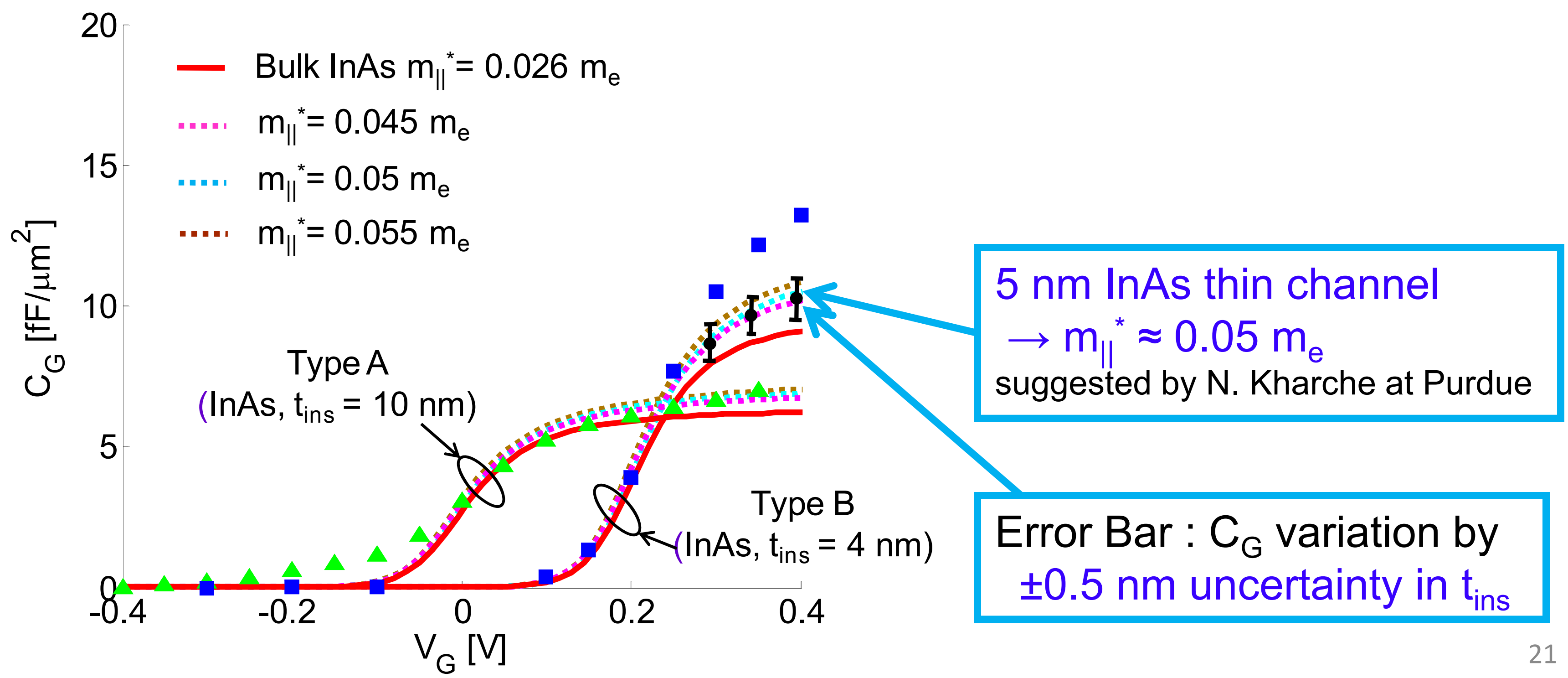

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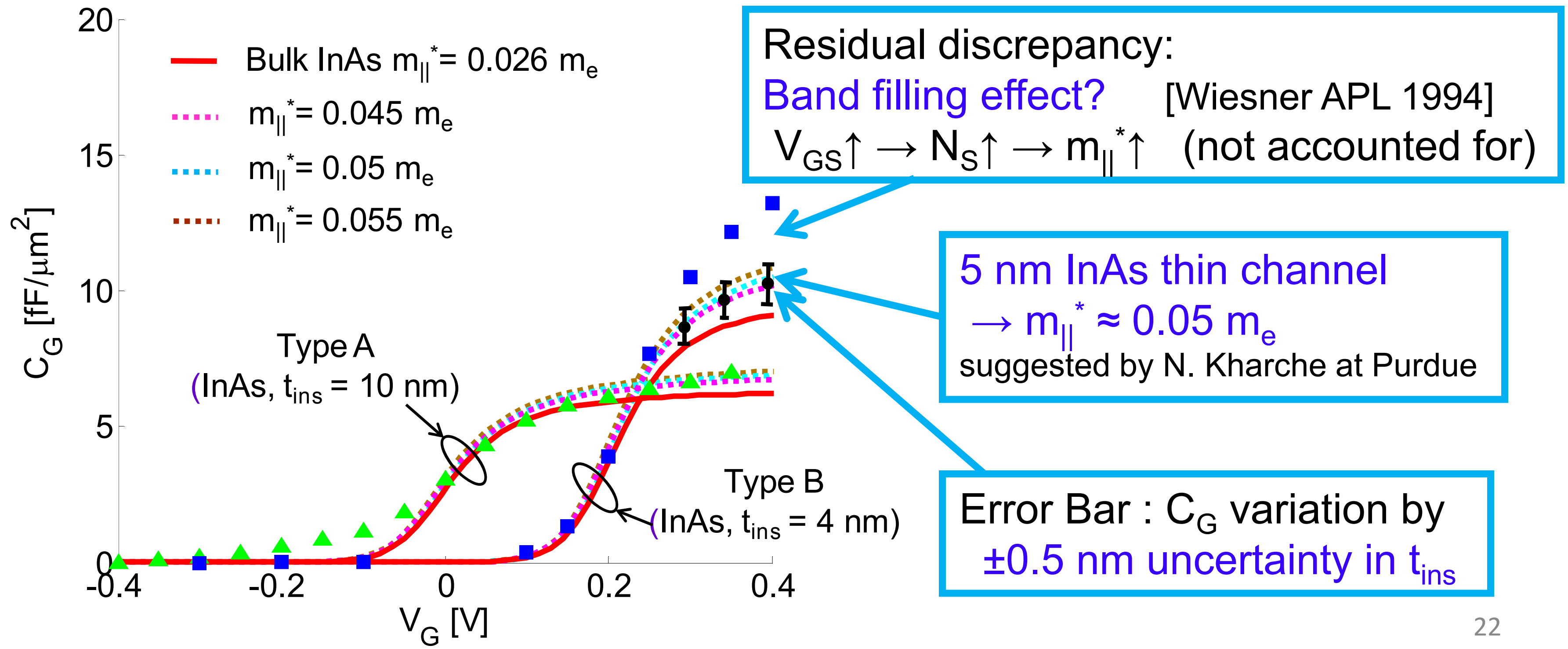
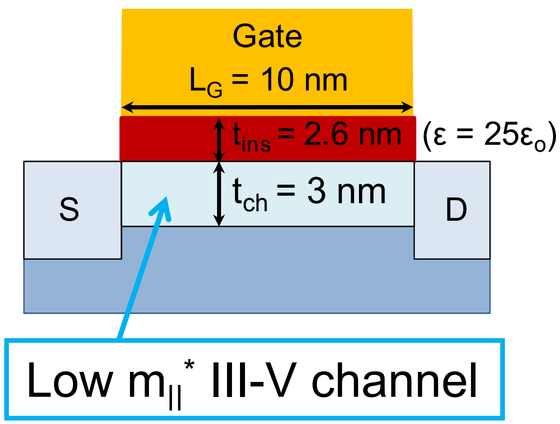
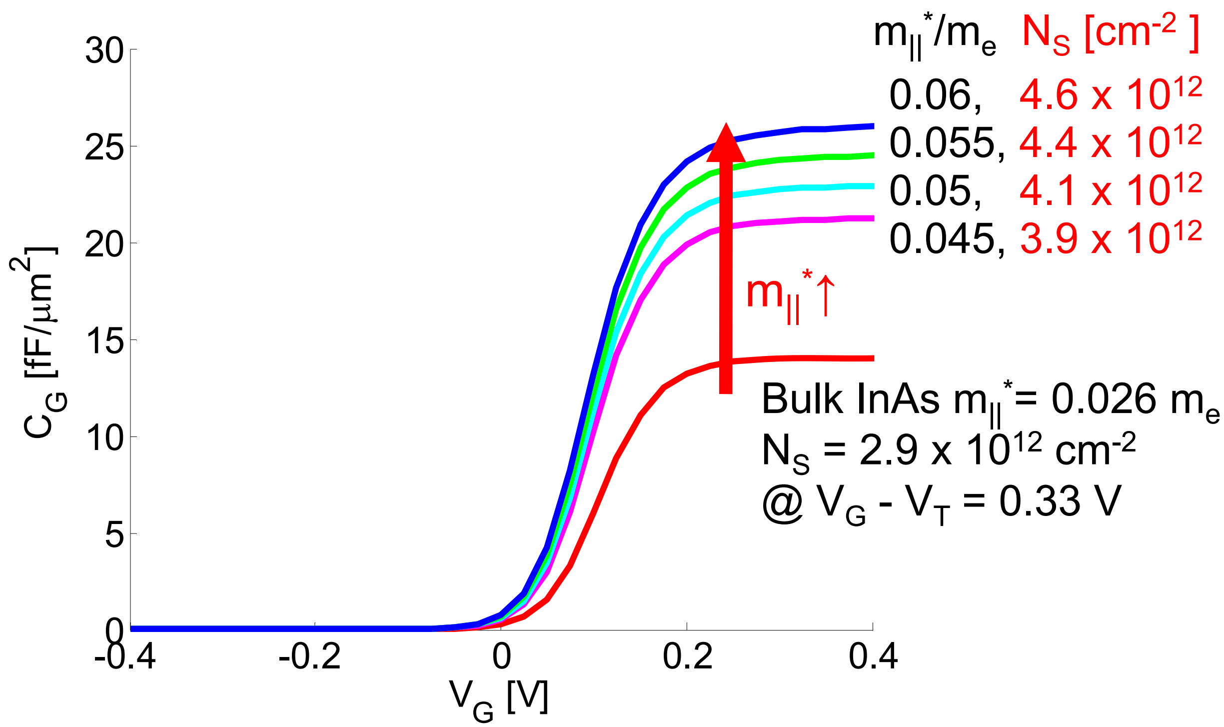


5. What does this mean for 10 nm III-V MOSFETs ?

Assume :
10 nm III-V MOSFETs



V_{DD} = 0.5 V



- $C_{Q1} << C_{ins}, C_{cent1}$ → C_{Q1} dominates in C_G

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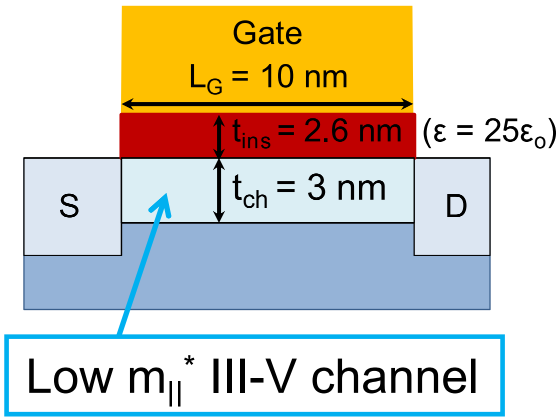

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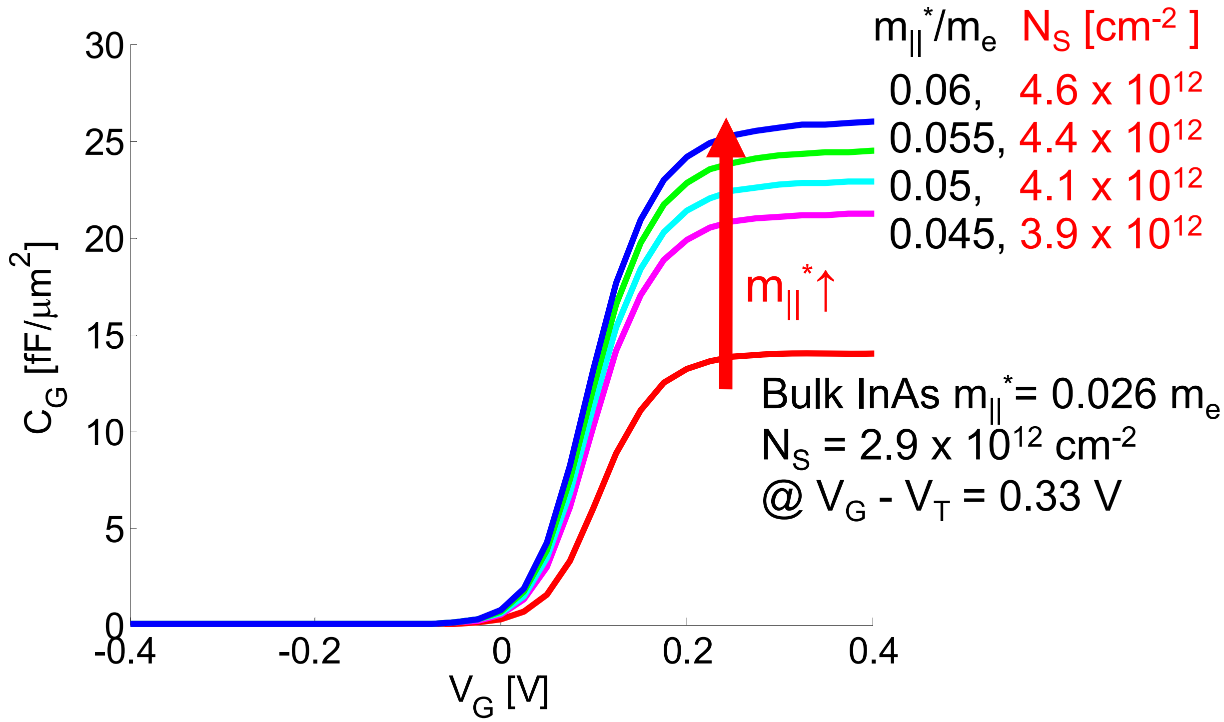

- $C_{Q1} << C_{ins}, C_{cent1}$ → C_{Q1} dominates in C_G

- Non-parabolicity + Quantization + In-grown biaxial strain
  → $m_{||}^*$ → C_{Q1}↑ → N_S ≈ mid 10^{12} cm^{-2} @ V_{DD} = 0.5 V

Conclusions

- Developed a simple quantitative model for C_G in III-V FETs
- Key findings :
  - Small C_Q in low $m_{||}^*$ channel limits C_G
  - Quantization + non-parabolicity + biaxial strain contribute to increase $m_{||}^*$
  - C_{cent} increased by using thin channel
- To improve C_G scaling
  - Thin channel designs increase C_Q and C_{cent}

  → N_S ~ mid 10^{12} cm^{-2} possible for 10 nm FET @ 0.5 V