Microelectronics Reliability 49 (2009) 1200–1206

Contents lists available at ScienceDirect

Microelectronics Reliability

journal homepage: www.elsevier.com/locate/microrel

Invited Paper

GaN HEMT reliability

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ARTICLE INFO

Article history:
Received 30 June 2009
Available online 30 July 2009

ABSTRACT

This paper reviews the experimental evidence behind a new failure mechanism recently identified in GaN high-electron mobility transistors subject to electrical stress. Under high voltage, it has been found that electrically active defects are generated in the AlGaN barrier or at its surface in the vicinity of the gate edge. These defects reduce the drain current, increase the parasitic resistance and provide a path for excess gate current. There is mounting evidence for the role of the inverse piezoelectric effect in introducing mechanical stress in the AlGaN barrier layer and eventually producing these defects. The key signature of this mechanism is a sudden and non-reversible increase in the gate leakage current of several orders of magnitude. This degradation mechanism is voltage driven and characterized by a critical voltage below which degradation does not occur. This hypothesis suggests several paths to enhance the electrical reliability of GaN HEMTs which are borne out by experiments.

1. Introduction

GaN HEMT technology looks increasingly attractive for a variety of high frequency and high-power applications. In spite of the impressive attributes of this technology and the outstanding performance values that have been demonstrated, its deployment in the field is currently being bottlenecked by its limited electrical reliability. There has been recent progress on this front. Mean-time-to-failure (MTTF) values of 10^7 h at a junction temperature of 150 °C have been recently reported for devices operating at 40 V [1]. In spite of these results and the fact that relatively high activation energies have also been reported (from 1.05 to 2 eV [1–7]), the meaning of this is not entirely clear. As the dominant mechanisms for electrical degradation are still under investigation, the degradation drivers are not known. It is therefore not understood what is it that temperature-accelerated experiments actually accelerate and whether these estimates of MTTF are of any relevance. With the current state of affairs, an acceptable certification that a certain technology can meet the reliability requirements of a given mission with any reasonable probability bound is not possible.

A solution to this necessarily demands attaining detailed physical understanding of the fundamental failure mechanisms behind electrical reliability. There have been recent studies about this but no consensus has emerged. As in III–V FETs, hot-electron-based mechanisms have been postulated in which hot electrons get trapped in the AlGaN, buffer, at the SiN/AlGaN interface or inside the SiN, or in which hot electrons contribute to trap formation at any of these locations [8–11]. Although hot electrons seem to play a role in device degradation, the relative relevance of this is unclear. To our knowledge, the key signature of hot-electron degradation has not been observed. That is a degradation that is exponentially proportional to $1/(V_{DS} - V_{DSsat})$ or correlating with gate current with a similar signature, as observed in Si MOSFETs, GaAs HEMTs and InP HEMTs [12–15].

In contrast, there is mounting evidence behind a reliability mechanism that also involves defect formation but through the inverse piezoelectric effect [16,17]. This paper summarizes the experimental evidence behind this hypothesis and its implications for device design.

2. High-voltage induced defect formation through the inverse piezoelectric effect

GaN and AlGaN are strongly piezoelectric materials. In response to high voltages, large stresses are induced inside these materials. By their very nature, in an AlGaN/GaN HEMT under high voltage operation, a large electric field appears under the gate edge across the barrier. This can result in very large mechanical stress concentrated in a very small region of the AlGaN barrier (Fig. 1). To make matters worse, due to their lattice mismatch, AlGaN on GaN is typically under substantial tensile strain and therefore stores a sizable amount of elastic energy at rest. Under electrical stress, the elastic energy in the high-field region increases on top of this. If the elastic energy exceeds a critical value, crystallographic defects are formed. These defects are electrically active and affect the device characteristics in a profound way.

There are several interesting aspects of a degradation mechanism of this kind, many of which can be tested by experiments:

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doi:10.1016/j.microrel.2009.07.003

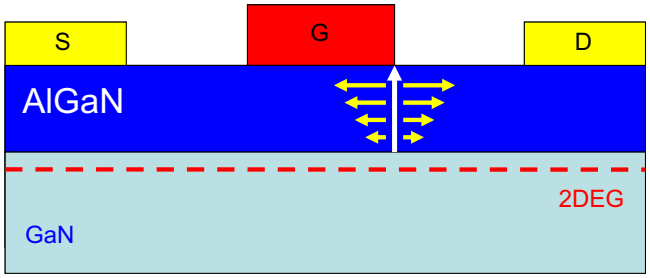

Fig. 1. Sketch of GaN HEMT under electrical stress with a high V_{DG}. A high-field appears under the gate edge on the drain side of the device (white vertical arrow) which results in large lateral tensile stress in the same region (horizontal arrows).

1. This should be an electric field driven mechanism as it is the electric field that produces mechanical stress through the inverse piezoelectric effect. In particular, the vertical electric field through the AlGaN barrier layer plays the key role while the horizontal electrical field should not contribute. This is because the horizontal electric field does not increase the elastic energy to the first order [18].
2. There should be a critical voltage beyond which degradation suddenly happens. This is because this type of degradation is unlikely to take place before the elastic energy in the AlGaN layer reaches its critical value. For example, in the epitaxial growth of strained heterostructures, beyond a certain thickness, the elastic energy relaxes through the formation of crystalline defects [19,20].
3. Current by itself should play no role, except for indirect heating of the lattice which is likely to exacerbate the problem.
4. The electrical defects should appear in the high-field region of the device which is on the drain side under normal operating conditions.
5. For transistors with short gate lengths, the gate length and the gate-to-source voltage (under normal operating conditions) should have an impact on the critical voltage as they affect the electric field profile on the drain side of the device.
6. The application of mechanical strain should be able to reduce or increase the critical voltage depending on sign as it increases the elastic energy in the AlGaN layer.
7. The composition and thickness of the AlGaN layer as well as the material quality should affect device reliability as it changes the initial level of elastic energy in the AlGaN. In fact, anything that affects the initial elastic energy in the AlGaN will affect this type of degradation. Other examples are the strain and composition of the buffer layer and the presence of an AlN layer in the barrier.
8. Device designs that mitigate the electric field should also improve the reliability due to this mechanism. Examples are field plates, slanted gates, and gate corner rounding.

In the next section, we present a collection of experiments that is consistent with these expectations. Some of these experiments cannot be explained by a hot-electron driven mechanism.

3. Experimental

Our work has been carried out on prototype industrial devices. The experimental results described here have been observed in many devices from different wafers from different runs, from three different companies. As the technology has matured, the reliability has generally improved. The specific pattern of degradation, while shifting to higher voltages, for the most part has not changed. All the observations that we report here are statistically significant.

As an exponent of the types of technologies that we have examined, a typical device with a 0.25 μm gate length, 4 × 100 μm gate width and a source to drain spacing of 4 μm features a current-gain cut-off frequency f_T of around 40 GHz and I_{Dmax} of about 1.2 A/mm. With the device biased at 40 V, the output power is about 9.8 W/mm and PAE is 55% at 10 GHz [3]. The devices used in reliability studies typically have a gate width of 2 × 25 μm.

For this work, we designed what we term a "Reliability test chip." This is a collection of test structures that we have accumulated over the years and that are packed together in a small chip (about 10 mm^2). Our current design of the reliability test chip includes DC and microwave transistors with different designs, dimensions and gate orientations. Most of these devices are fully testable before the via process is completed. We also have other test structures such as TLM, side-gate TLM, Fat-FETs, and Hall patterns. This test chip must be customized to some extent to the device design and process used by our industrial partners and it has to be designed following their design rules.

Our experiments typically involve stressing the device under DC for a certain length of time. At frequent intervals during the tests, the stress is halted and the device is characterized through a benign characterization suite with two components:

- There is a *coarse* characterization that is performed by measuring a number of basic device parameters such as V_T, I_{Dmax}, R_S, R_D, and I_{Goff}. This is typically done every 1–2 min throughout the experiment. These parameters have been selected to provide a view of the impact of stress in the different regions of the device. The bias conditions for these parameters need to be customized to some extent for each device design.
- There is also a *fine* characterization that to this list adds complete *I–V* characteristics over a certain range: output, transfer, gate, subthreshold and kink. This typically runs at the beginning and at the end of an experiment and about every 20 min or at other significant times during an experiment.

A key aspect of this benign characterization suite is that it is *fast*. The coarse characterization typically takes 15 s of testing time while the fine characterization takes about 1 min of testing time. Another essential aspect of this characterization suite is that it is *benign*. This means that characterization should introduce negligible change in the device characteristics. We ascertain this by executing the complete characterization suite 100 times and demanding that no single electrical parameter that is extracted changes more than 2% during this experiment. This has meant that we cannot evaluate the breakdown voltage of the device since this is a very aggressive measurement that significantly affects the device.

Our electrical reliability evaluation typically involves *step-stress experiments*. This means that the stress is increased in a step manner over time. This is a highly productive approach that allows us to observe degradation in virtually every single experiment that we perform and it also leads to evaluating a number of conditions in a single device. We also perform *stress-recovery* experiments in which the stress is applied for a while and then the device is allowed to rest for a certain period of time. These types of experiments are useful in situations of prominent trapping, as is the case in GaN HEMTs. A mix of these two experiments is a *step-stress-recovery experiment* in which stress is applied, then the device is allowed to rest, and then the stress is resumed at a higher level. This is useful when evaluating trap formation as a result of the stress.

Our experiments are of a DC electrical stress nature. In this, we use different bias conditions. Most relevant for many applications is the *high-power state* in which the device is biased at high current and high voltage. Due to self-heating, the device typically gets very

hot during this experiment. The *ON-state* is also relevant in some cases. In this, the device is biased in the saturation regime at high current but low voltage. The *OFF-state* is characterized by very small current and high voltage. The $V_{DS} = 0$ *state*, as its name suggests, applies a large negative voltage across the gate but the source and drain are shorted together. The advantage of these last two types of stress is that there is negligible power dissipation and therefore self-heating and the complications of evaluating the junction temperature are mitigated.

These four bias conditions establish a rather different electric field distribution in the device. In the ON-state the fields are small. In the high power and OFF-states, there is a high lateral field in the channel and high vertical field through the barrier. In the $V_{DS} = 0$ state, there are high vertical fields through the barrier but small fields in the channel. From the point of view of hot electron production, these four conditions are also quite different. Since hot electron production is exponentially proportional to the field and linearly on the current, only the high-power state generates large amounts of hot electrons. Depending on the current level, the OFF-state can also generate hot electrons at high-fields.

Our standard experiments are performed in the dark, under N_2 and at room temperature.

4. Results

Fig. 2 shows the change in *I–V* characteristics of a typical GaN HEMT after a $V_{DS} = 0$ step-stress experiment. In this experiment, V_{GS} is stepped from −10 to −50 V in 1 V steps every 1 min. It is evident from the output and transfer characteristics that electrical stress has degraded the current driving ability of the device and has increased its ON resistance. From the subthreshold characteristics we see a marked increase in the off-state current which clearly arises from a very large increase in the gate current, particularly in reverse bias. From temperature dependent studies of the gate current, we find that the activation energy of the reverse bias current has markedly decreased to virtually zero though it does not change in forward bias (Fig. 3) [21].

Figs. 4 and 5 give more details of the experiment in Fig. 2. Fig. 4 shows the evolution of the stress voltage and current as a function of time and Fig. 5 graphs some of the device parameters as a function of $V_{DGstress} = V_{SGstress}$. Here, I_{Dmax} is defined as the drain current at $V_{GS} = 2$ and $V_{DS} = 5$ V, and I_{Goff} is defined as the gate current at $V_{GS} = -5$ and $V_{DS} = 0.1$ V.

For moderate voltages, there is very little change in the bias or in any of the parameters of the device. Suddenly, over a narrow range of voltages around $V_{GS} = V_{GD} = -21$ V, the gate current increases by nearly three orders of magnitude and I_{Dmax}, R_S and R_D start to degrade. We have observed this peculiar signature for sudden degradation in nearly every device that we have studied under these conditions across many wafers, runs and manufacturers provided that the stress voltage is high enough. This is what we believe is the unique signature of the defect formation mechanism through the inverse piezoelectric effect [16,17].

It is important to realize that the bias current that flows through the device during the stress (Fig. 4) is initially small (~0.3 mA/mm) and there is therefore negligible self-heating or hot-electron production. Around V_{crit}, this current increases, but by the time I_{Goff} has increased by two orders of magnitude $I_{Gstress}$ is still below

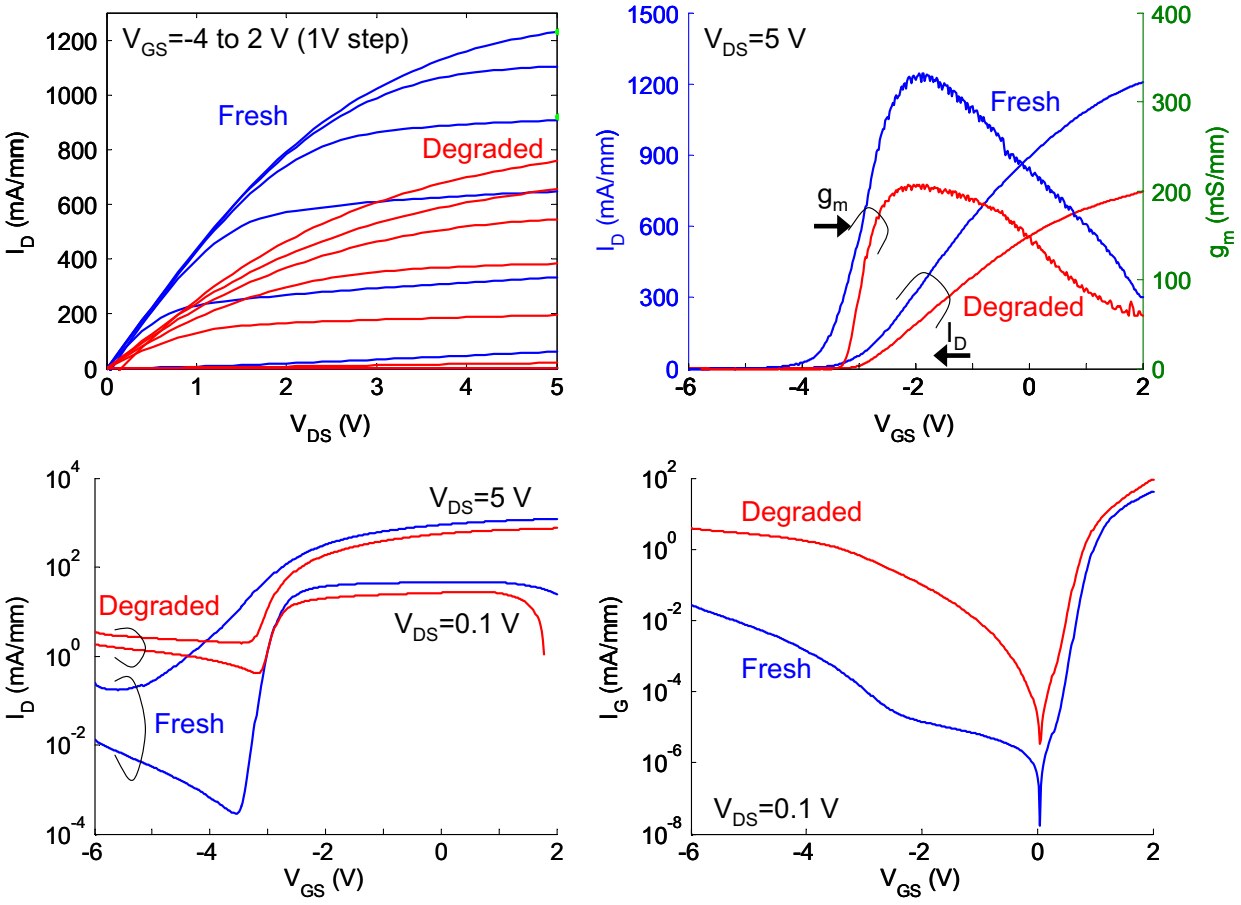

Fig. 2. Change in device characteristics before and after a step-stress experiment in the $V_{DS} = 0$ state. V_{GS} was stepped from −10 to −50 V in 1 V steps (1 min per step). From the upper-left corner (clockwise): output characteristics, transfer characteristics, gate current characteristics and subthreshold characteristics.

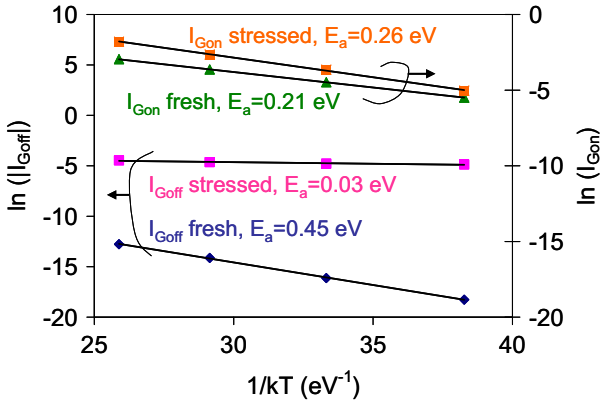

Fig. 3. Temperature dependence of gate current in reverse bias (I_{Goff}) and forward bias (I_{Gon}). I_{Gon} is the forward bias gate current at $V_{DS} = 0.1$ and $V_{GS} = 0.5$ V.

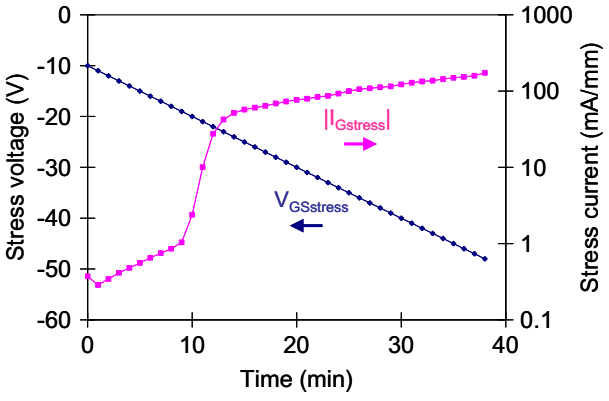

Fig. 4. Stress voltage and stress gate current $I_{Gstress}$ in the $V_{DS} = 0$ step-stress experiment of Fig. 2.

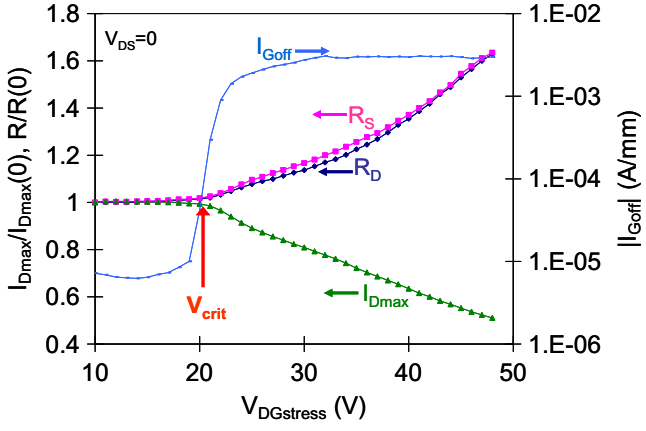

Fig. 5. Change in I_{Dmax}, R_D, R_S, and I_{Goff} in the $V_{DS} = 0$ step-stress experiment of Figs. 2 and 4.

10 mA/mm. Therefore, it is difficult to attribute the sudden degradation that takes place around V_{crit} to hot-electron production or self-heating.

Under the $V_{DS} = 0$ condition, the stress in the device is symmetric and, as seen in Fig. 5, the degradation in R_S and R_D is nearly identical. Additional insights can be obtained from OFF-state experiments where the high-field region appears only on the drain side of the device.

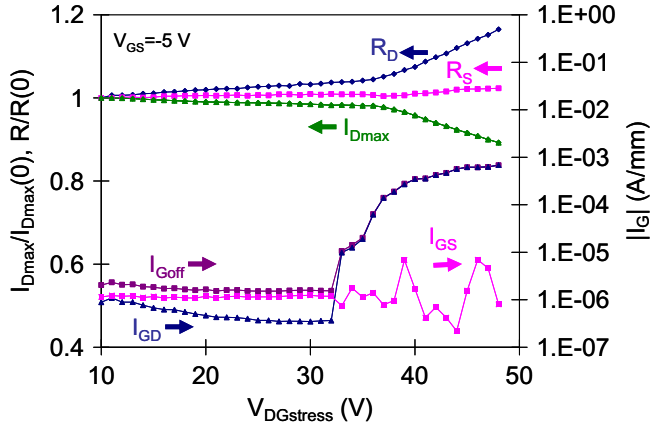

Fig. 6. Change in I_{Dmax}, R_D, R_S, and I_{Goff} in an OFF-state step-stress experiment ($V_{GS} = -5$ V). The two components of I_{Goff} (I_{GD} and I_{GS}) are also plotted.

Fig. 6 summarizes the result of a step-stress experiment in the OFF-state. In this experiment, V_{DS} was stepped from 5 to 45 V while V_{GS} was kept constant at −5 V. It can be seen that I_{Dmax} and R_D start to degrade beyond a critical voltage around $V_{DG} = 35$ V. At around the same voltage, I_{Goff} sharply increases. The fact that this is significantly higher than the value of V_{crit} observed under $V_{DS} = 0$ stress is significant and is addressed below. In this figure, we have also plotted the two components of I_{Goff}: current from gate-to-drain, I_{GD}, and from gate-to-source, I_{GS} (this current is obtained as the difference between I_{Goff} and I_{GD} and is therefore quite noisy). Then it is the gate-to-drain component of I_{Goff} that is degraded. This is consistent with the increase in R_D but not in R_S, which indicate that the drain side of the device is degraded but the source side remains almost intact.

We concluded from the data in Fig. 5 that the stress current had no relevance for the changes that occur in the device at V_{crit}. One can confirm this by performing experiments in the high-power state for different drain current levels on neighboring devices. Fig. 7 shows the result of one such experiment which clearly shows that increasing the stress drain current not only does not enhance degradation, it actually mitigates it! Increasing $I_{Dstress}$ increases the critical voltage [17]. This confirms that current by itself is not an accelerating factor of the type of degradation that is taking place at V_{crit}. This experiment is clearly inconsistent with a hot-electron type hypothesis for this degradation mechanism.

The results in Fig. 7 make sense when one examines the role of V_{GS} in degradation. Fig. 8 shows the impact of V_{GS} on OFF-state

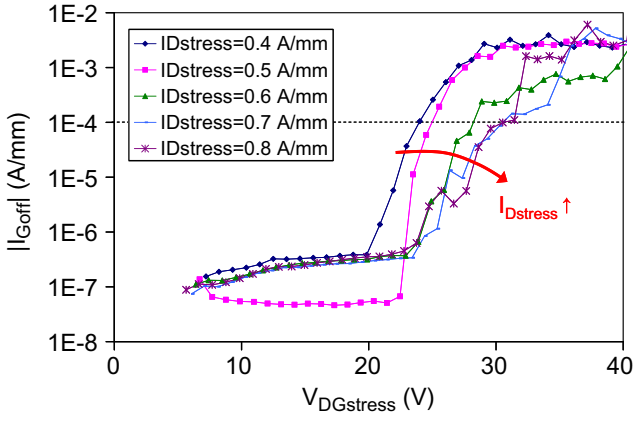

Fig. 7. Change in I_{Goff} in step-stress experiments in the high-power state for different values of the stress drain current.

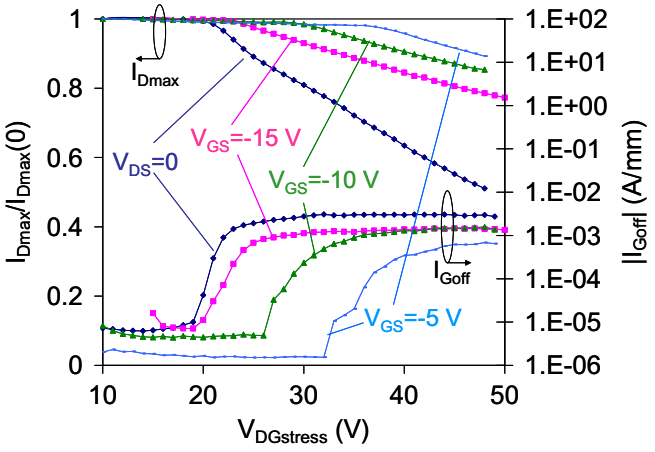

Fig. 8. Change in I_{Dmax} and I_{Goff} in step-stress experiments in the OFF-state for different values of V_{GS}. A V_{DS} = 0 step-stress experiment is also shown. As $|V_{GS}|$ decreases, the critical voltage increases.

step-stress experiments [17]. The graph also includes a V_{DS} = 0 stress experiment. All of them have been performed on neighboring devices. It is very clear from these data that decreasing V_{GS} in absolute terms increases V_{crit} in a very marked way. In other words, decreasing the field on the source side mitigates the degradation on the drain side. This is understandable in the context of an inverse piezoelectric effect driven mechanism. In short gate length devices, V_{GS} is known to affect the field on the drain side of the device [22]. A high absolute value of V_{GS} does actually increase the field on the drain side somehow and in this way enhances mechanical stress and reduces the critical voltage for degradation. The same effect is at play when examining the gate length dependence of V_{crit} in V_{DS} = 0 step-stress experiments [16]. We have found that the critical voltage increases as the gate length increases (Fig. 9). This is again due to the interaction of the V_{GS} and V_{GD} on the fields on the source side and the drain side of the device.

An important aspect of this degradation mechanism is that degraded devices past V_{crit} exhibit prominent trapping behavior [16,23,24]. An example is shown in Fig. 10 which shows the result of a V_{DS} = 0 stress-recovery experiment performed at 40 V. In its virgin state, this device shows little trapping. In the early stages of this experiment at the beginning of the very first pulse, the device goes through the critical transition and degrades. There is then a rapid rise of I_G and a drop in I_{Dmax}. When the stress is halted, I_{Dmax} recovers significantly with a time constant of the order of several

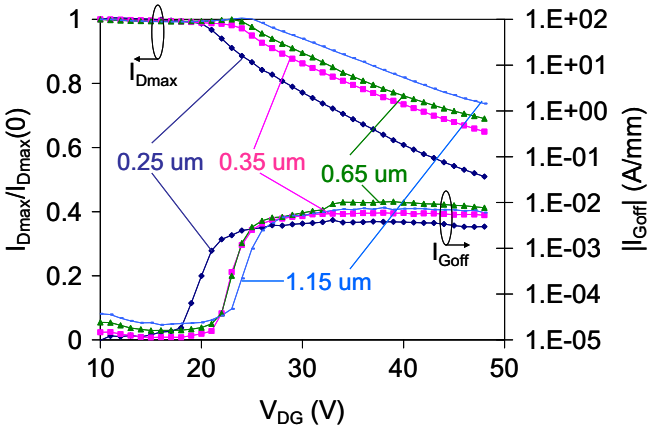

Fig. 9. Change in I_{Dmax} and I_{Goff} in V_{DS} = 0 state step-stress experiments for different gate length devices. As the gate length increases, the critical voltage increases.

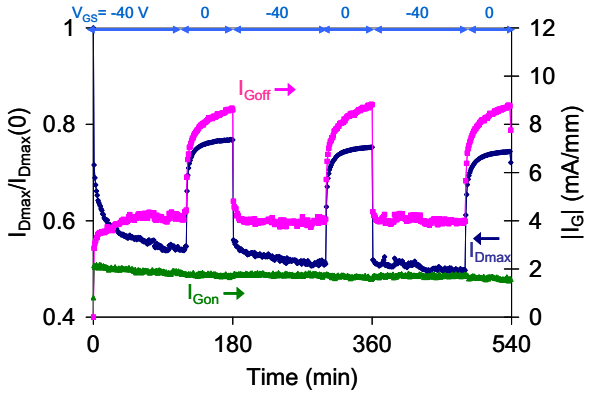

Fig. 10. Change in I_{Dmax}, I_{Goff}, and I_{Gon} in a V_{DS} = 0 stress-recovery experiment. The device is stressed for 2 h at V_{GS} = −40 V. This is followed by a 1 h long recovery period. This 3 h cycle was repeated 3 times.

minutes. After the stress is resumed, I_{Dmax} goes right back to where it was when the stress was removed and continues to degrade from there. This can be repeated multiple times. This behavior can be understood through trap formation and trapping. Somewhere in the early stages of degradation of this device, traps are formed. As electrons get trapped, I_{Dmax} is reduced through partial depletion of the channel charge. When the stress is removed, electrons detrap and I_{Dmax} is partially restored. Upon resumption of stress, electrons get promptly retrapped and I_{Dmax} drops to the same value that it had right before the stress was halted. Degradation continues from there.

It is interesting to observe in Fig. 10 that I_{Goff} also reveals prominent trapping phenomena. When electrons detrap during the recovery phase, I_{Goff} increases. During stress, when electrons fill the traps, I_{Goff} decreases. An explanation for this behavior is given below. Also of interest is the fact that I_{Gon} does not exhibit any trapping. This is undoubtly related to the fact that the activation energy of the forward gate current is unchanged as a result of stress (Fig. 3).

In separate experiments, we have been able to detrap electrons through temperature, microscope and UV light exposure and forward gate biasing. All this confirms that the prominent transients seen in Fig. 10 are produced by electron trapping and detrapping.

An intriguing question to answer is at what voltage trap formation takes place. Is that at V_{crit} or does it take place in a more grad-

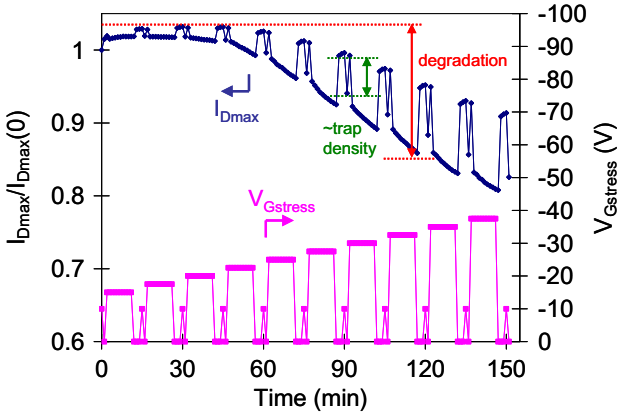

Fig. 11. Time evolution of I_{Dmax} and stress bias condition in a step-stress-recovery experiment in the V_{DS} = 0 state. For the stress period, V_{GS} was step stressed from −15 V to −37.5 V in 2.5 V step. A 10-min stress period is followed by a 5-min recovery period. At the end of the recovery period, a 1-s V_{GS} = −10 V pulse was applied to sample the trap density.

ual way? In order to answer this question, we have designed a step-stress-recovery experiment into which we have introduced a diagnostic pulse to track trap concentration [16,25]. This is shown in Fig. 11. This is a $V_{DS} = 0$ stress experiment in which the stress voltage is increased in a step fashion. In between steps, there is a recovery period. Inside the recovery period, there is a 10 V pulse that is applied to the gate. The response to this pulse is a good measure of current collapse and therefore trapping [25]. We can therefore track separately damage to the device, which is best measured through the drop of I_{Dmax} at the end of each stress step, and trap density, which is the response of I_{Dmax} to the voltage pulse. The entire experiment is performed under microscope light to speed up the detrapping transients.

As Fig. 11 shows, in the virgin state the device exhibits little trapping behavior. The application of a 10 V pulse affects I_{Dmax} very little. This does not change much in the early stages of the stress experiment. However, right around the same point where I_{Dmax} starts degrading due to stress, the response to the voltage pulse starts increasing. As the experiment progresses, both measures of degradation increase.

To put things in perspective, Fig. 12 graphs the change in I_{Dmax} at the end of the stress step (we term this degradation) and the change in I_{Dmax} in response to the voltage pulse (this measures trap density). It is clear that they both correlate and that they both start increasing in a significant way at the critical voltage. This, plus the synchronized trapping transients in I_{Goff} and I_{Dmax} shown in Fig. 10 suggest a common origin to the degradation in I_{Dmax} and I_{Goff} and it reveals the role of traps in this degradation.

The mechanical nature of this degradation mechanism can be confirmed by performing experiments under external uniaxial mechanical stress using a chip bending apparatus [21]. These experiments have shown that adding tensile strain reduces the critical voltage for degradation, just as expected from the inverse piezoelectric effect hypothesis.

We have recently developed a methodology for trap analysis that can be integrated with our electrical stress experiments [23]. In this methodology, we perform trapping and detrapping experiments under different conditions spanning six orders of magnitude in time right in the middle of stress experiments. From this study, we have been able to prove that trap formation starts at the critical voltage but continues beyond, that those traps are in the AlGaN barrier or at its surface, that the GaN buffer is unaffected by electrical stress, and that the traps are created in the drain side of the device (in OFF-state experiments). All these observations are consistent with our defect formation mechanism through the inverse piezoelectric effect.

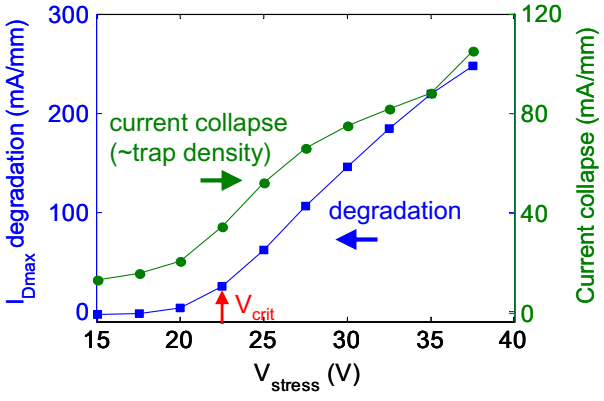

Fig. 12. Total I_{Dmax} degradation and change in current collapse and I_{Goff} in the experiment of Fig. 11. Both figures of merit sharply increase beyond a critical voltage V_{crit}.

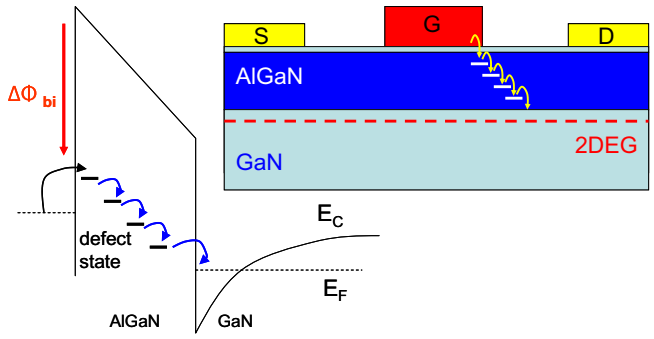

Fig. 13. Conceptual I_G degradation mechanism. Crystallographic defects produced by the inverse piezoelectric effect provide a leakage path for electrons from the gate to the channel across the AlGaN barrier.

A pictorial view of the role of traps in degraded GaN HEMTs after an OFF-state experiment is shown in Fig. 13. Stressing beyond the critical voltage creates traps in the AlGaN right next to the gate edge. These traps become a path way for electrons to flow from the gate down to the channel. If these traps get filled with electrons, their electrostatic influence partially depletes the electron charge in the channel and this degrades I_{Dmax} and R_D. The filling status of these traps affects I_{Goff}. When they are empty, electron flow is easy through them and I_{Goff} is high. When they are full, electron flow is hampered and I_{Goff} is small.

Other experiments that we have performed do not contradict our inverse piezoelectric effect hypothesis:

- We have seen no gate orientation dependence on the wafer (0, 30, 60, 90°) to the type of degradation that is studied here.
- We have also not seen any impact of the environment (N_2 vs. air).
- The prominent increase in I_G is irreversible.
- V_{crit} decreases with temperature [26].

5. Discussion

Our hypothesis for the mechanism behind electrical degradation that takes place at V_{crit} received dramatic confirmation through XTEM studies of degraded devices [1,27,28]. These have shown the presence of prominent crystallographic damage on the drain side of the device right next to the gate edge. The damage consists of dimples, cracks that extent through the AlGaN but stop at the GaN interface and, in extreme cases, metal diffusion from the gate down the crack. In addition, the level of crystallographic damage correlates with the degradation in the electrical characteristics of the device [28].

The identification of this electrical failure mechanism suggests several paths to its mitigation. As is often the case, these approaches are rarely without drawbacks, most often they affect performance.

Since the degradation mechanism that we postulate occurs when the elastic energy stored inside the AlGaN under the gate edge increases beyond its critical value, one path for mitigation consists of minimizing the initial stress in the AlGaN barrier. This can be accomplished by using a thinner barrier, as seen by Lee [29], by using AlGaN with lower AlN composition [20,30], by eliminating the AlN spacer layer, or by introducing an AlGaN buffer layer [16].

A second path to mitigation is mechanically strengthening the AlGaN barrier. This can be accomplished through a GaN cap [20] or by SiN passivation [31,32], which have shown to mitigate strain relaxation in the AlGaN layer significantly.

Yet a third path for mitigation consists of minimizing the electric field across the AlGaN barrier at the gate edge. This can be accomplished through field plates [27]. Engineering of the gate edge such as in a recessed device also ought to help. A reduction in sheet carrier concentration in the drain should also ameliorate the situation.

6. Conclusions

We have presented evidence behind an electrical degradation mechanism for GaN HEMTs that is associated with the strong piezoelectric nature of GaN and AlGaN. Under high voltage conditions, the high electric field that is produced introduces strong tensile stress in the AlGaN barrier layer that peaks right below the gate edge. This results in an increase in stored elastic energy inside the AlGaN. If this exceeds a critical value, crystallographic defects are formed that are electrically active. This provides a path for excess gate leakage current and it also results in electron trapping that depletes the sheet charge in the channel resulting in degradation of many figures of merit. This degradation mechanism can be mitigated through minimizing the initial strain in the AlGaN barrier layer, strengthening it from a mechanical point of view and managing the electric field distribution to moderate its peak under the gate.

Acknowledgements

This work was funded by a DARPA program (Mark Rosker, program manager) and ARL Contract #W911QX-05-C-0087 (Alfred Hung, COTR) and by Office of Naval Research Grant #N00014-08-1-0655 (Paul Maki and Harry Dietrich). We also acknowledge collaboration with TriQuint semiconductor and BAE Systems.

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