III-V's:
From THz HEMT to CMOS

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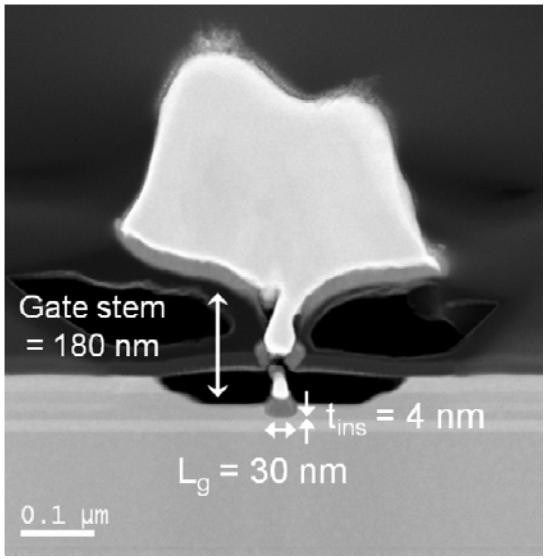
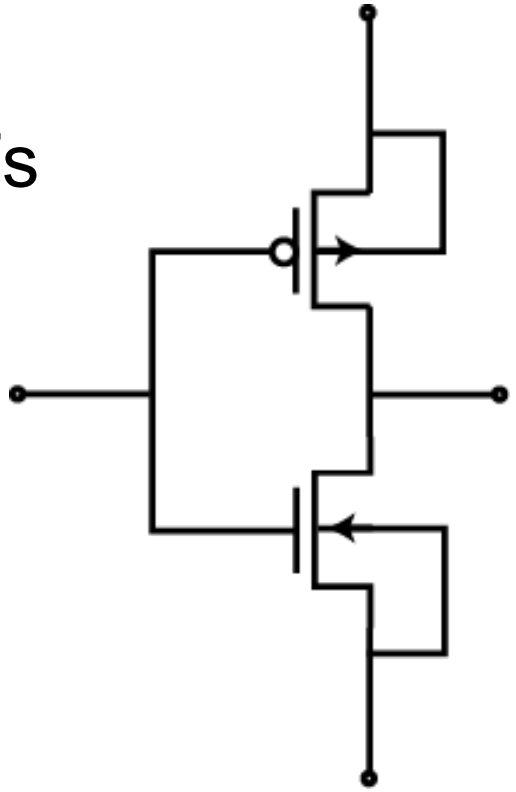
MTL, NSL, SEBL



Outline

- Introduction
- Near-THz III-V HEMTs
- Logic characteristics of III-V HEMTs
- III-V CMOS
- Conclusions



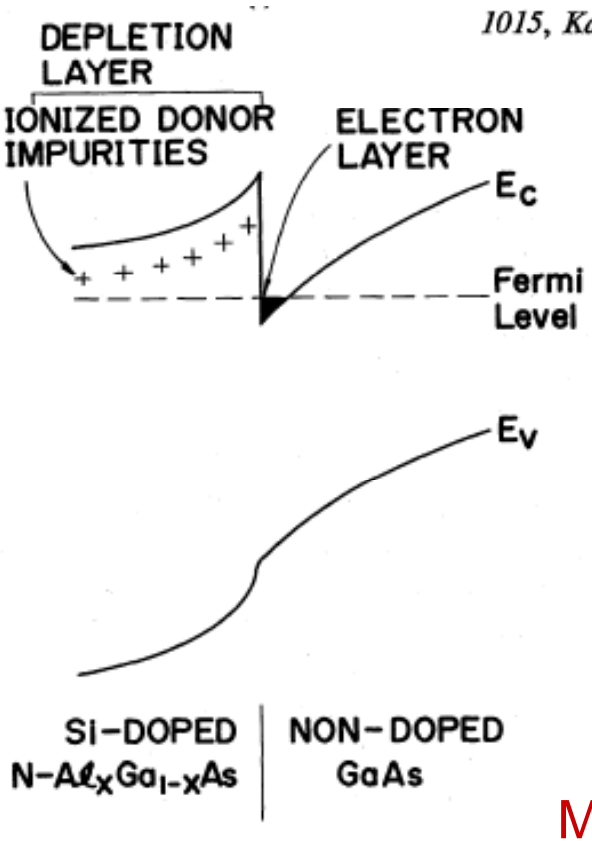
The High Electron Mobility Transistor

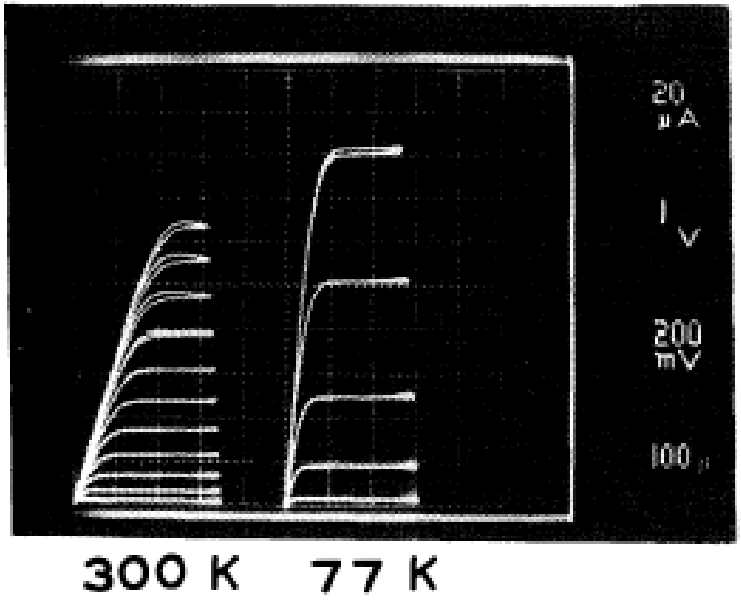
A New Field-Effect Transistor with Selectively Doped GaAs/n-$Al_xGa_{1-x}As$ Heterojunctions

Takashi MIMURA, Satoshi HIYAMIZU, Toshio FUJII and Kazuo NANBU

Fujitsu Laboratories Ltd.,
1015, Kamikodanaka, Nakahara-ku, Kawasaki 211

(Received March 24, 1980)

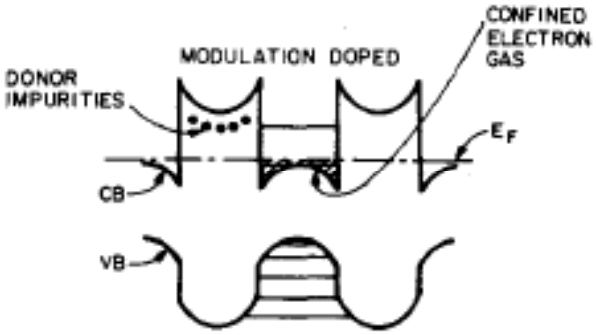


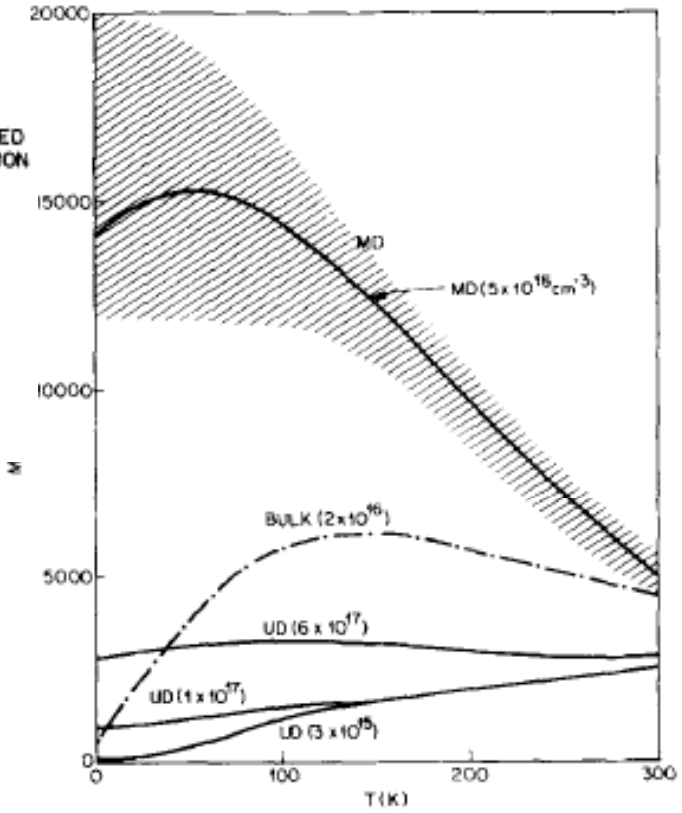


Mimura, JJAPL 1980

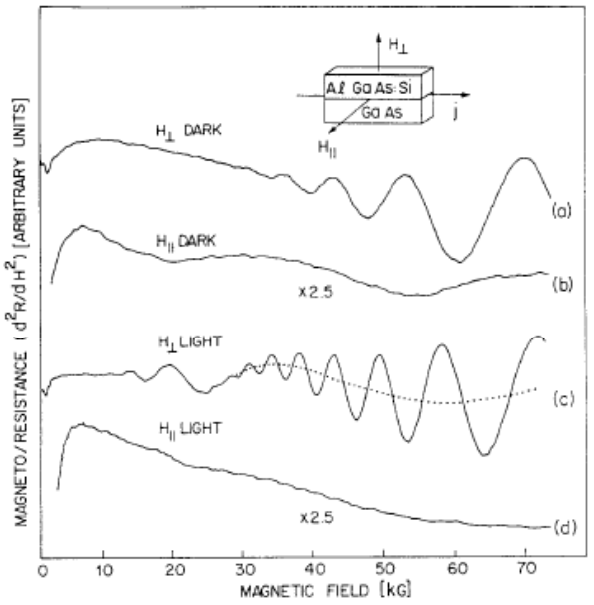
Modulation doping

- High electron mobility in modulation-doped AlGaAs/GaAs heterostructures
- 2 DEG at AlGaAs/GaAs interface



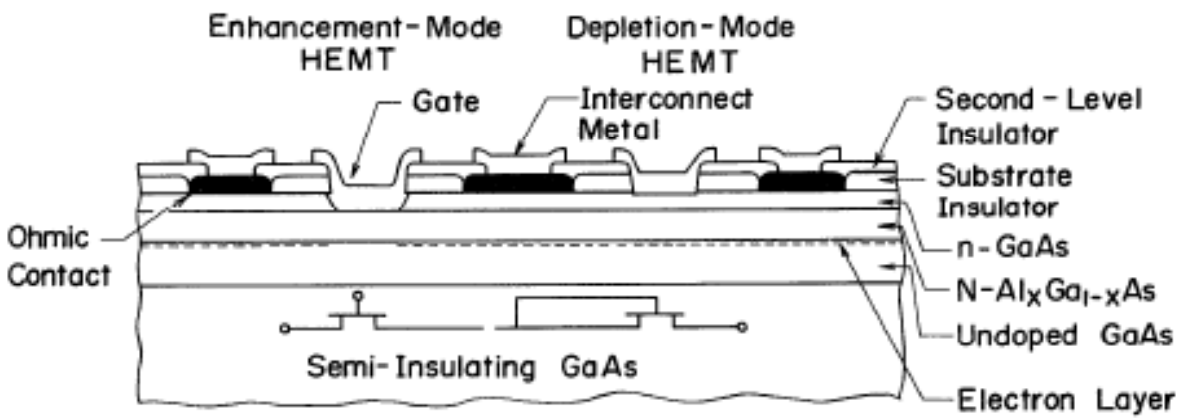


Dingle, APL 1978

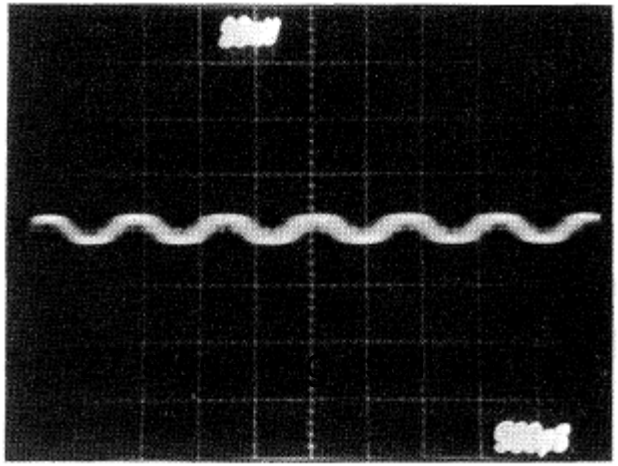


Stormer, Solid St Comm 1979

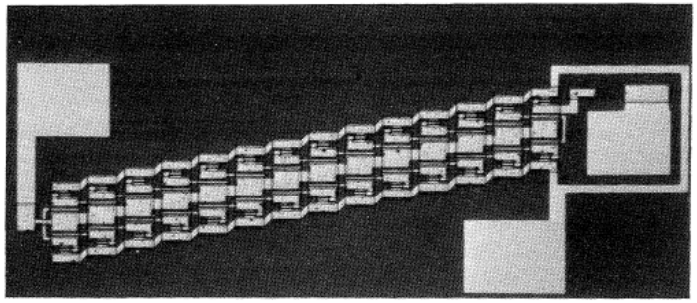
HEMT circuits



E/D logic



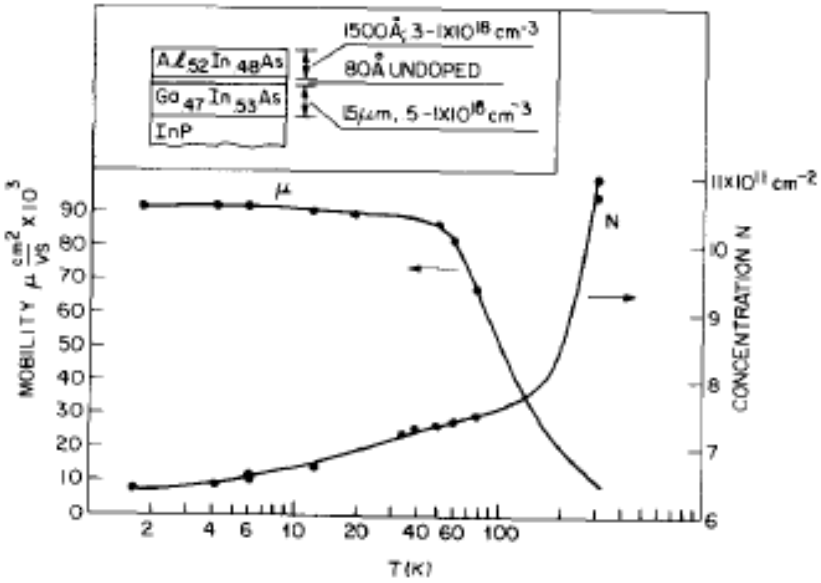
"The switching delay of 17.1 ps is the lowest of all the semiconductor logic technologies reported thus far."



Mimura, JJAPL 1981

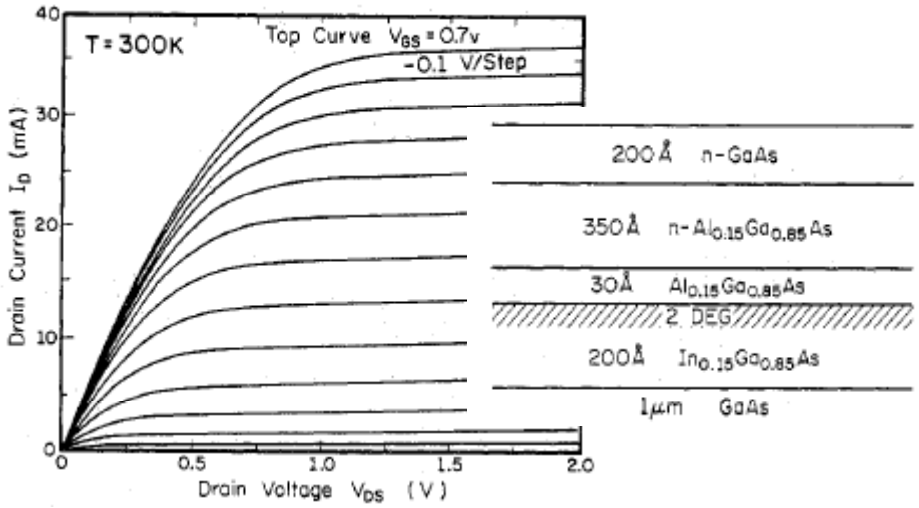
HEMTs in other material systems

InAlAs/InGaAs on InP



Kastalsky, APL 1982

AlGaAs/InGaAs PHEMT



Ketterson, EDL 1985

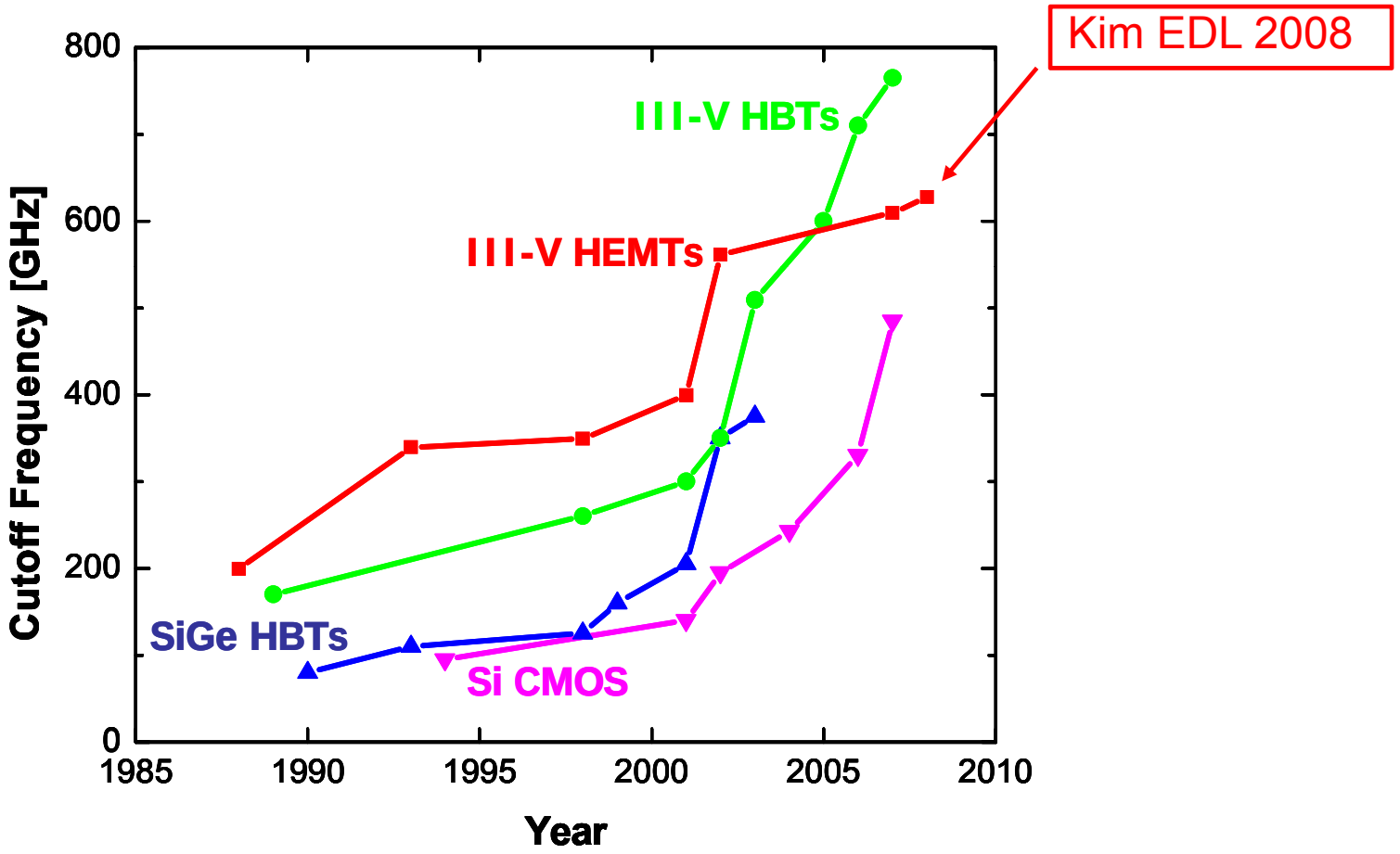
Also in AlGaN/GaN, Si/SiGe, AlSb/InAs, etc

Also with holes in many heterojunction systems

HEMT Electronics:
“You’ve come a long way baby!”

Near THz HEMTs

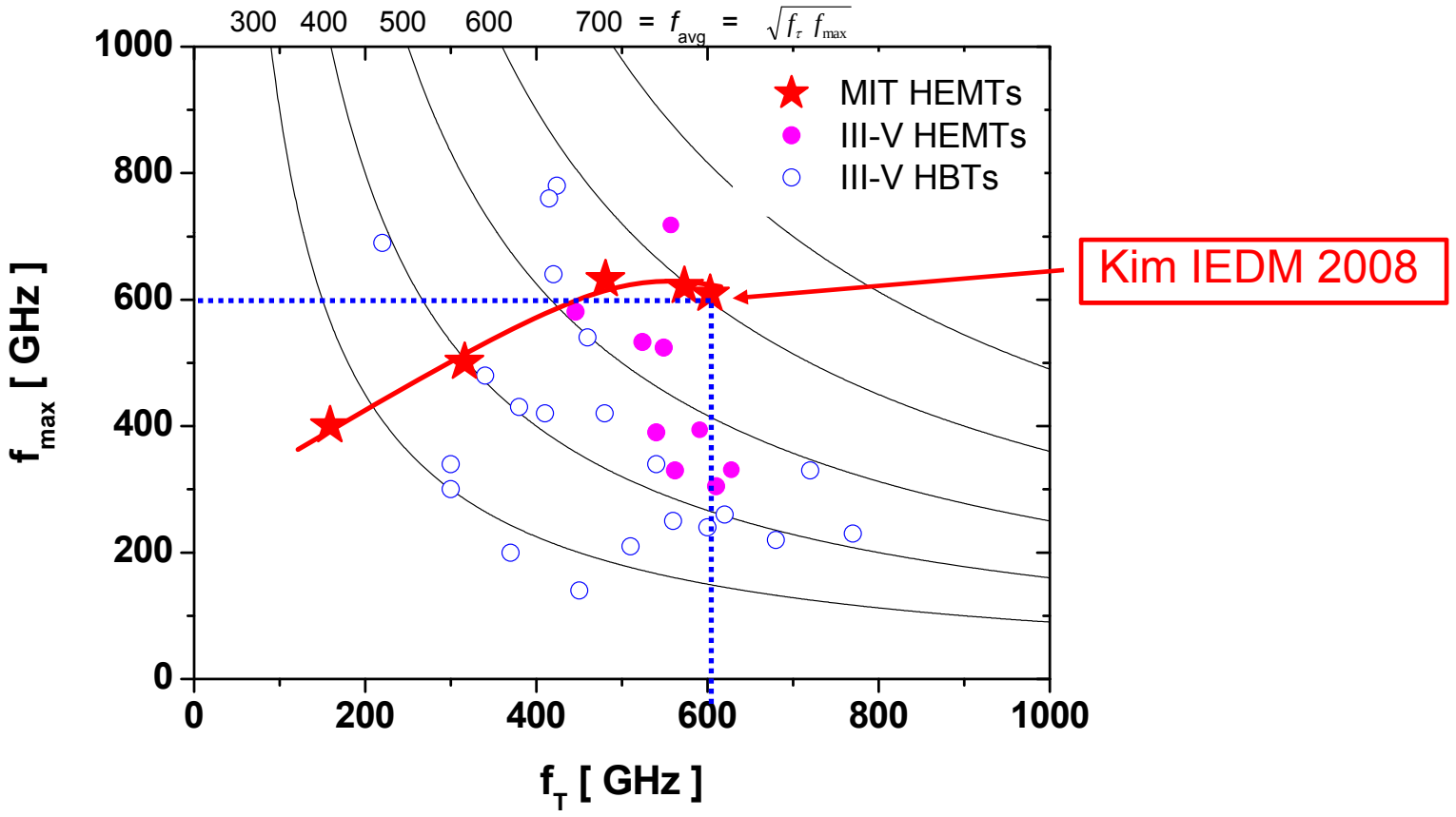
- f_T vs time:



For over 20 years, f_T (III-V's) > f_T (Si)

Near THz HEMTs

- f_T vs f_{max}:

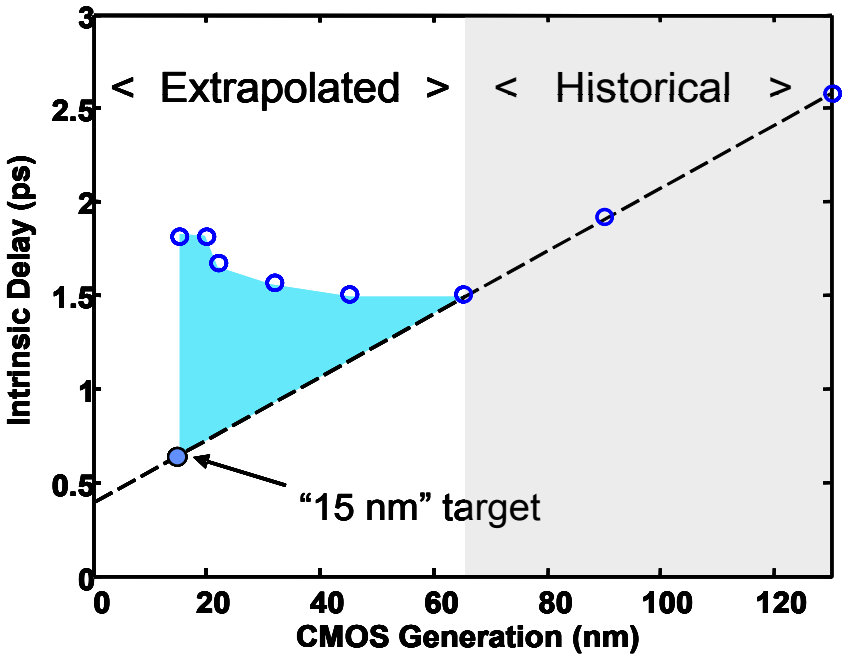


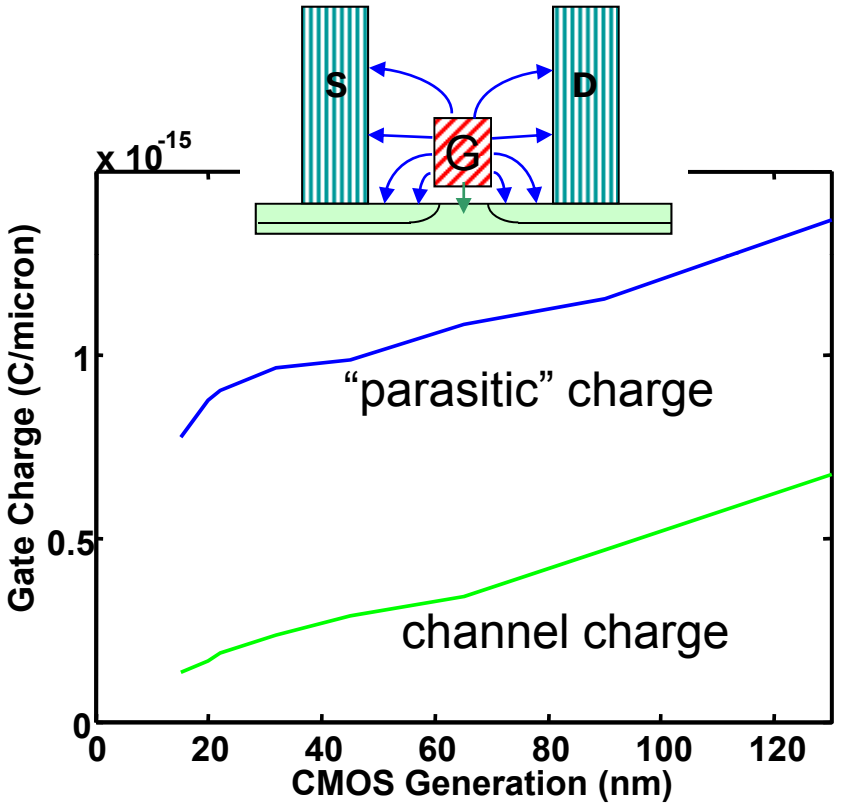
III-V HEMT: only device with f_t, f_{max}>600 GHz

III-Vs for CMOS?

- Si scaling running into increasing difficulties:

Courtesy of Dimitri Antoniadis (MIT)

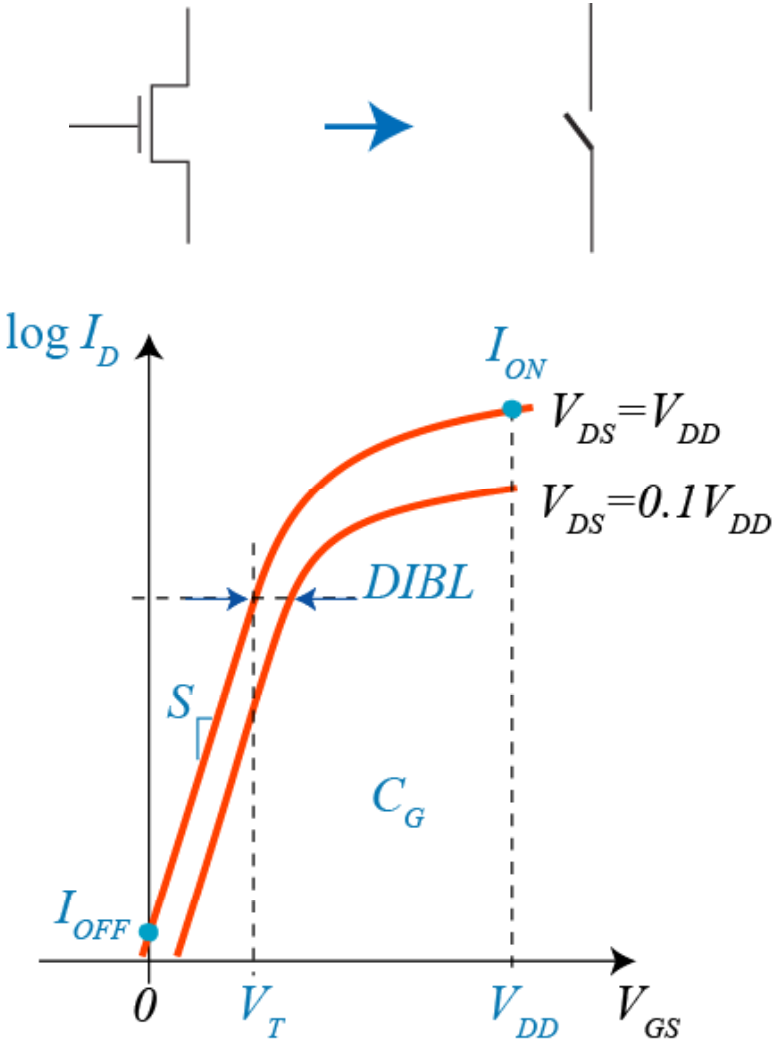




Parasitics becoming overwhelming → need higher current

Transistor as switch

In logic applications transistor operates as ***switch***

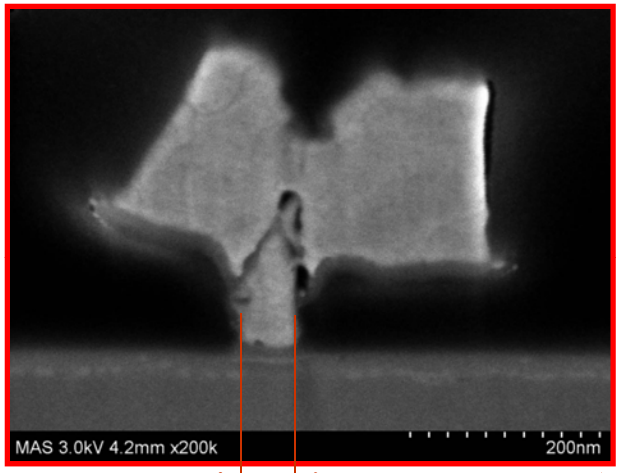


Interested in:

- ON current (I_{ON})
- OFF current (I_{OFF})
- V_T
- V_T dependence on L_g
- V_T dependence on V_{DS} (DIBL)
- Subthreshold swing (S)
- Device footprint
- Gate capacitance
- Operating voltage (V_{DD})

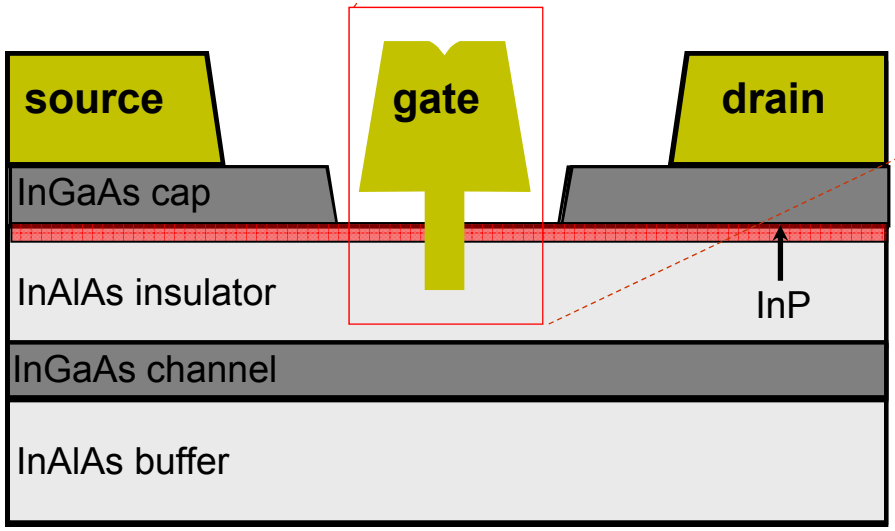
How Do III-V FETs Look for Logic?

Logic Characteristics of InGaAs High-Electron Mobility Transistor



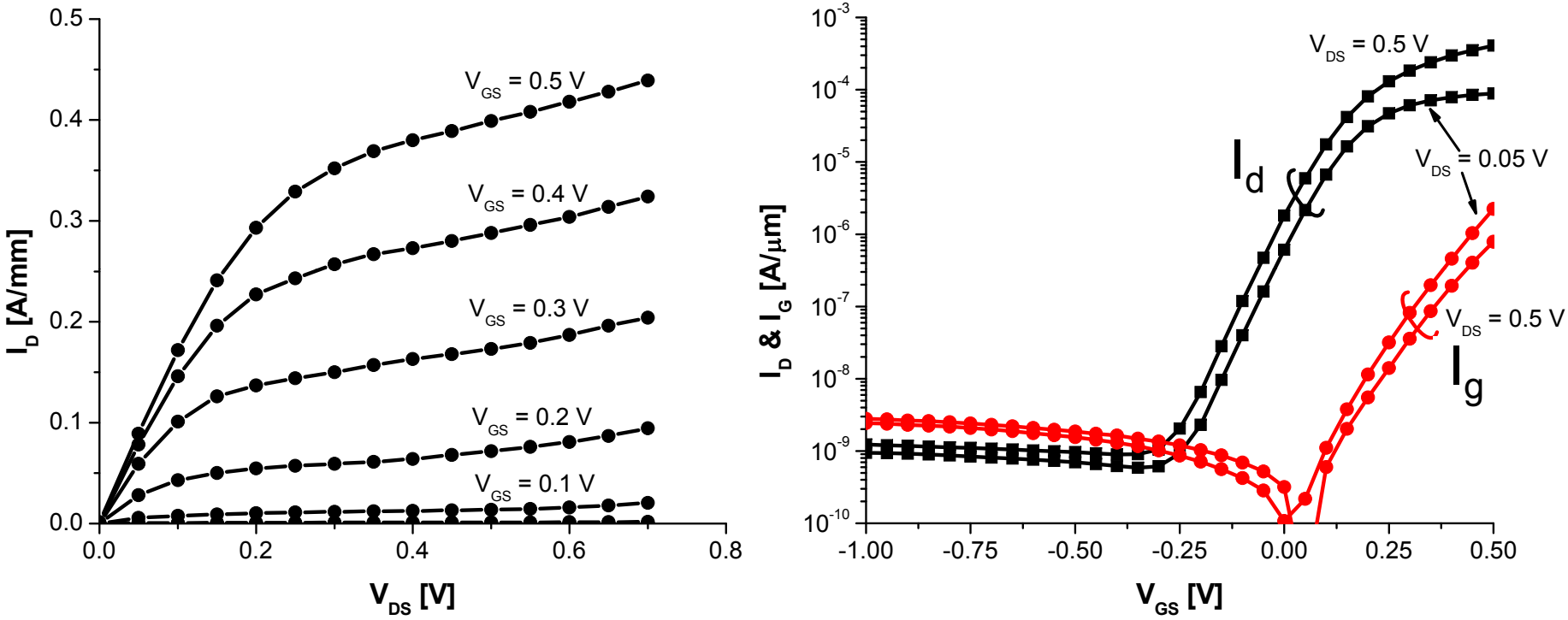
L_g ~ 60 nm

Kim, IEDM 2006



- Substrate is InP
- Channel is $In_{0.7}Ga_{0.3}As$
  μ > 10,000 $cm^2/V.s$ at 300K
- Barrier is $In_{0.52}Al_{0.48}As$

60 nm InGaAs HEMT

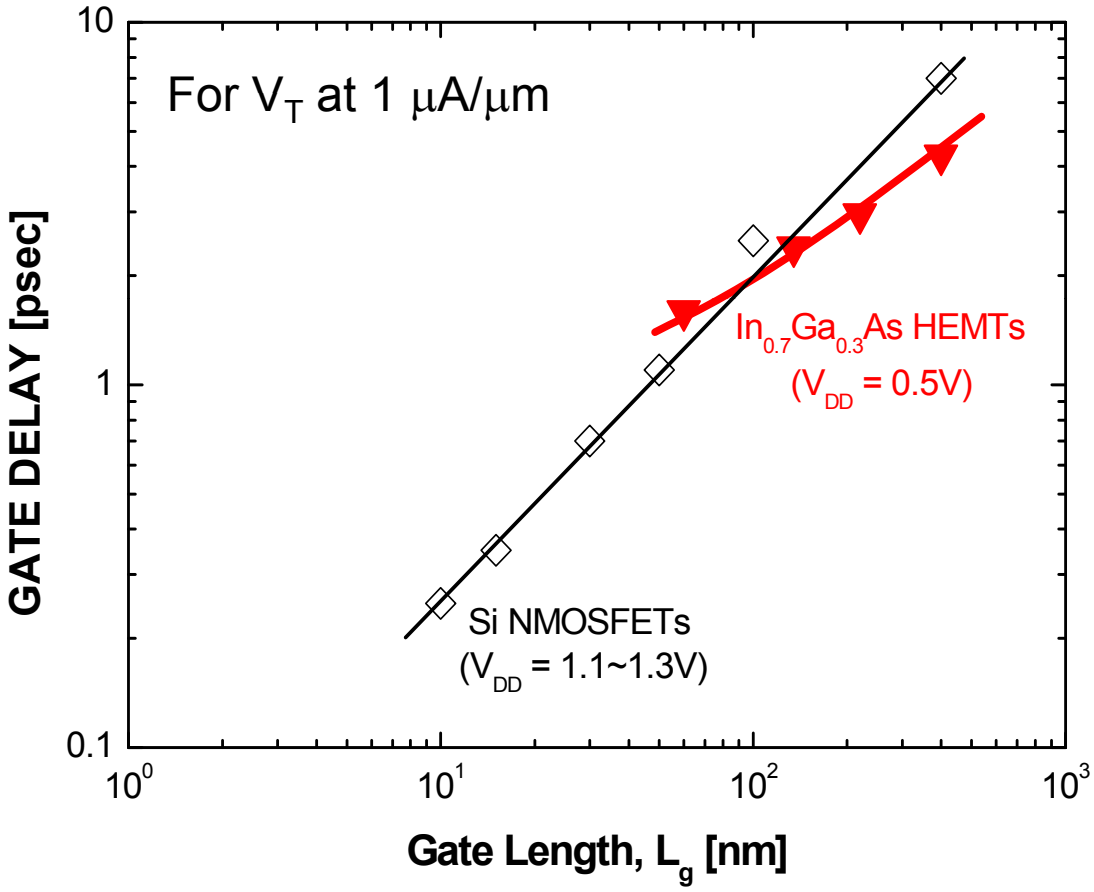


Kim, IEDM 2006

At 0.5 V:

V_T= -0.02 V, S= 88 mV/dec, DIBL= 93 mV/V, $I_{on}/I_{off} > 10^4$

Benchmarking Against Si MOSFET: Gate Delay (CV/I) vs. L_g



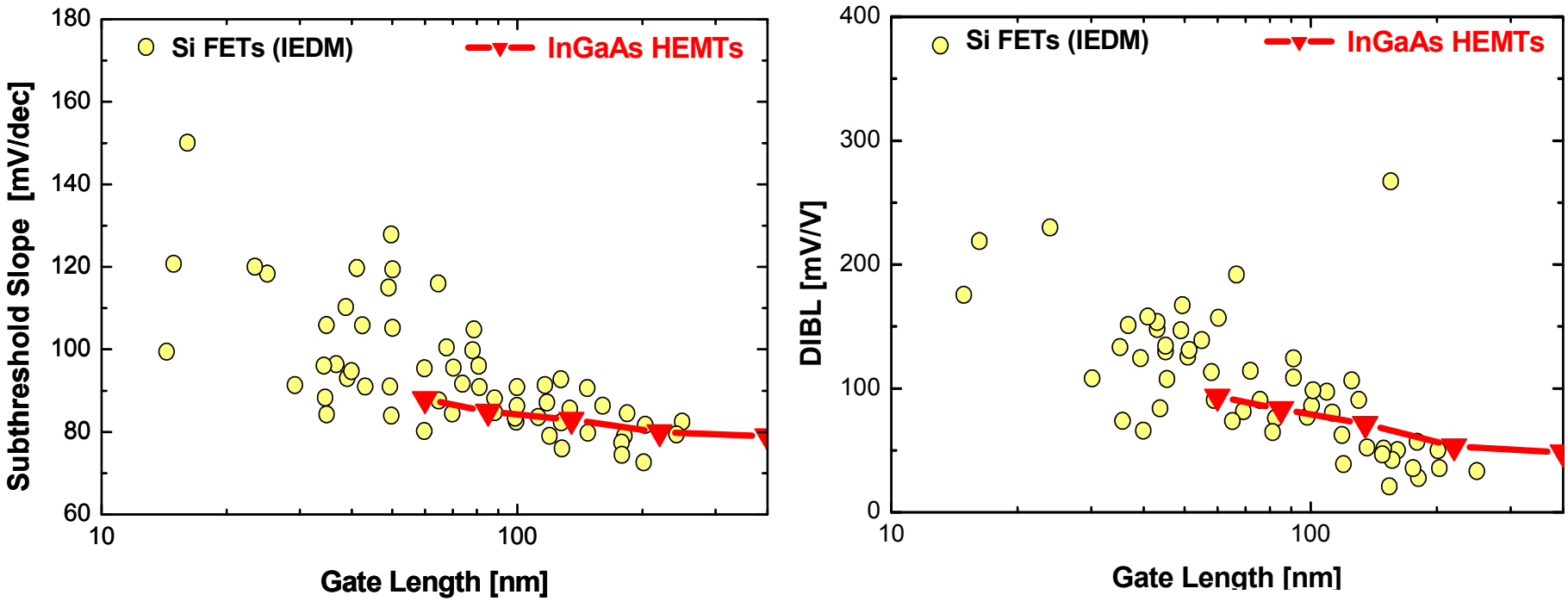
Kim, IEDM 2006

Si data from Chau, T-Nano 2005

Gate delay comparable to Si, in spite of lower voltage

Benchmarking Against Si MOSFET: S & DIBL vs. L_g

Kim, IEDM 2006



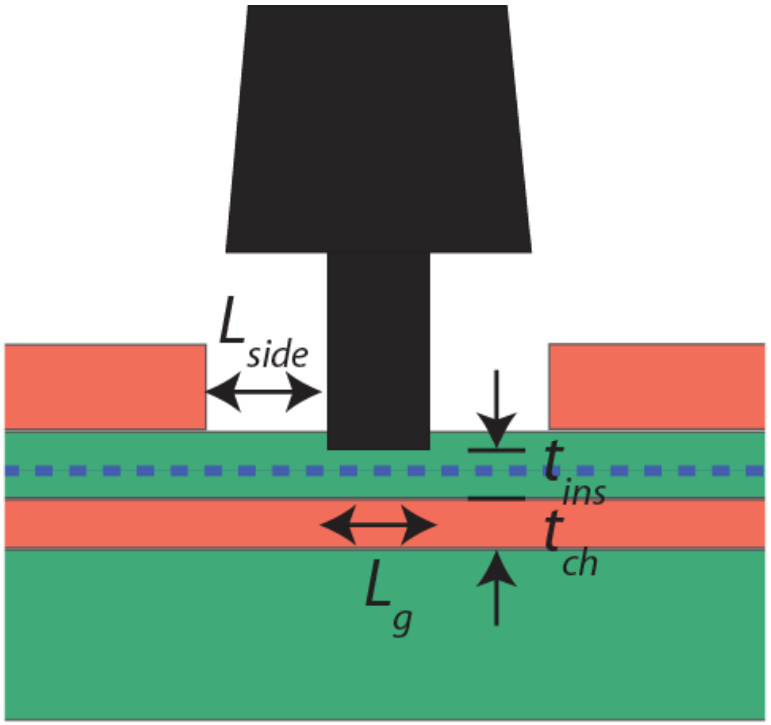
At L_g=60 nm, InGaAs HEMT as good as Si MOSFET

→ Can this device concept scale to the 15 nm node?

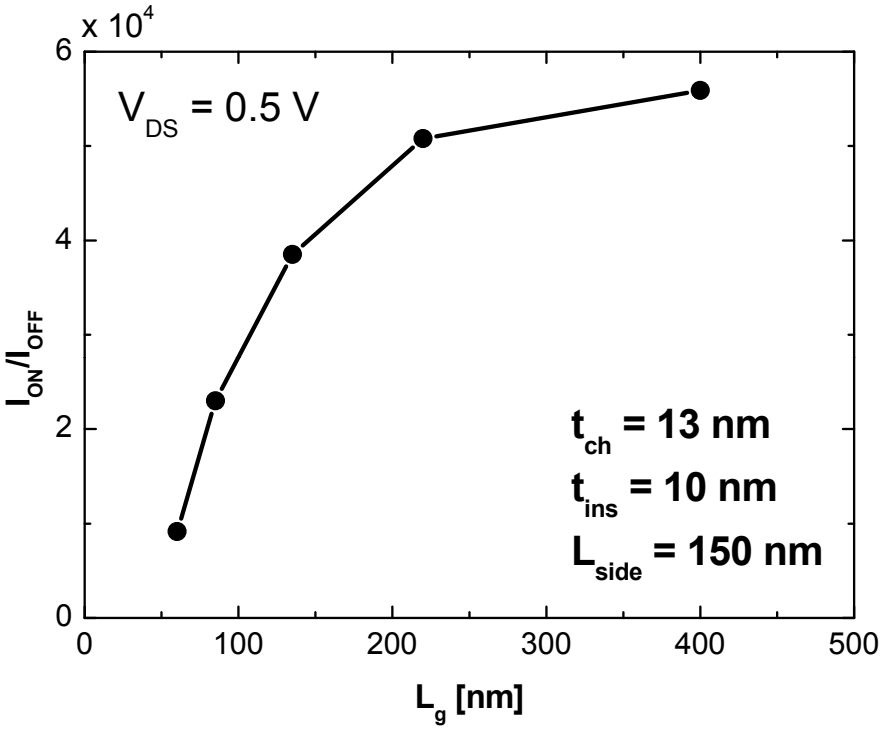
→ How will its performance compare with Si?

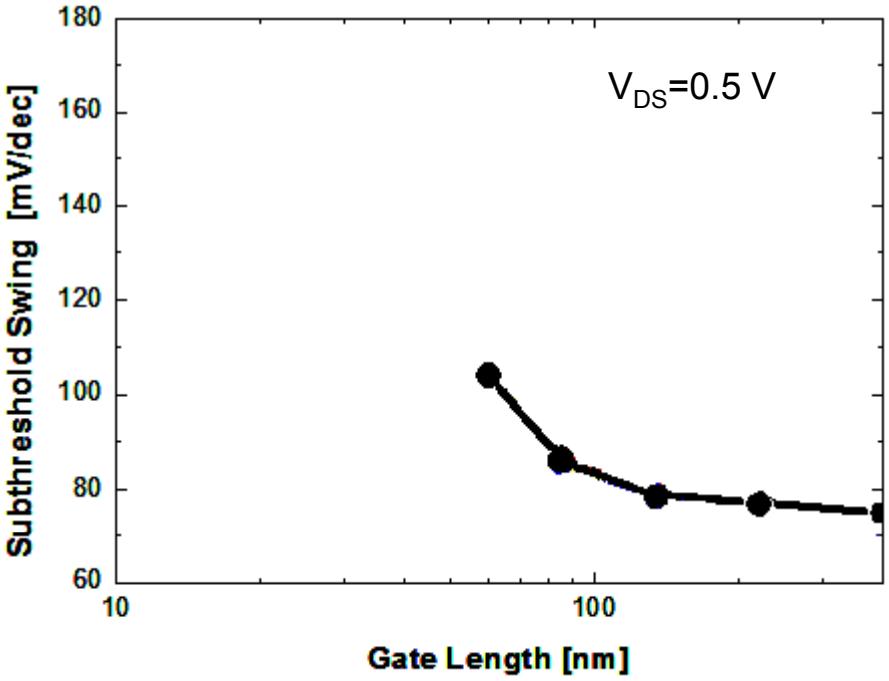
HEMT scaling

- Key dimensions: L_g, t_{ins}, t_{ch}, L_{side}
- Scaling trajectory:
  - $L_g \downarrow \rightarrow$
    - $t_{ins} \downarrow$
    - $t_{ch} \downarrow$
    - L_{side}?



Impact of gate length

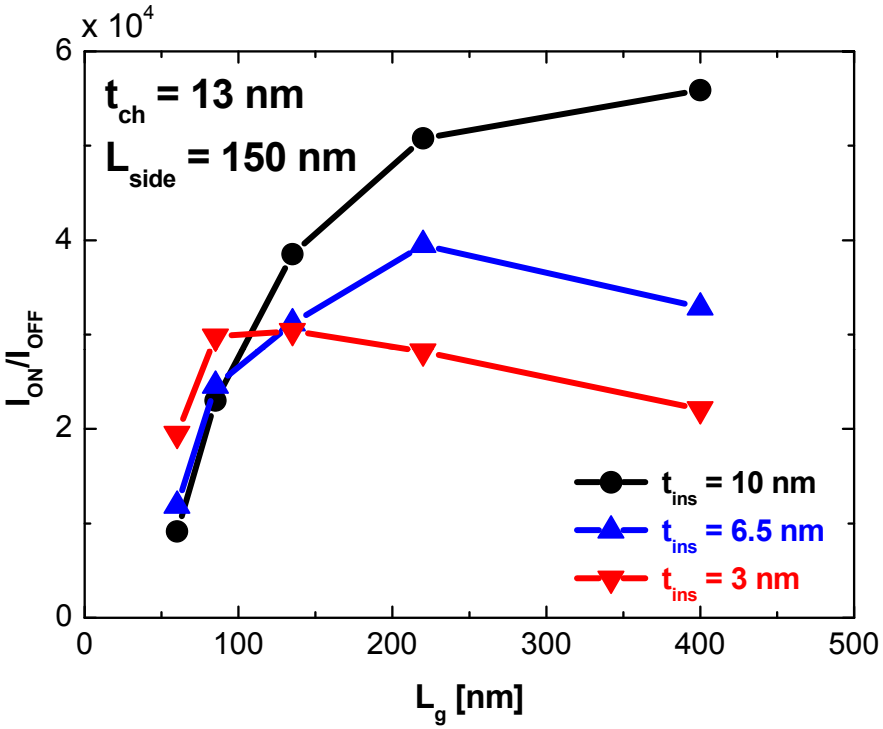


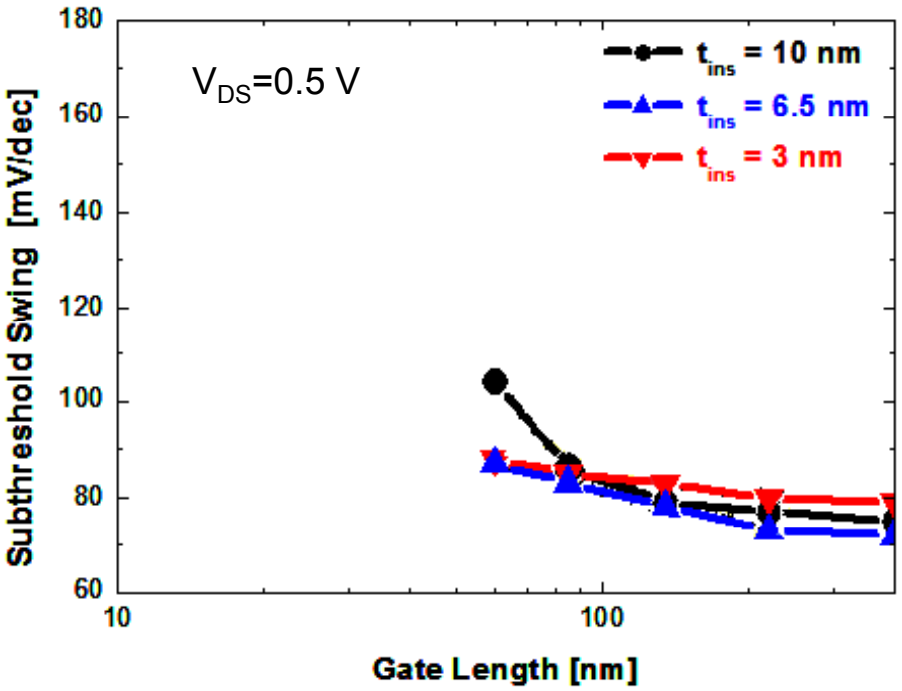


- $L_g\downarrow$
  - I_{on}/I_{off} drops in the sub-200 nm regime
  - SCE worsen

Kim, IEDM 2006

Impact of barrier thickness

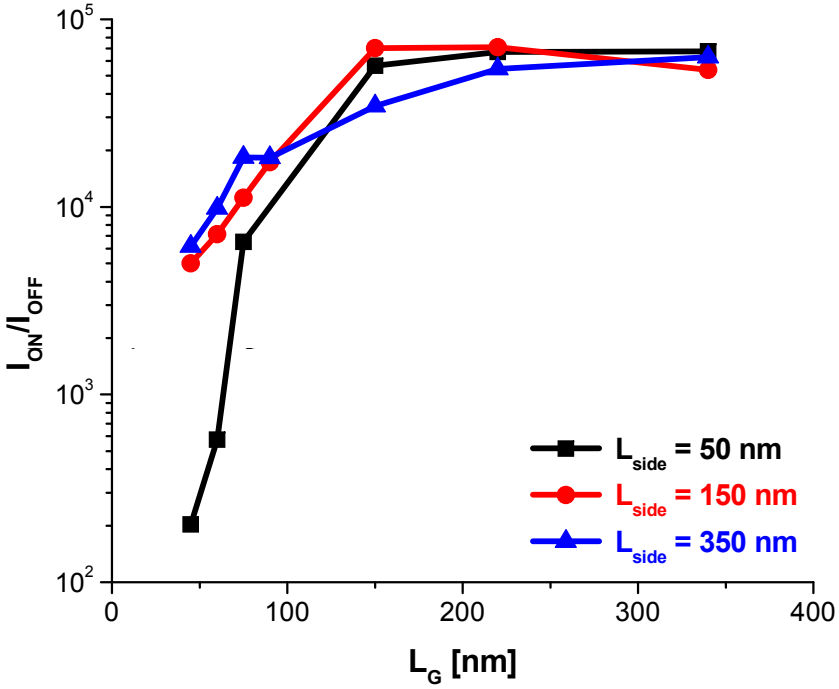


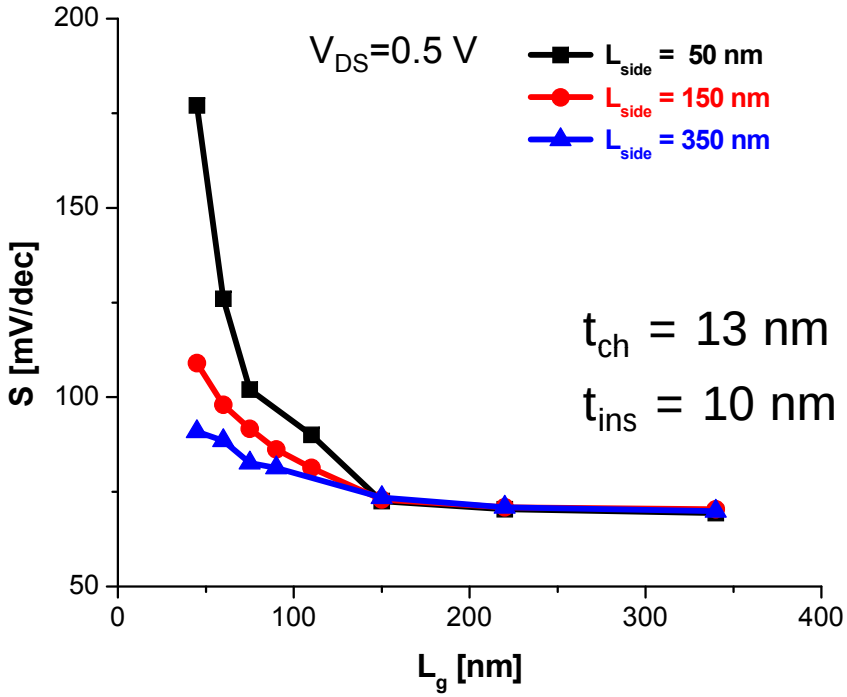


- t_{ins}↓
  - I_{on}/I_{off} worsens for long L_g due to I_G↑ and R_s↑
  - SCE and scalability improve

Kim, IEDM 2006

Impact of side recess length





- $L_{side}\uparrow$

  – I_{on}/I_{off} scalability improves

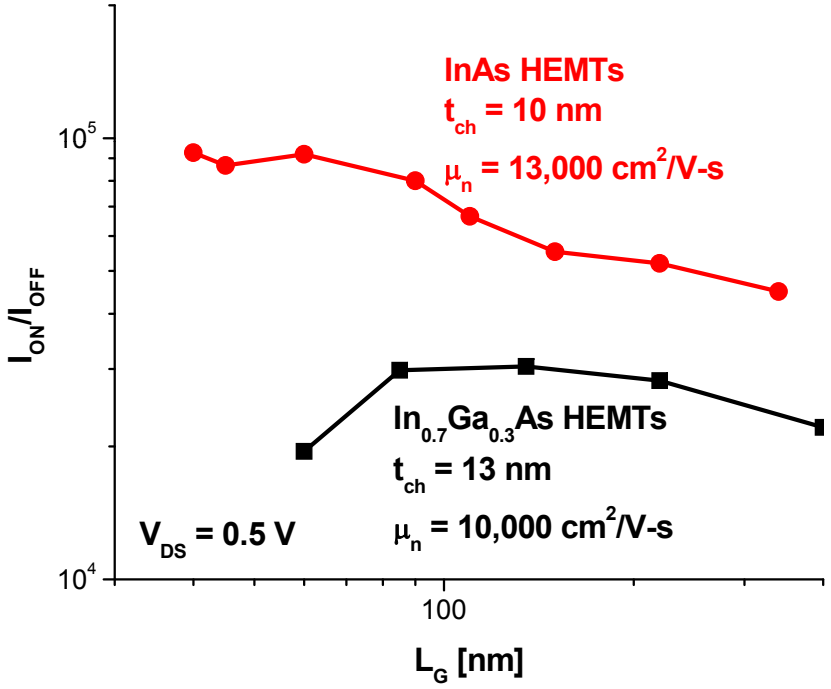
  – Better SCE

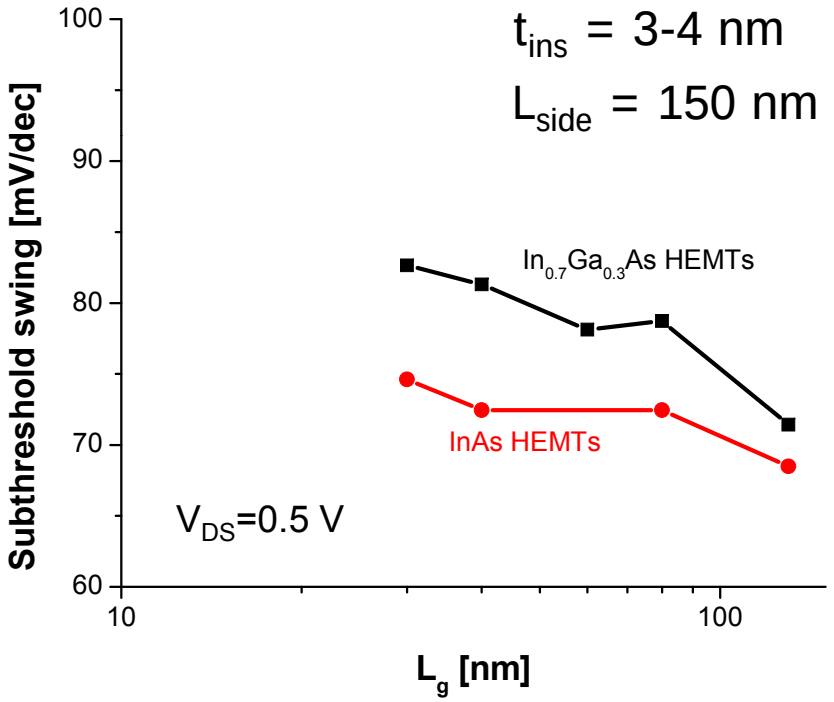
  – But… minimum L_{side} shortens as $t_{ins}\downarrow$ $t_{ch}\downarrow$

Kim, ISDRS 2007

Impact of channel thickness

- $t_{ch}\downarrow$ → performance degradation
  → increase InAs composition in channel

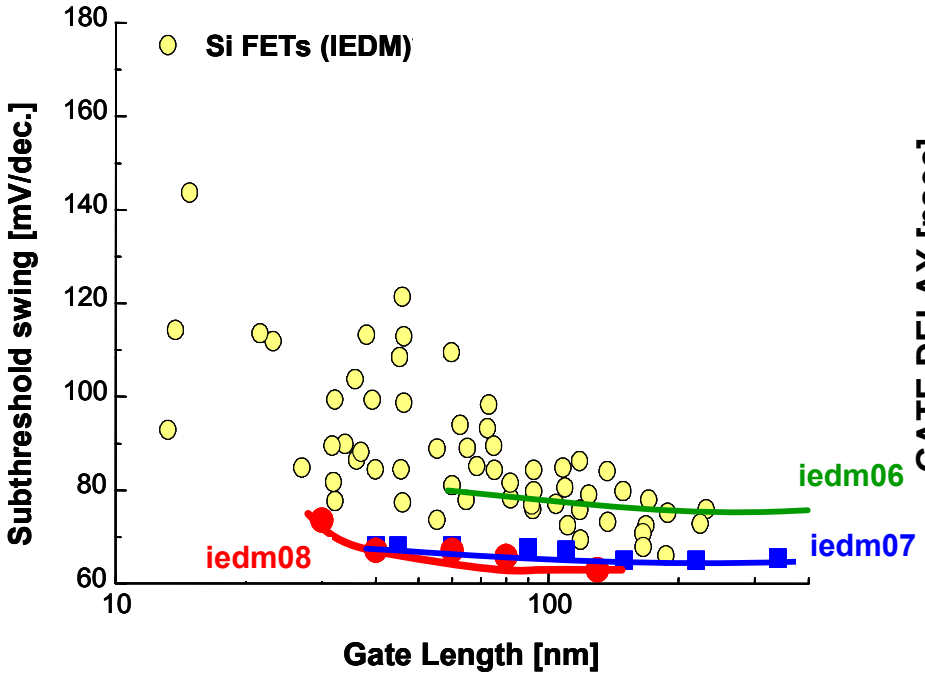


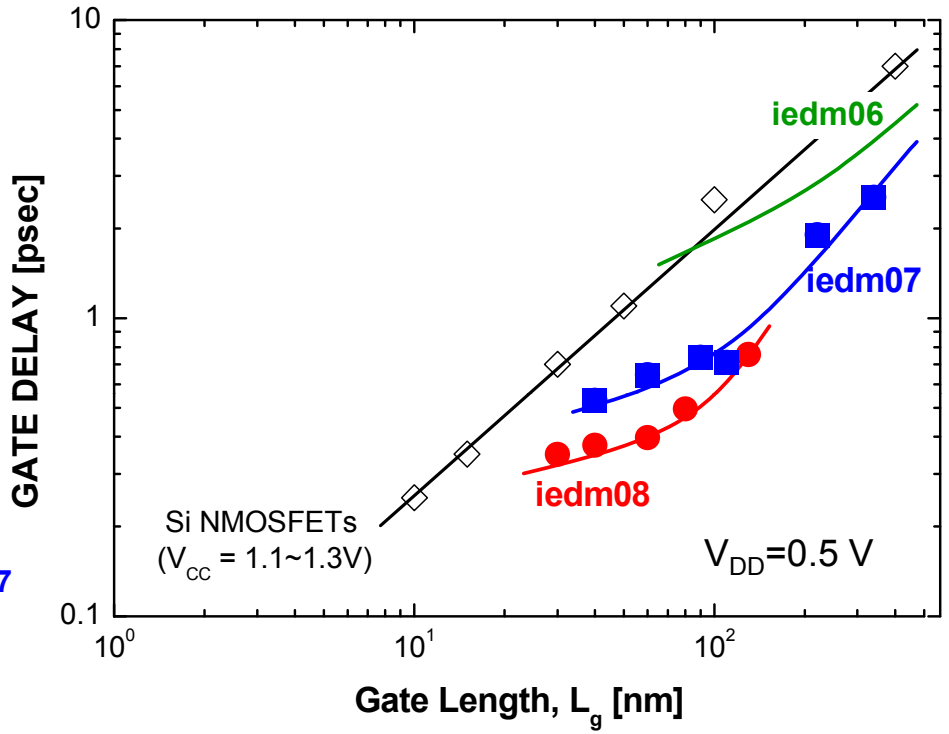


- $t_{ch}\downarrow$ + x(InAs)↑
  → $I_{on}/I_{off}\uparrow$, better scalability, better SCE

Kim, IEDM 2007

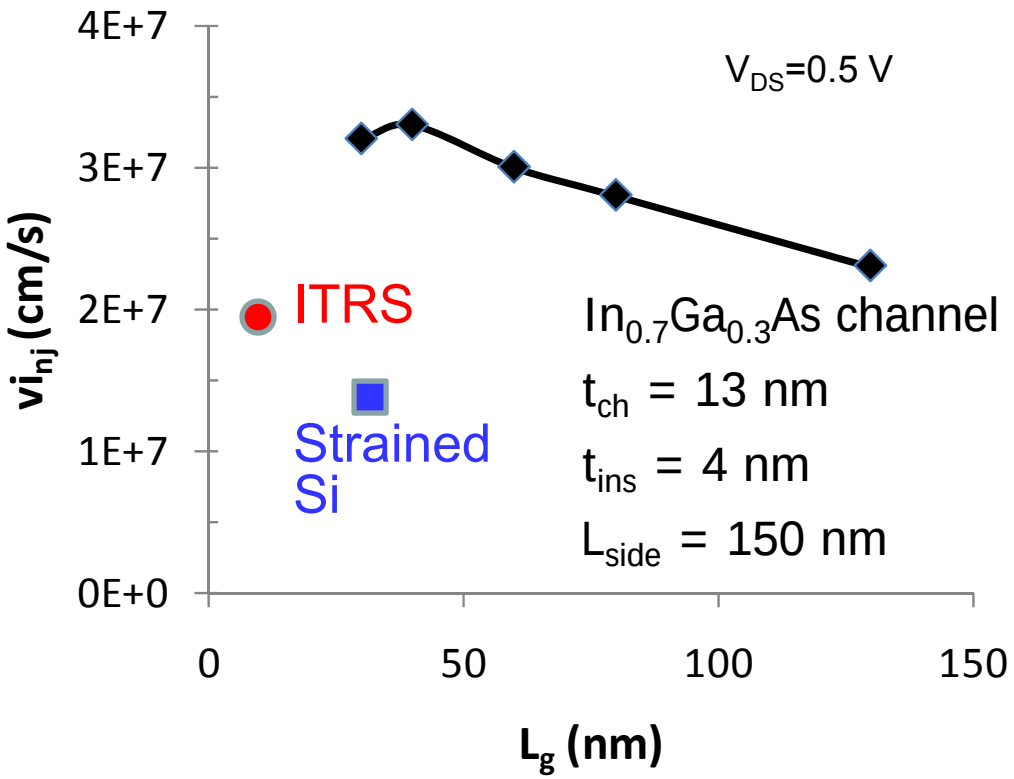
Scaled HEMTs: Benchmarking with Si

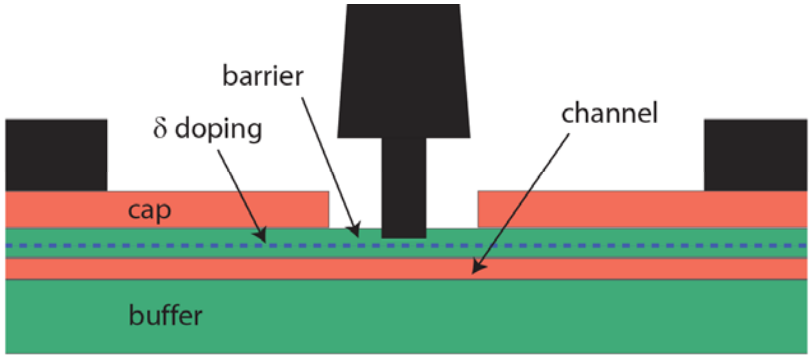




- Scaled to L_g=30 nm
- Superior short-channel effects as compared to Si MOSFETs
- Lower gate delay than Si MOSFETs at lower V_{DD}

What's behind such performance?

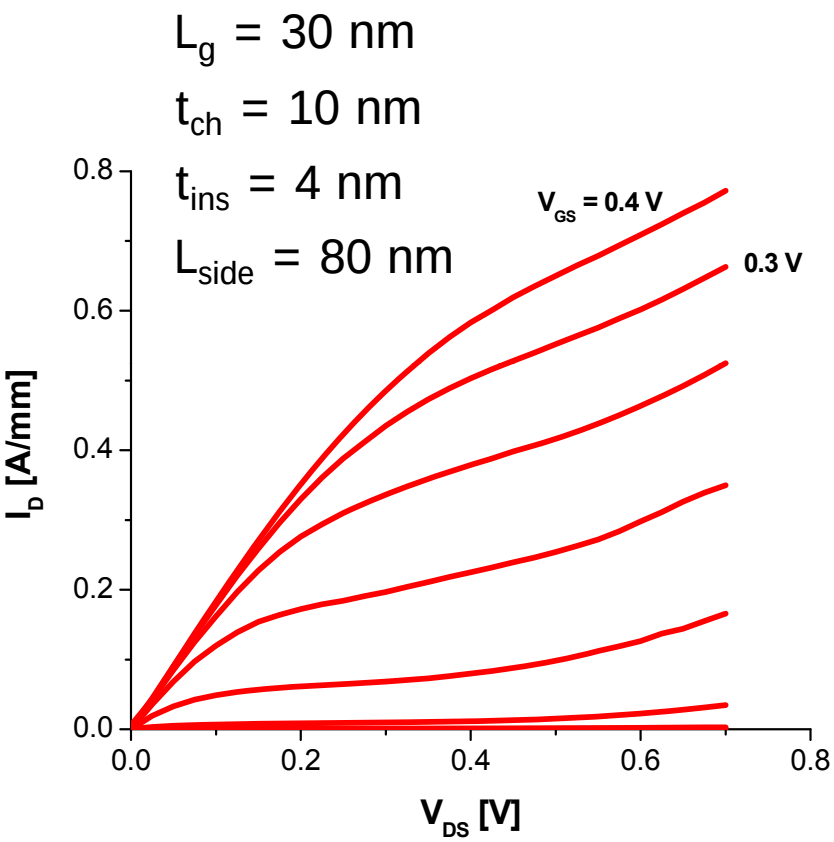


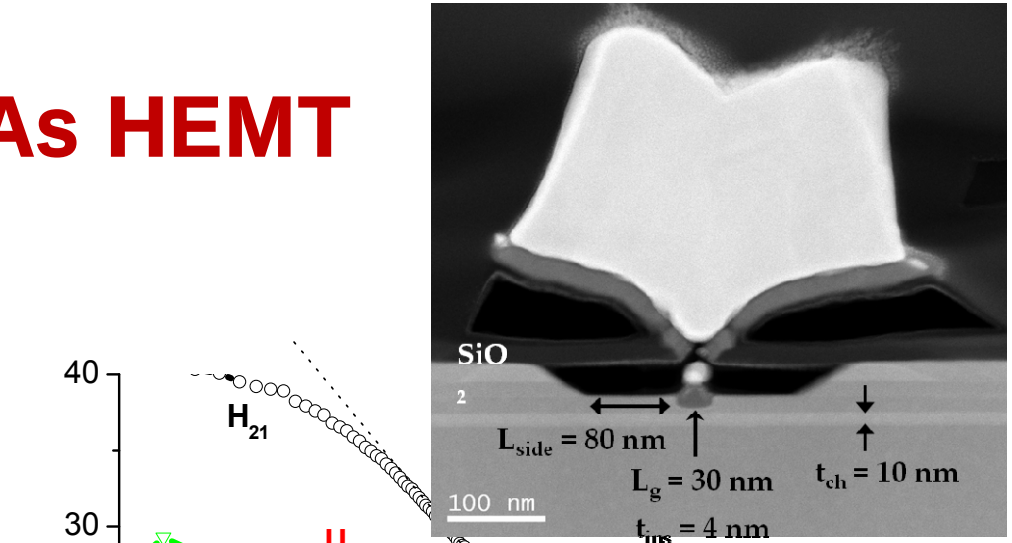


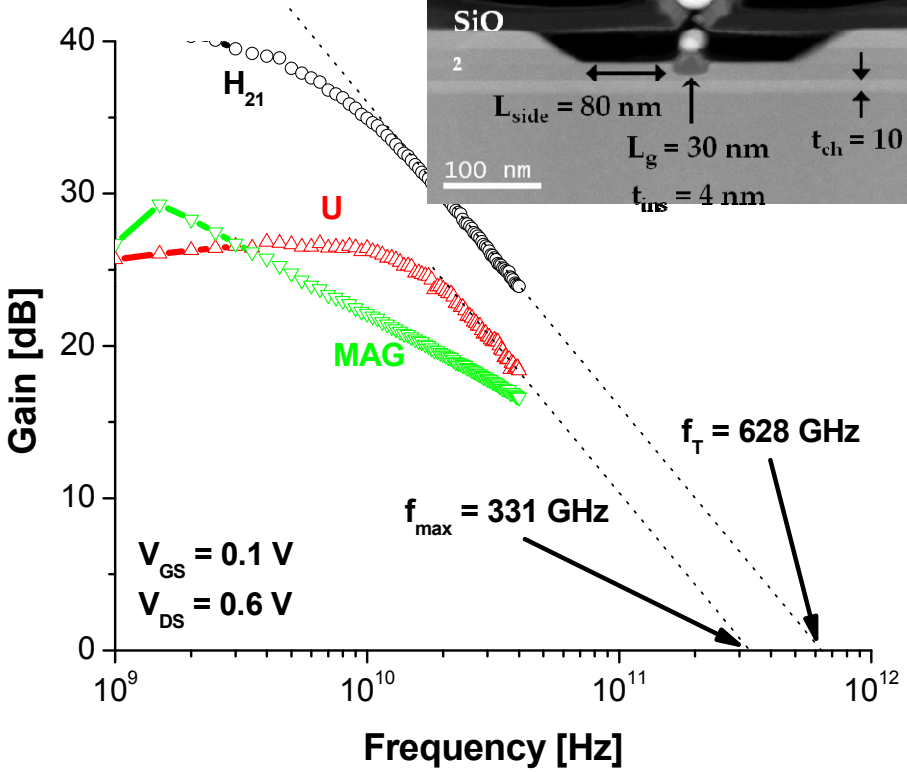
- High electron velocity in channel (v_{inj}>3x10^7 cm/s)
- Medium-K barrier
- Quantized channel
- 2DEG extrinsic region

→ outstanding SCE

30 nm InAs HEMT



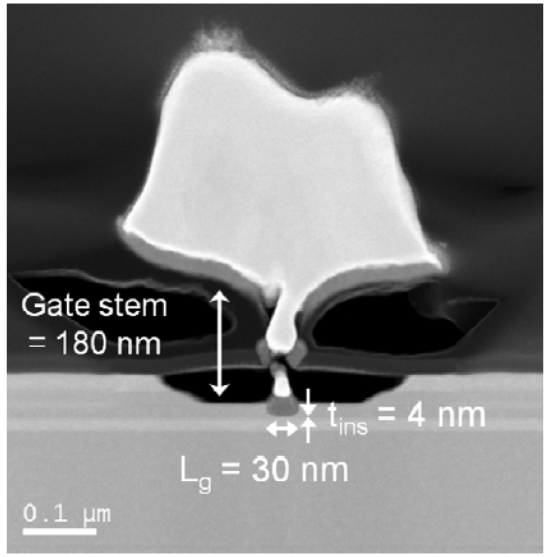




- Paying attention to SCE pays off in frequency response
- f_T=628 GHz: highest f_T reported on any FET on any material system

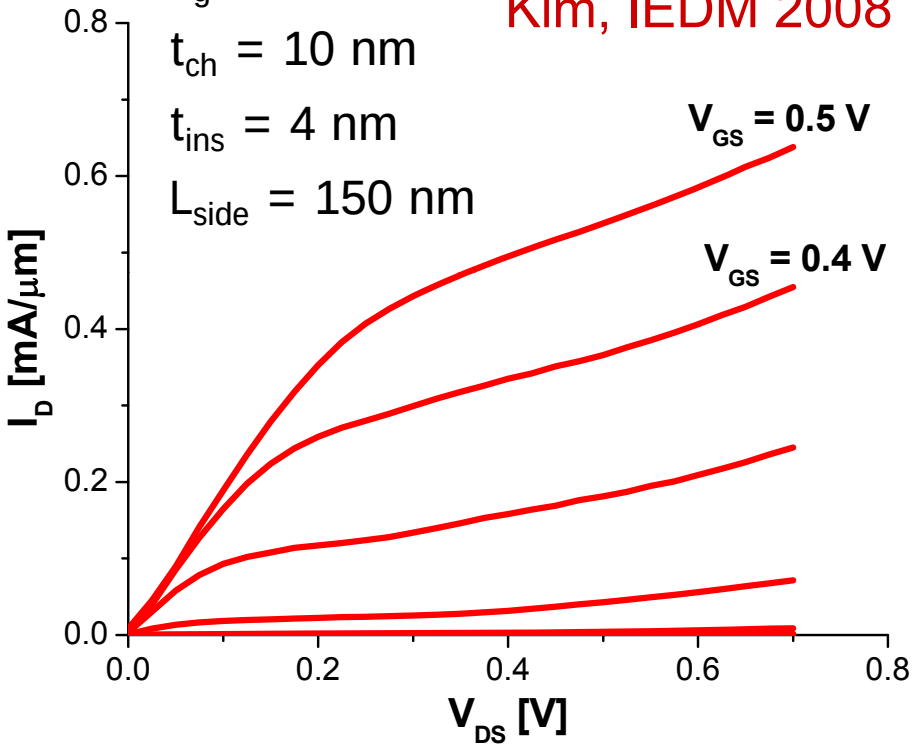
Kim, EDL 2008

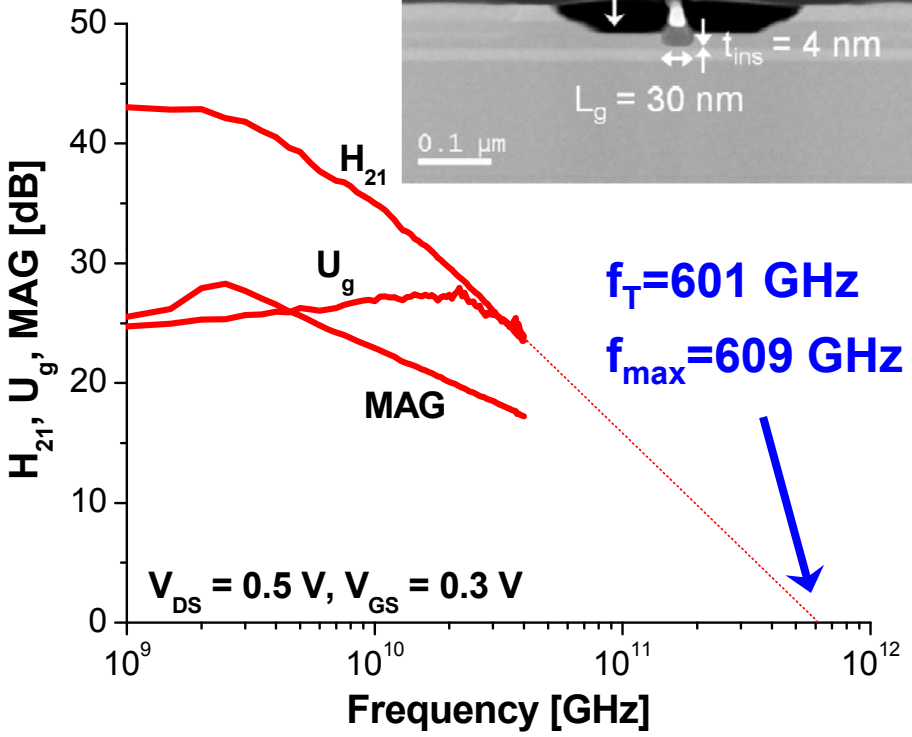
30 nm InAs HEMT by Pt Sinking



L_g = 30 nm
t_{ch} = 10 nm
t_{ins} = 4 nm
L_{side} = 150 nm

Kim, IEDM 2008

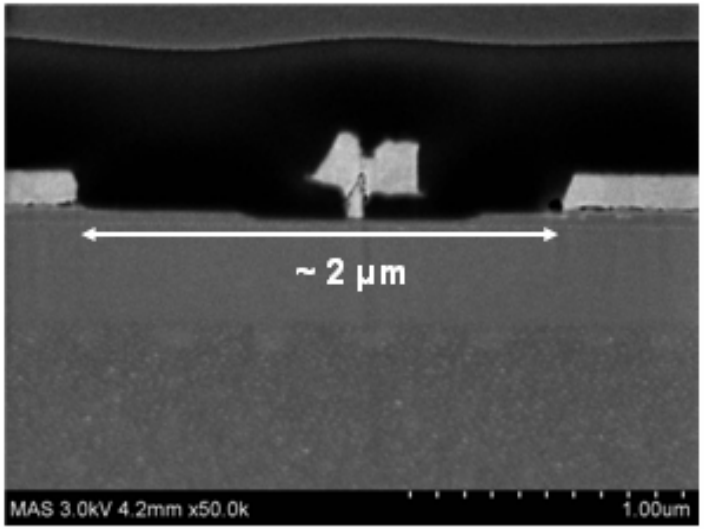




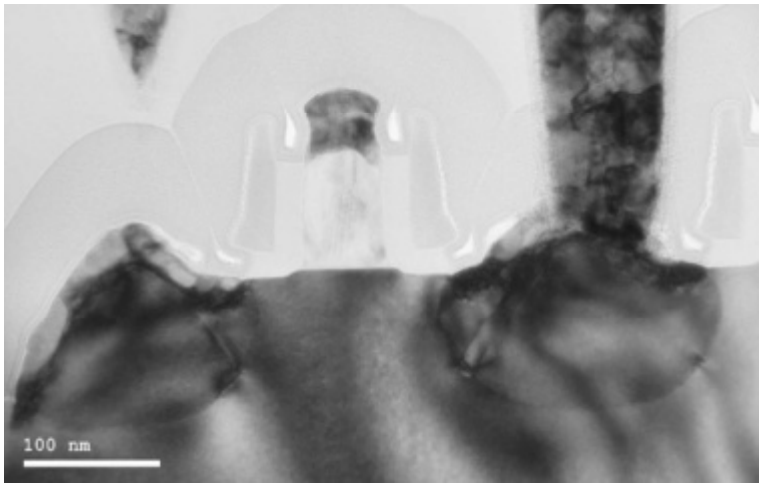
- 180 nm gate stem height to reduce parasitic capacitance
- Enhancement mode FET: V_T = 0.08 V
- First transistor with both f_T and f_{max} > 600 GHz

III-V HEMT vs. Si CMOS

60 nm HEMT



Intel's 65 nm CMOS

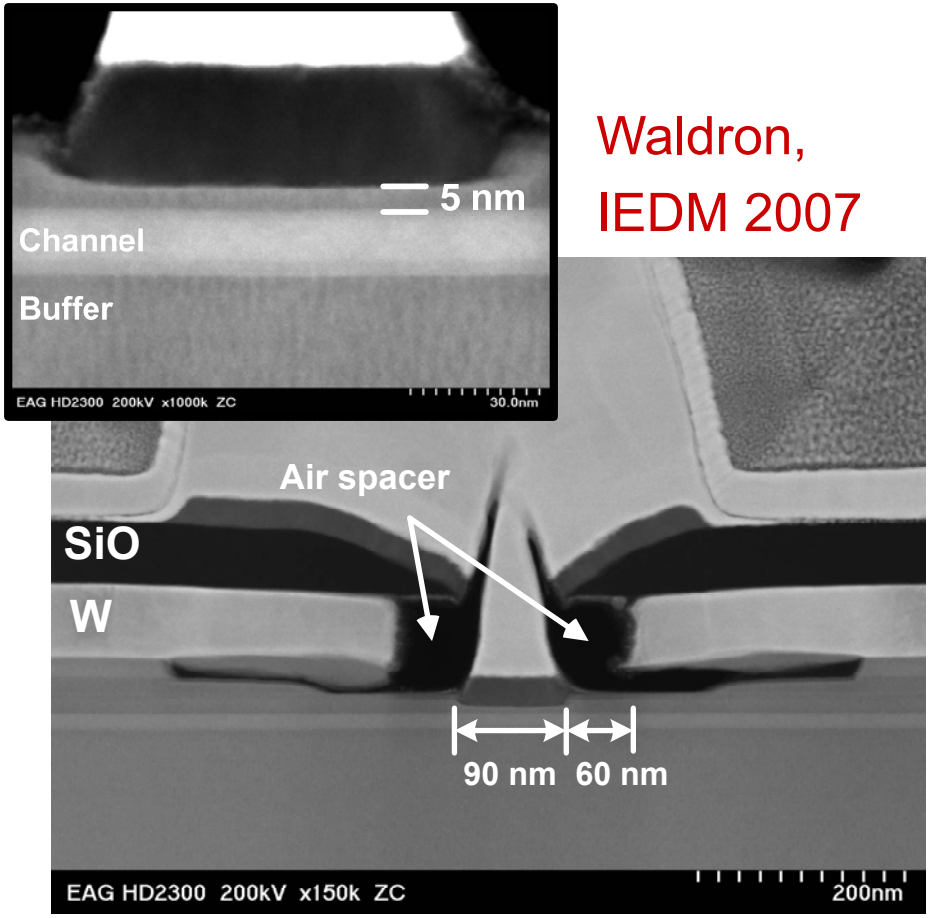


http://www.chipworks.com/uploadedImages/Intel_PMOS.bmp

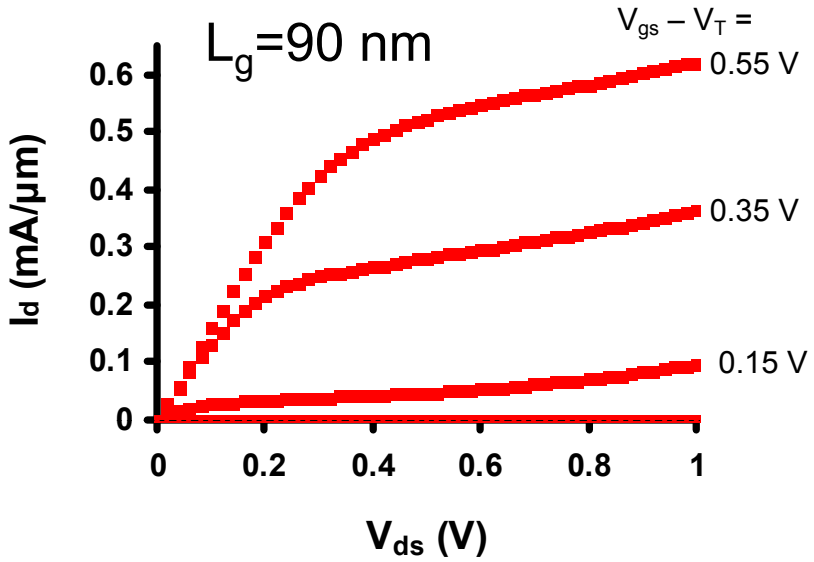
Some issues:

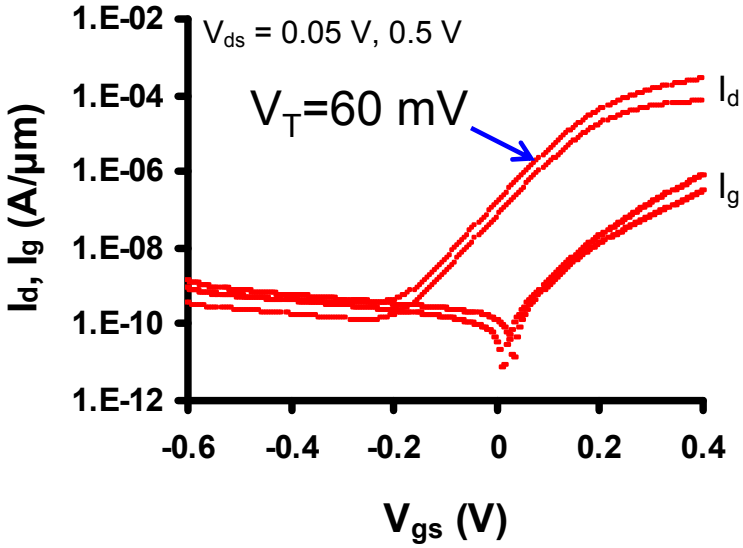
- Gate shape
- Big! [footprint 1000x too big]
- Non self-aligned contacts

Self-Aligned InGaAs HEMT



Waldron, IEDM 2007

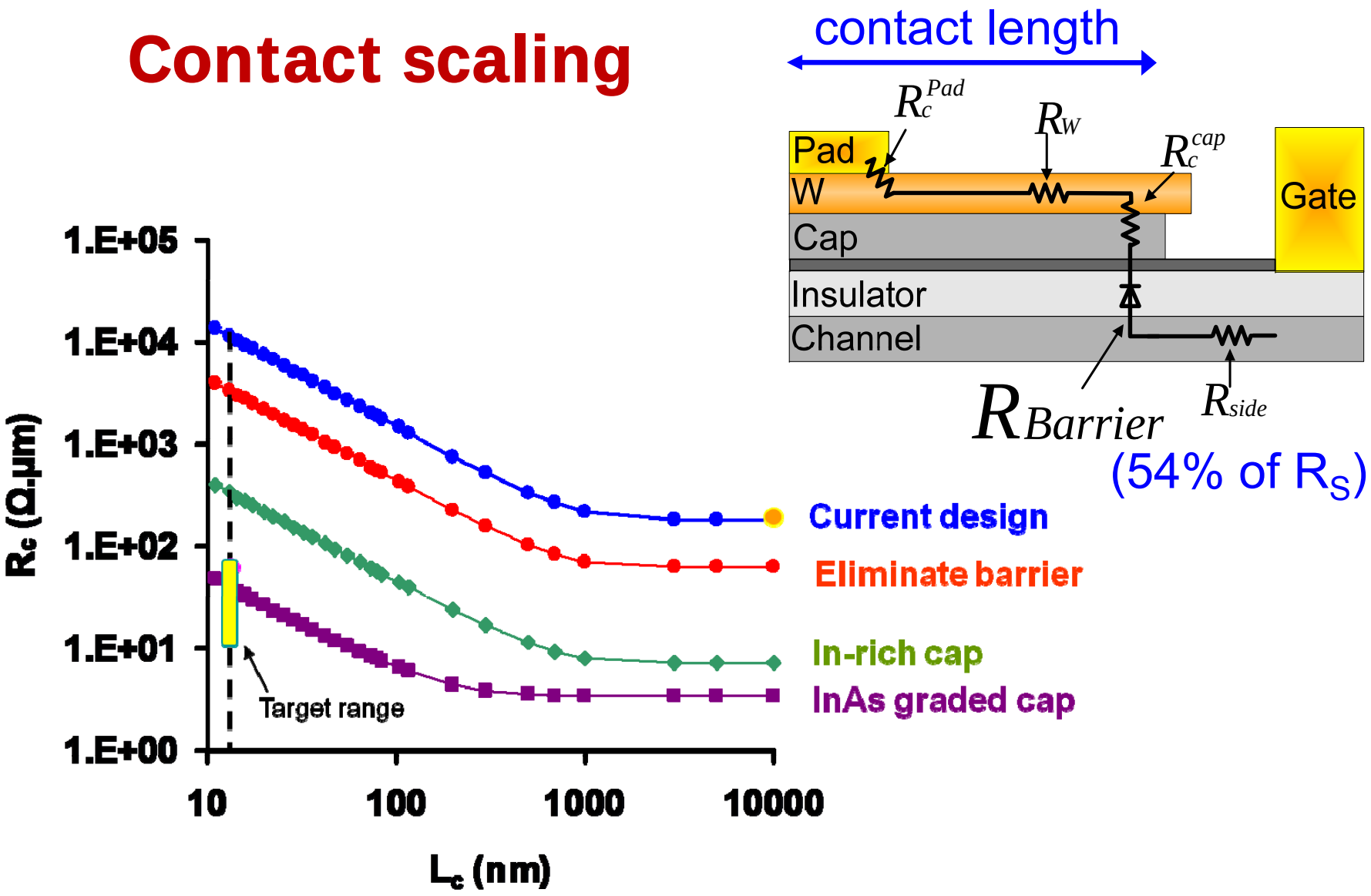




Self-aligned W non-alloyed ohmic contacts

DIBL=55 mV/V, SS=70 mV/dec, $I_{on}/I_{off}=8x10^4$, $R_S=0.24$ Ω.mm

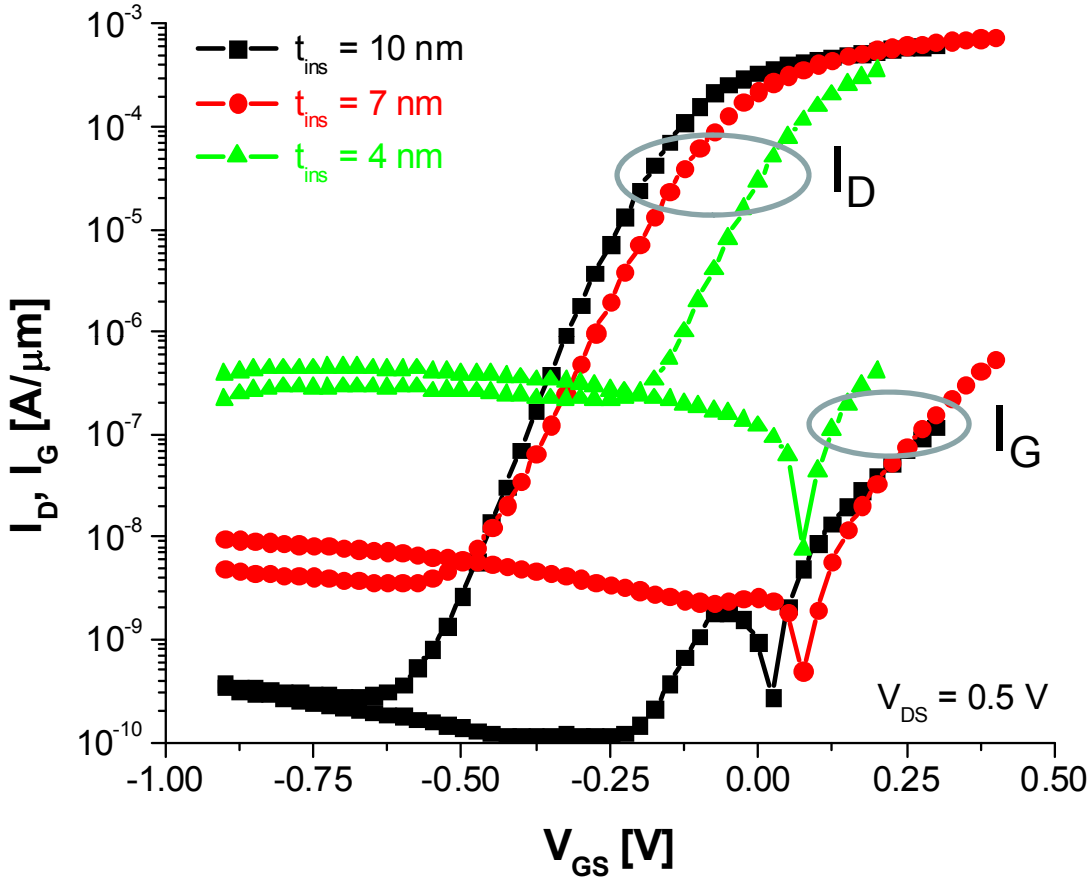
Contact scaling



To achieve target, need to eliminate barrier under contact

→ high-K gate dielectric required

High-K gate dielectric also required for t_{ins} scaling



L_g = 30 nm

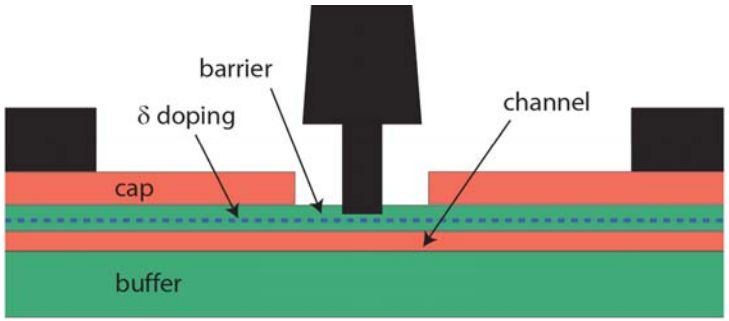
t_{ch} = 10 nm

L_{side} = 150 nm

$t_{ins} \downarrow \rightarrow I_G \uparrow$

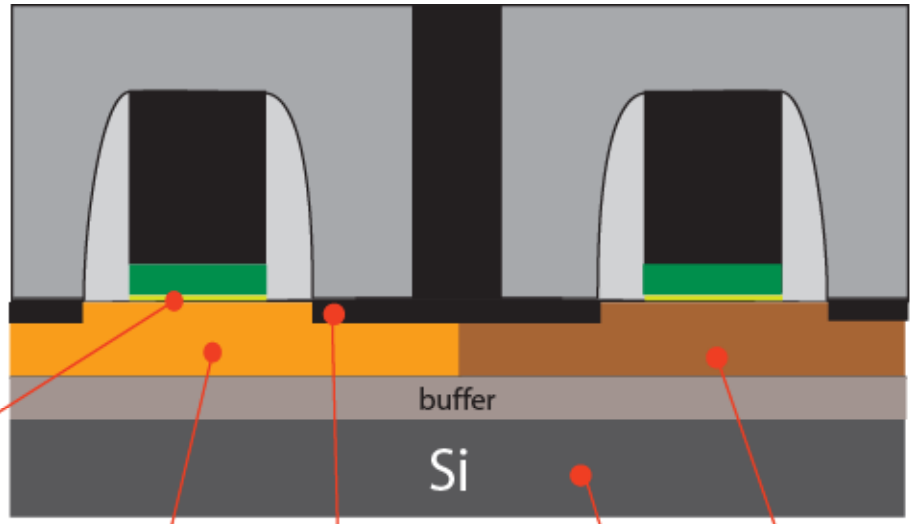
→ Further scaling requires high-K gate dielectric

From THz HEMT to III-V CMOS



Modern III-V HEMT

Future III-V CMOS



high-K dielectric gate insulator

III-V channel

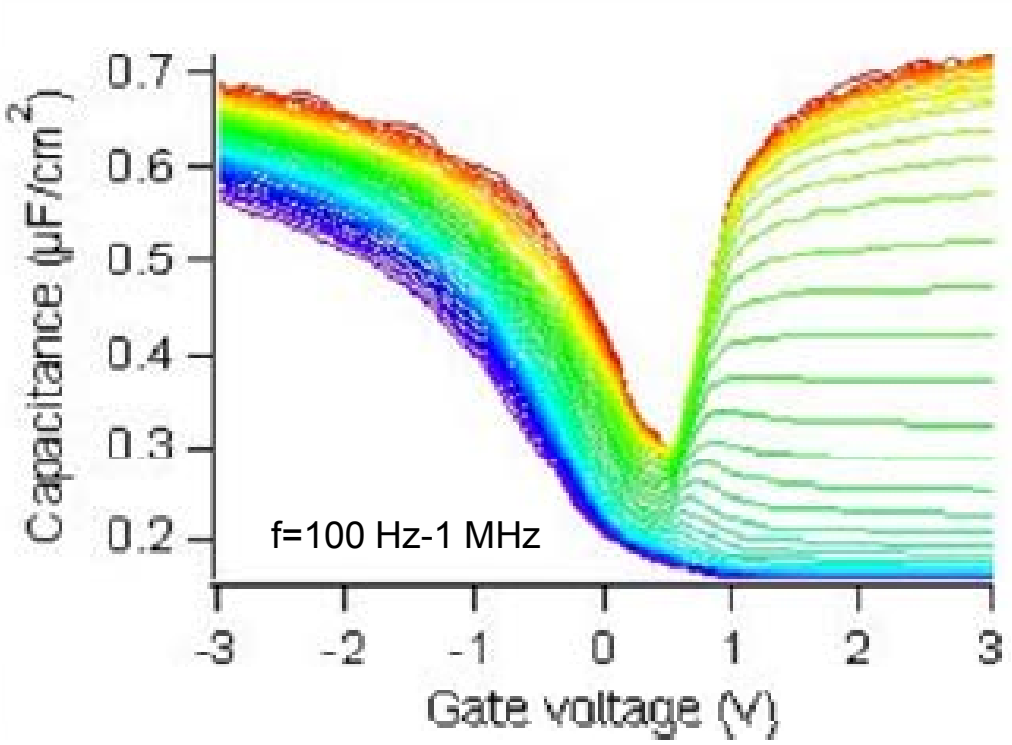
self-aligned ohmic contacts

large area Si substrate

p-type device

The High-K/III-V System by ALD

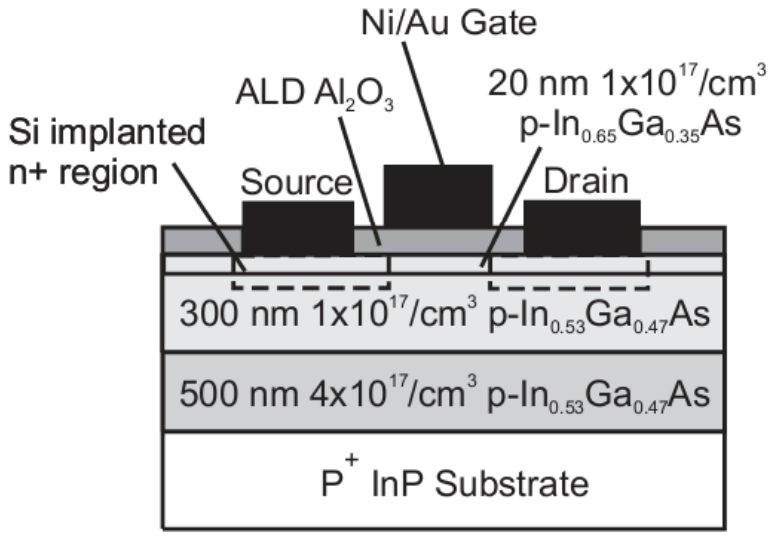
- *Ex-situ* ALD produces high-quality interface:
  - Surface inversion demonstrated on p-type InGaAs
  - D_{it} in mid ~10^{11} $cm^{-2}.eV^{-1}$ demonstrated

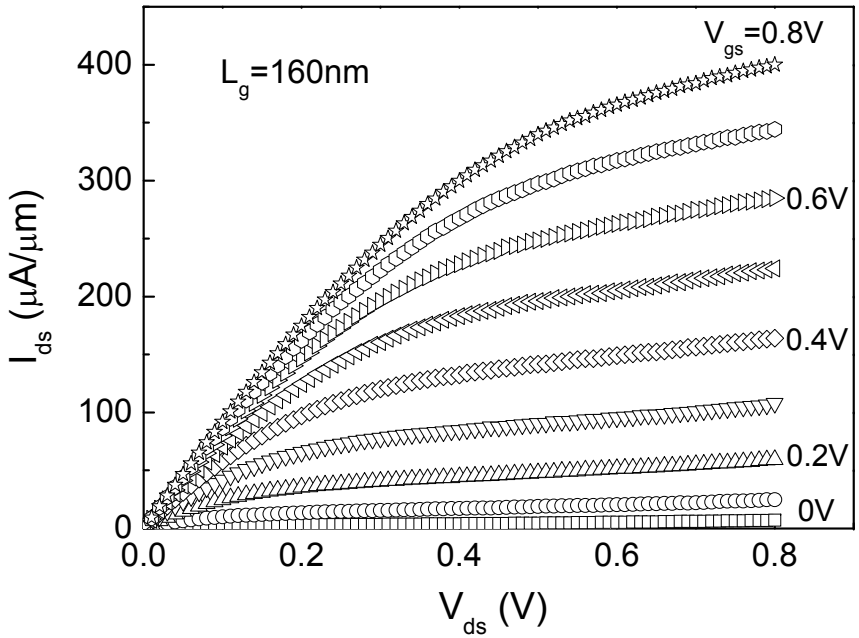


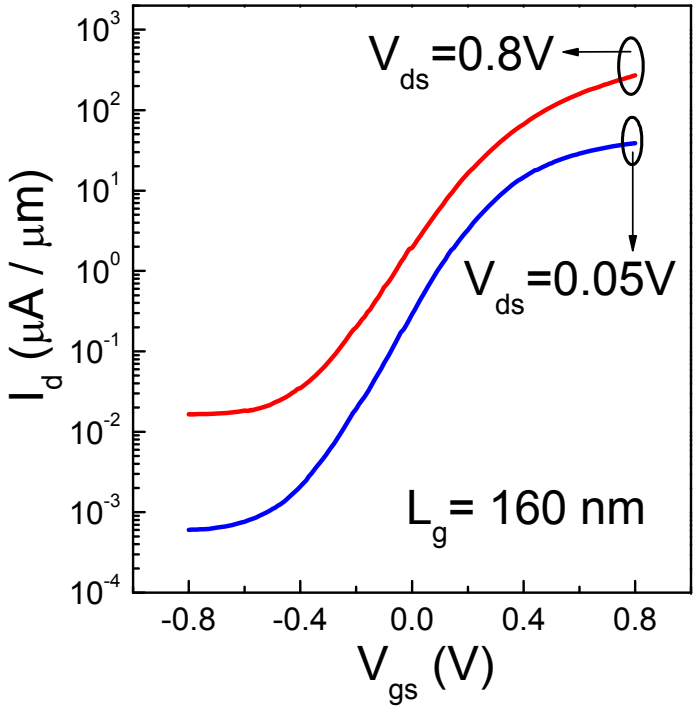
$Al_2O_3/In_{0.52}Ga_{0.47}As$

Lin, SISC 2008

Al_2O_3 / $In_{0.75}Ga_{0.25}As$ MOSFETs







For V_{dd}=0.8 V:

V_T=0.2V

I_d(ON)= 399 μA/μm

G_{mpk}= 633 μS/μm

I_{on}/I_{off}=1.6x10^3

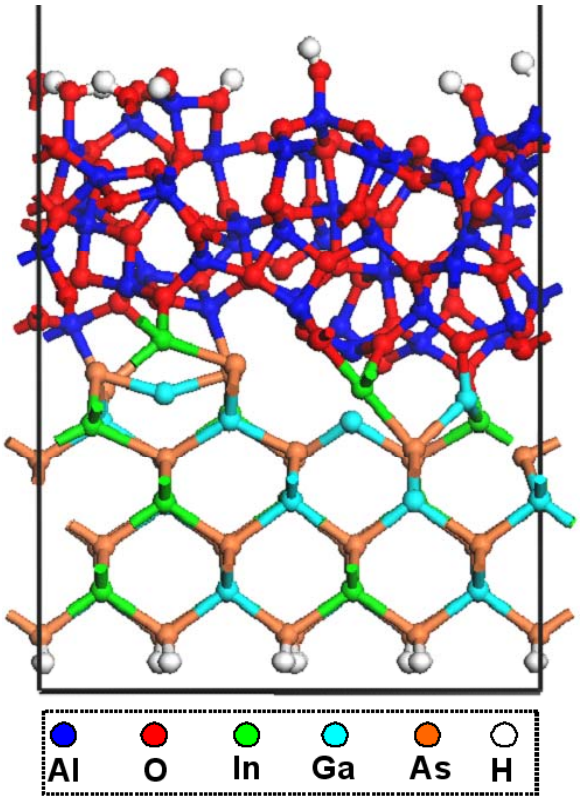
SS= 141 mV/dec

DIBL= 116 mV/V

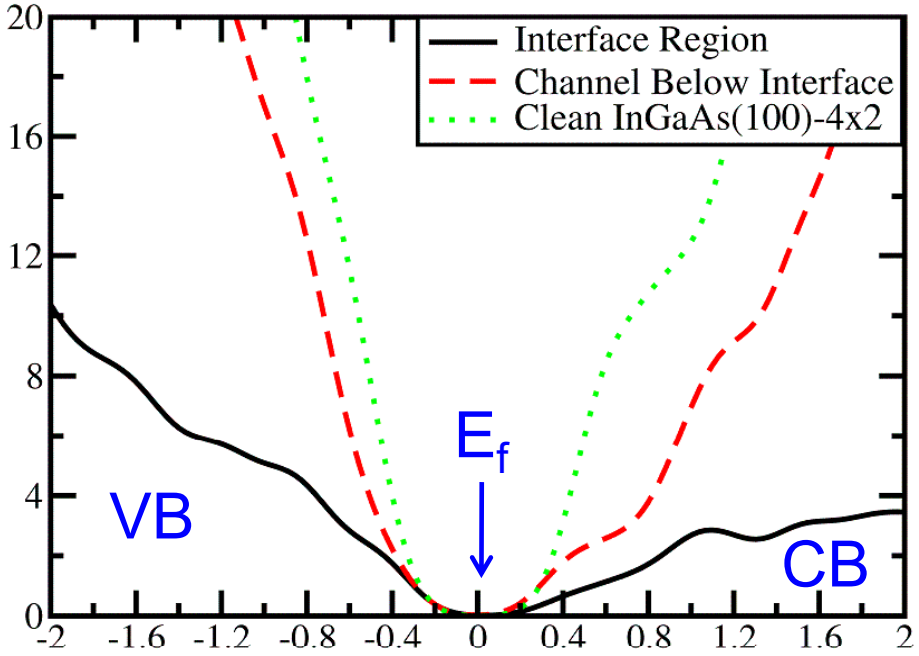
Wu, EDL 2009

The Al_2O_3 / InGaAs Interface

Density-Functional Theory Molecular Dynamics (DFT-MD) simulations show high quality Al_2O_3/InGaAs interface

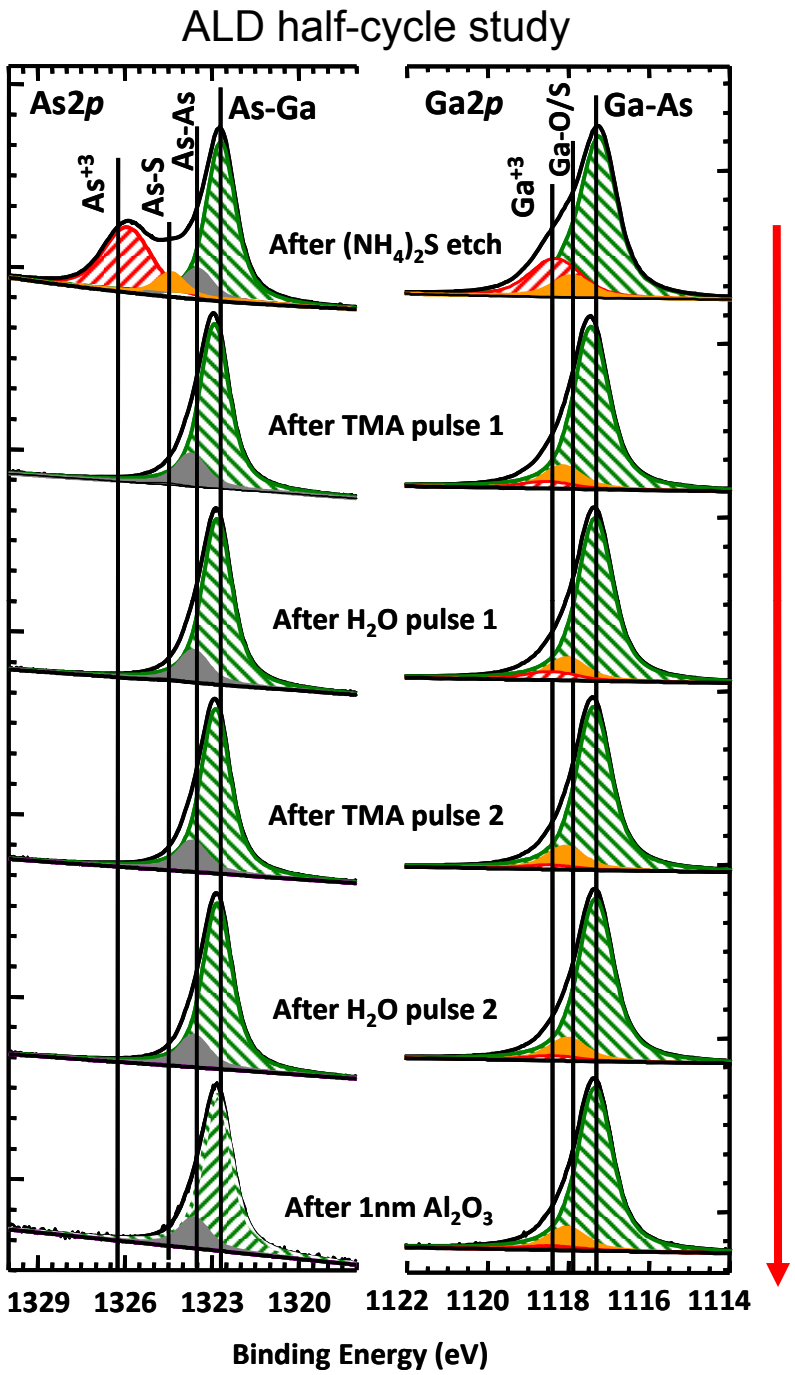


Low InGaAs lattice distortion



- No midgap states
- Fermi level midgap consistent with low interface dipole

Chagarov, Surf. Sci., in press



ALD "Clean-up" Effect

$Al_2O_3/In_{0.2}Ga_{0.8}As$

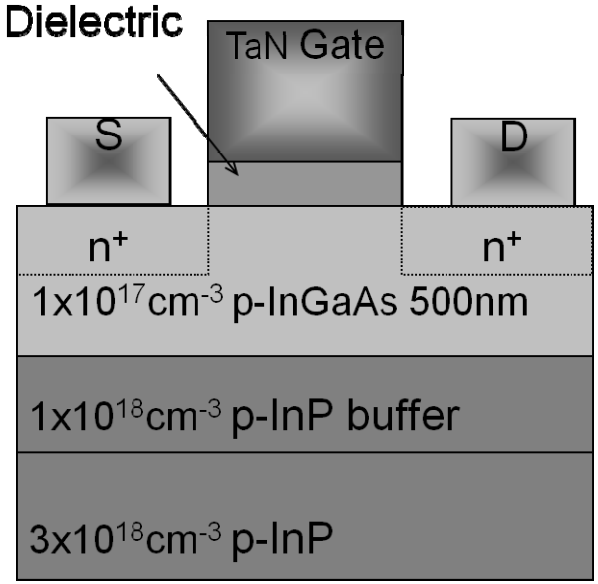
- Sample treated in $(NH_4)_2S$
- Precursors: TMA + H_2O
- In-situ XPS analysis

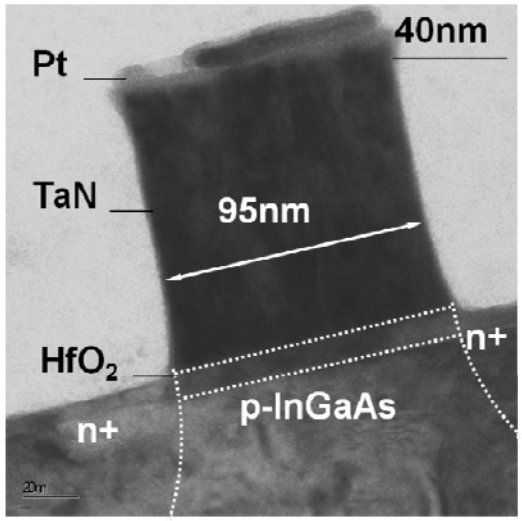
experiment evolution

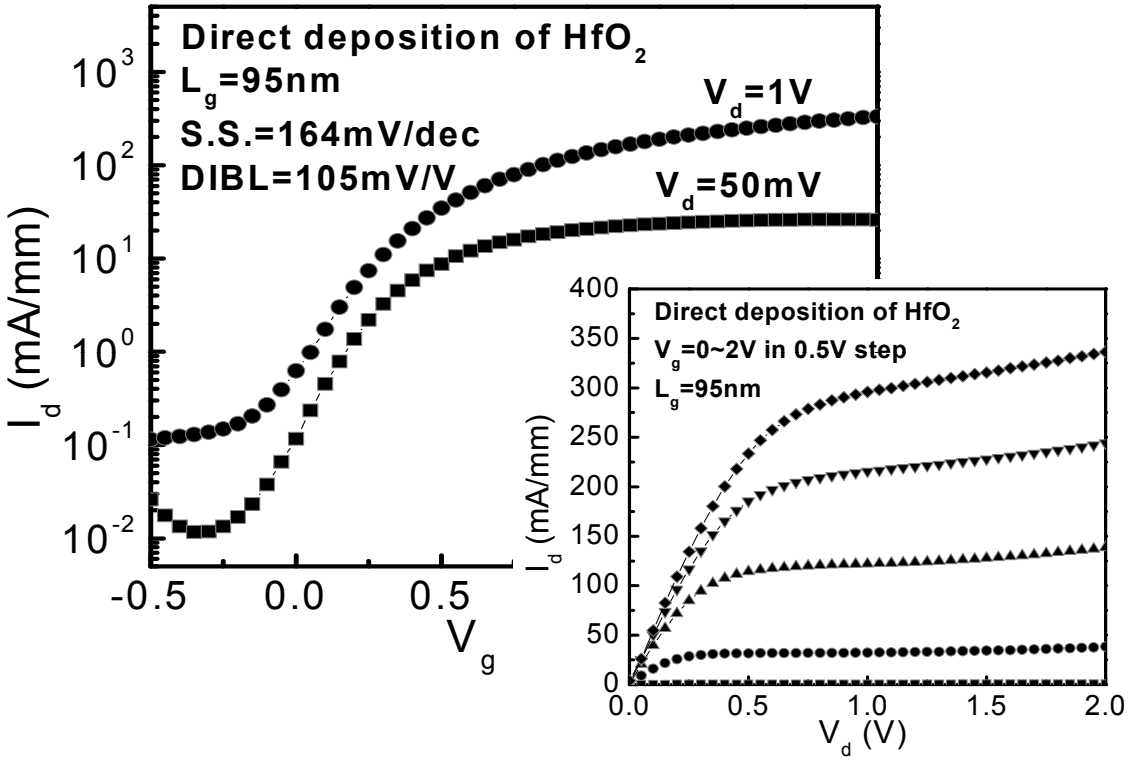
- Clean-up of all As oxides and reduction of Ga^{+3} oxides after first TMA pulse
- As-As bonding persistent

Milojevic, APL 2008

III-V MOSFET architecture 1: Implanted Self-Aligned MOSFET



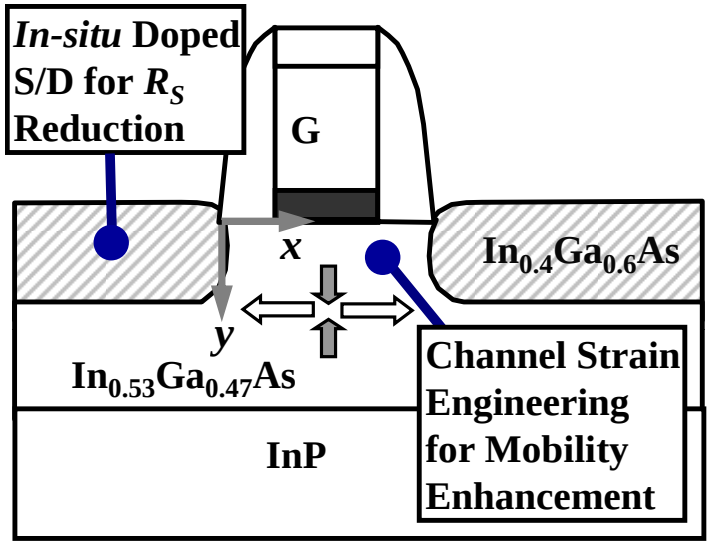


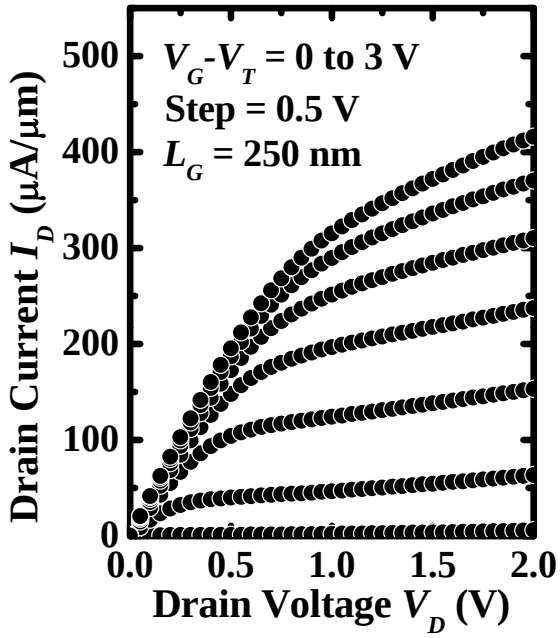


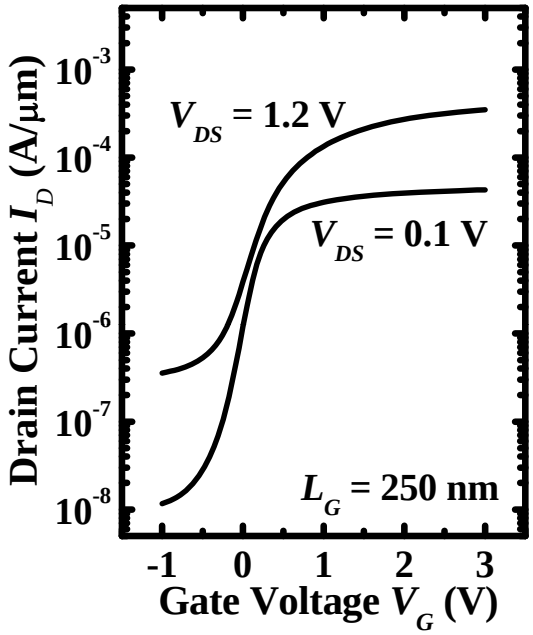
- 10 nm HfO_2 by MOCVD
- Si I/I + RTA 600 C, 60 s
- L_g=95 nm

Lin, IEDM 2008

III-V MOSFET architecture 2: MOSFET with regrown ohmic contacts



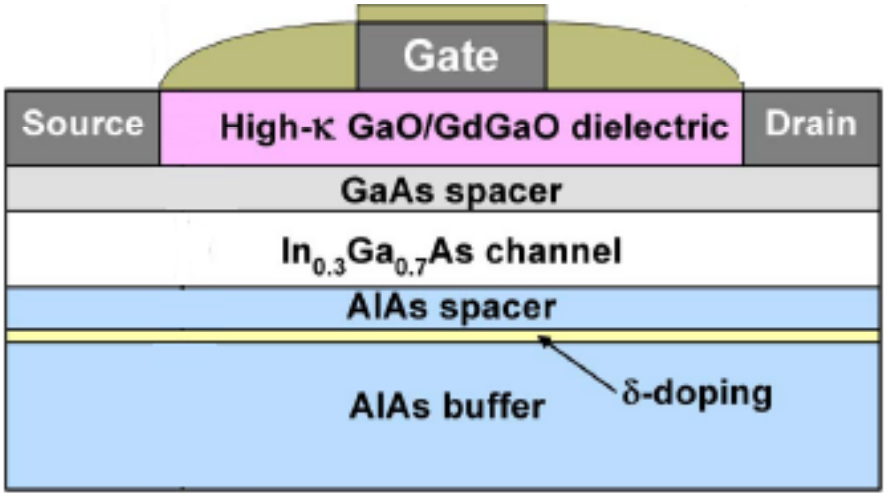


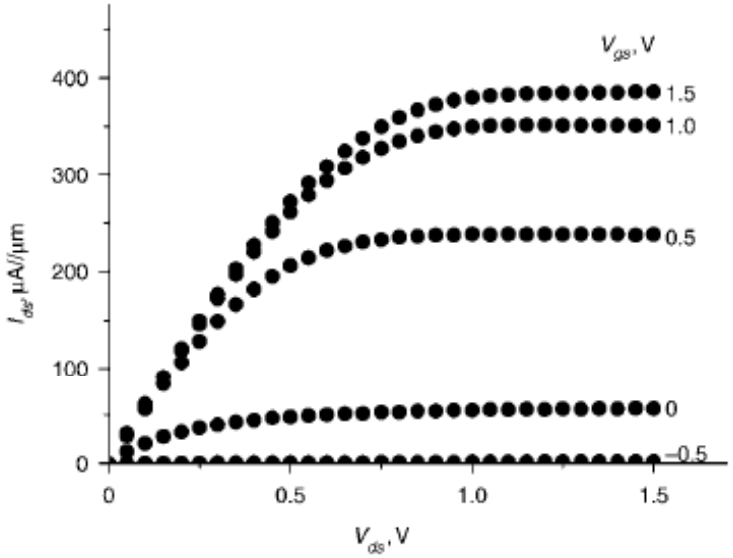


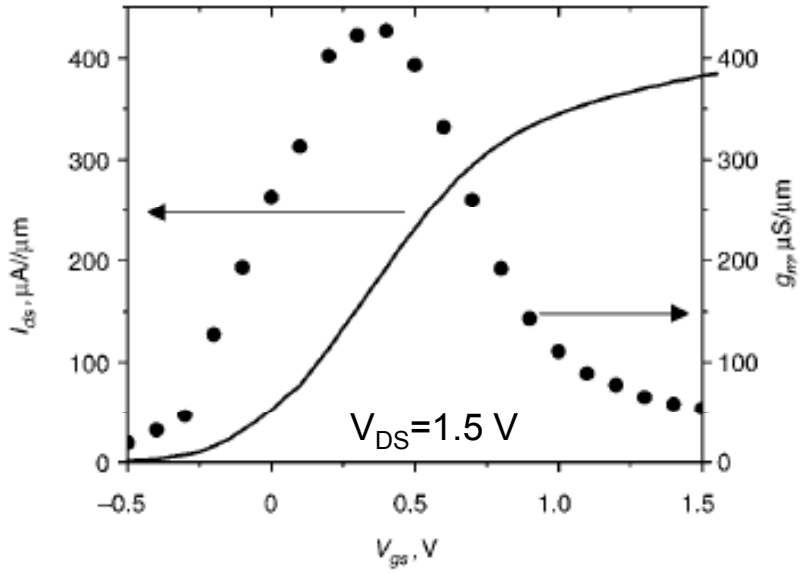
- 15 nm HfAlO by MOCVD
- TaN gate, SiON spacers
- In-situ Si doped InGaAs S/D by MOCVD (635 C, 2 min)
- L_g=250 nm

Chin, EDL 2009

III-V MOSFET architecture 3: Implant-free gate-last MOSFET







- 10 nm GGO by MBE
- 5 nm AlGaAs/GaAs barrier
- 10 nm $In_{0.3}Ga_{0.7}As$ channel
- Pt/Au gate
- L_g=180 nm

Hill, EL 2007

Worries…

- Can we make 15 nm-class III-V MOSFETs with higher performance than equivalent Si devices?
- What are we going to do about the p-type devices?
- Will III-V MOSFETs be reliable?
- Will III-V CMOS be ready on time?

Conclusions

- III-Vs attractive for CMOS
- III-V CMOS will strongly leverage Si

  → rather than “beyond Silicon”, a III-V channel will be an *add-on to Si technology* (as Cu, strain and high-K dielectrics have been in the past)
- Great challenges ahead:
  - Growth of III-V heterostructures on Si with thin buffer layers
  - Stable and reliable high-K/III-V interface with high interfacial quality
  - Nanometer-scale, self-aligned, E-mode FET architecture
  - High quality p-channel device