Hydrogen Sensitivity of InP HEMTs With WSiN-Based Gate Stack

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***Abstract*—We have experimentally investigated the hydrogen sensitivity of InP high-electron mobility transistors (HEMTs) with a WSiN–Ti–Pt–Au gate stack. We have found that exposure to hydrogen produces a shift in the threshold voltage of these devices that is one order of magnitude smaller than published data on conventional Ti–Pt–Au gate HEMTs. We have studied this markedly improved reliability through a set of quasi-two–dimensional mechanical and electrostatic simulations. These showed that there are two main causes for the improvement of the hydrogen sensitivity. First, the separation of the Ti-layer from the semiconductor by a thick WSiN layer significantly reduces the stress in the heterostructure underneath the gate. Additionally, the relatively thinner heterostructure used in this study and the presence of an InP etch-stop layer with a small piezoelectric constant underneath the gate reduces the amount of threshold voltage shift that is caused by the mechanical stress.**

***Index Terms*—High-electron mobility transistors (HEMTs), hydrogen, InP, piezoelectric effect, reliability.**

I. Introduction

THE goal of this paper is to study the hydrogen (H) sensitivity of state-of-the-art InAlAs–InGaAs high-electron mobility transistors (HEMTs) specifically designed for ultra-high speed optical fiber communication systems [1]. H degradation has been identified as a reliability concern in III-V MESFETs [2] and HEMTs [3]. H is known to alter the electrical characteristics of these devices ultimately leading to parametric failure. One of the paths through which H affects III-V FETs is the formation of TiH_x in the Ti–Pt–Au gate stack [4]. This creates tensile stress in the heterostructure underneath which, through the piezoelectric effect, causes a threshold voltage shift.

In state-of-the-art InP HEMTs with Ti-based gate stack, H-induced threshold voltage shifts can be as large as 150 mV depending on the gate length and the exposure conditions [6]–[10]. Since the Ti-layer is believed to be the source of the stress, the introduction of other metal such as WSiN at the bottom of the gate stack is expected to mitigate H sensitivity by separating the Ti-layer from the heterostructure. However, to date, no data have been reported that can test this hypothesis. The goal of this paper is to study the H sensitivity of InP HEMTs with a WSiN–Ti–Pt–Au gate stack [1] and to compare it to that of more conventional Ti–Pt–Au gate stack designs. The work presented in this paper is an updated and expanded version of preliminary results in [5].

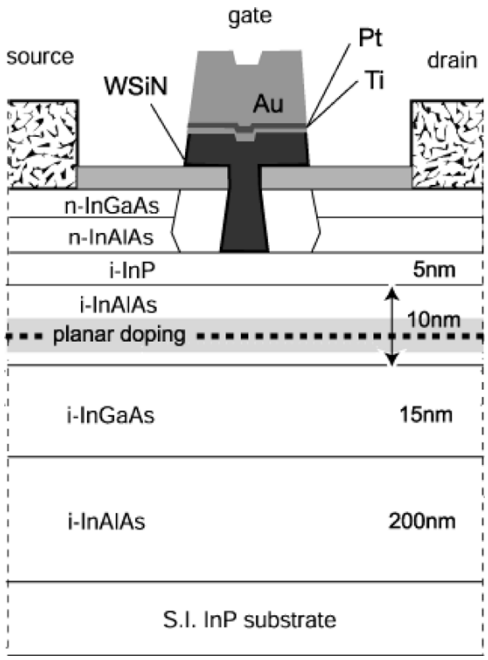

Fig. 1. Cross section of InP HEMT studied in this paper [1], [11].

II. Experiments

A cross section of the investigated InP HEMTs is shown in Fig. 1. The active device structure consists, from top to bottom, of a 5-nm InP etch stop, a 10-nm InAlAs insulator with Si planar doping, a 15-nm InGaAs channel, and a 200-nm InAlAs buffer layer [11]. The layers in the heterostructure are significantly thinner than previously studied devices that did not feature the InP etch stop [6]. In contrast with conventional InP HEMTs, these devices feature a WSiN–Ti–Pt–Au gate stack and an InP gate recess etch-stop layer in the intrinsic heterostructure [1]. The WSiN layer is 100 nm thick and is introduced to enhance the thermal reliability of the devices [11]. The InP etch stopper enhances device manufacturability.

In studying the H sensitivity of these devices, we have followed a methodology similar to that of [4]. The test devices were part of small test chips that contained devices of different gate lengths. The experiments basically consist of three phases. First, the devices were baked in N_2 at 195 °C for over 60 h to

Manuscript received May 18, 2004; revised December 9, 2004. This work was supported in part by Nippon Telegraph and Telephone Corporation (NTT) and in part by Triquint. The Massachusetts Institute of Technology portion of this work was supported in part by Nippon Telegraph and Telephone Corporation. The review of this paper was arranged by Editor A. Mehdi.

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Digital Object Identifier 10.1109/TED.2005.843871

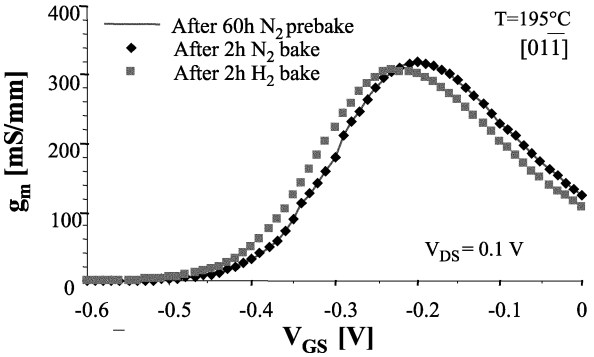

Fig. 2. Room-temperature transfer characteristics of a 0.1 μm InP HEMT with a $[01\bar{1}]$ gate orientation after 60-h prebake in N_2 at 195 °C, after a subsequent 2-h bake in N_2 at 195 °C and after another 2-h bake in forming gas at 195 °C ($V_{\rm DS} = 0.1$ V).

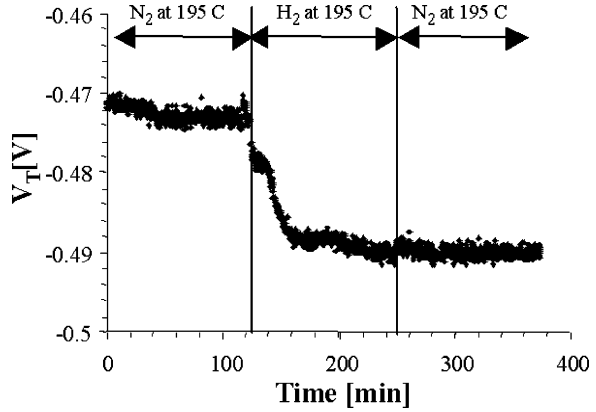

Fig. 3. Time evolution of V_T during a typical experiment ($T = 195$ °C). The device has a 0.1-μm gate length and a $[01\bar{1}]$ gate orientation.

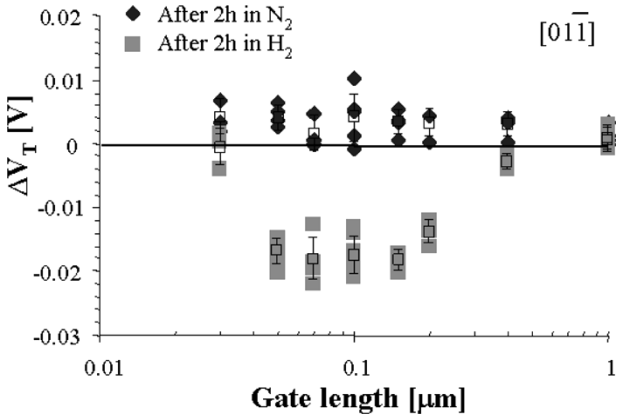

Fig. 4. Threshold voltage shifts caused by a 2-h bake at 195 °C in N_2 and in forming gas as a function of gate length. The means and standard deviations of the measurement are added to the figure. The devices have a $[01\bar{1}]$ gate orientation.

saturate all thermally induced effects in a Blue M OV-12A oven. The next two phases took place in a Cascade Microtech Summit 9600 thermal probe station, which allows for measurements in a controlled atmosphere and at different temperatures. In a second phase, the thermal stability was evaluated by baking the devices again at 195 °C for 2 h under N_2. Finally, the devices are baked again at 195 °C for 2 h [4] in forming gas (5% $H_2/95\%$ N_2). This third step is where hydrogen degradation takes place. This methodology allows us to compare the effects of a 2-h thermal bake in N_2 and H_2 in the same device and thus isolate even small H effects from a background of unrelated thermal effects. In separate experiments, a few devices were monitored *in situ* during the N_2 and H_2 anneals (threshold voltage V_T was measured at regular intervals at 195 °C). In some cases, after the forming gas bake, we evaluated the effect of a 2-h recovery anneal in N_2 at 195 °C.

Device characterization was carried out at room temperature before and after all three phases with a HP4155 semiconductor parameter analyzer. For this purpose, we developed a rather "benign" device characterization test suite that does not affect the device characteristics. This characterization suite involves measurements of the parasitic resistances, the output, transfer, and subthreshold characteristics and the threshold voltage. The measurements and figure-of-merit extraction are controlled by a PC and use a fixed probe configuration. Most of the emphasis in this paper has been placed on the threshold voltage which is defined at a drain-to-source voltage $V_{\rm DS} = 0.1$ V and a drain current $I_D = 1$ mA/mm above leakage.

The studied devices had gate lengths between 30 nm and 1 μm [1]. The devices have been designed and optimized for the $[01\bar{1}]$ gate orientation, but there were also devices along the [011] direction. Fig. 2 shows the room-temperature transfer characteristics in the linear regime of a 0.1-μm device with a $[01\bar{1}]$ orientation after 60-h pre-bake in N_2 at 195 °C and after subsequent 2-h bakes in N_2 or H_2 at 195 °C. The effect of H exposure is mostly a negative shift in V_T. In contrast, the additional 2-h bake in N_2 did not affect the device at all. This confirms that the 60-h bake in N_2 was enough to exhaust all thermal effects.

Fig. 3 shows the time evolution of V_T for a 0.1-μm InP HEMT with a $[01\bar{1}]$ gate orientation *in situ* during N_2 anneal, H_2 exposure and N_2 recovery at 195 °C. Before these anneals, the device was prebaked in N_2 for 60 h at 195 °C. This figure clearly shows that V_T shifts negatively during the forming gas anneal, while it is largely unaffected by the bakes in a N_2 atmosphere at the same temperature. Also, the impact of H_2 is basically saturated after about 50 min of exposure to forming gas. Furthermore, there is no indication of any recovery in a post-H exposure N_2 anneal. All devices were found to behave in this way under the studied conditions.

For the standard devices with a $[01\bar{1}]$ gate orientation, Fig. 4 shows the shift in the threshold voltage ΔV_T at room temperature as a function of the gate length for 33 devices. The 2-h N_2 treatment at 195 °C seems to shift V_T slightly positive. In contrast, the equivalent H_2 treatment causes a distinct and statistically significant negative ΔV_T, which is largest in magnitude for the 0.1-μm devices. Fig. 5 shows room-temperature ΔV_T in devices with a [011] gate orientation under identical conditions for 20 devices. Here, N_2 treatment also causes a small ΔV_T. The H_2 bake causes a negative shift with a gate length dependence that is almost a mirror image of that of Fig. 5, except that it is shifted by about -10 mV.

The maximum value of ΔV_T for short gate length devices that we have observed in any gate orientation is of the order of 15–20 mV. This is about an order of magnitude smaller than previous observations on InP HEMTs of this gate length under similar hydrogen exposure conditions [7]–[10]. This is a remarkable finding that bodes well for the long-term environmental reliability prospects of advanced InP HEMTs.

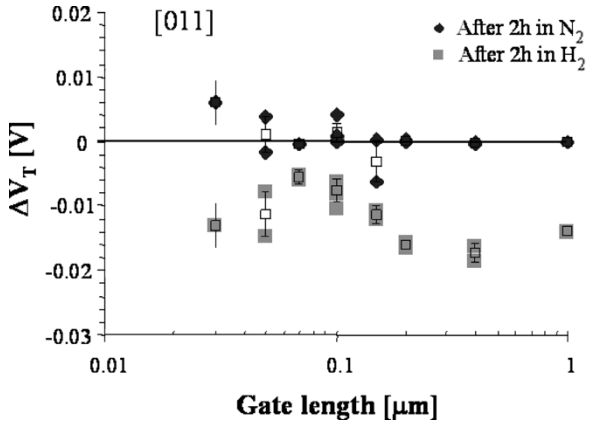

Fig. 5. Threshold voltage shifts caused by a bake at 195 °C in N_2 and in forming gas. The means and standard deviations of the measurement are added to the figure. The devices have a [011] gate orientation.

III. Simulation

In order to understand these results, we have carried out device simulations utilizing the techniques described in [6]. In essence, these involve two-dimensional (2-D) finite element simulations using ABAQUS and one-dimensional electrostatics calculations using MATLAB. In all, we studied four kinds of device structures.

1) To compare with [6], we first simulated a "reference" device with a standard Ti–Pt–Au gate stack and a layer structure consisting of 250-nm InAlAs–30 nm InGaAs–20nm InAlAs (from bottom to top) [6].
2) We then examined the impact of thinning the heterostructure to a layer structure consisting of 200-nm InAlAs–15-nm InGaAs–16-nm InAlAs. This is referred to as the "thinner heterostructure". It also uses a standard Ti–Pt–Au gate stack.
3) We next studied the effect of substituting 6 nm of the top InAlAs layer of the thinner heterostructure by a 6-nm InP etch stop layer [11]. This is referred to as "improved heterostructure."
4) Finally, we added a thick WSiN layer at the bottom of the gate stack.

The results of these simulations are shown in Fig. 6 for a [011] gate orientation. Identical results are predicted for the $[01\bar{1}]$ gate orientation, except for an opposite sign in ΔV_T.

Consistent with our measurements, we found that the InP HEMT with a WSiN-based gate-stack and an improved heterostructure exhibits a H sensitivity that is about an order of magnitude smaller than the reference device. This is shown in Fig. 6 which plots relative V_T shift as a function of the device structure for the four structures studied here. The data in this figure further reveal that there are two separate causes for the improved H sensitivity of WSiN-based InP HEMTs: The heterostructure itself and the introduction of the thick WSiN layer under the Ti. We have separately studied the effects of these changes on the H-induced ΔV_T.

Fig. 6 shows that by thinning the semiconductor structure from the reference device to the thinner heterostructure, ΔV_T is reduced by about 20%. As our model in [6] suggested, the threshold voltage shift is, to the first order, proportional to the depth of the channel multiplied by the difference between the

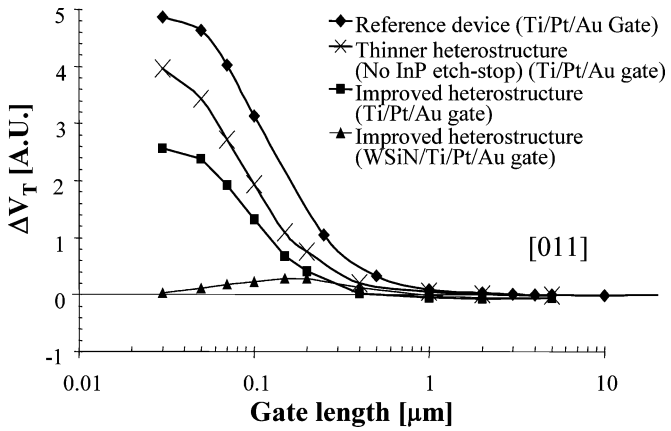

Fig. 6. Calculated ΔV_T versus gate length for: 1) reference structure with Ti–Pt–Au gate; 2) thinned heterostructure with Ti–Pt–Au gate; 3) improved heterostructure (including InP etch stop layer) with a Ti–Pt–Au gate and; 4) improved heterostructure with a WSiN–Ti–Pt–Au gate. Gate orientation is [011].

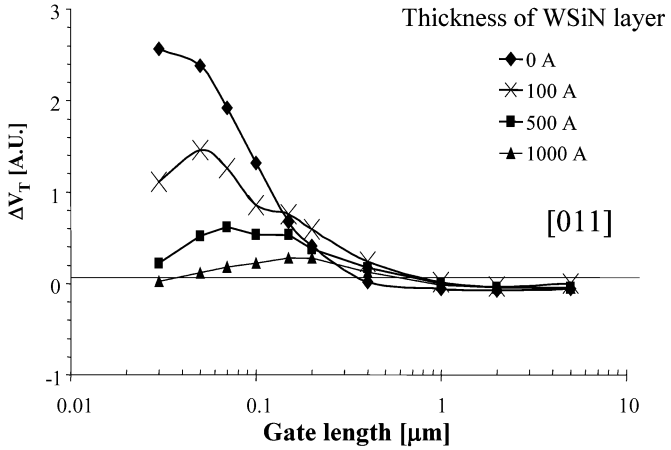

Fig. 7. Calculated ΔV_T versus gate length for InP HEMTs with the improved heterostructure with a WSiN–Ti–Pt–Au gate for different thicknesses of the WSiN layer (0, 10, 50, and 100 nm). Gate orientation is [011].

average piezoelectric field above the channel and in the buffer. Bringing the channel closer to the surface, therefore, should reduce ΔV_T, as is observed in the simulations.

The introduction of the 6-nm InP etch-stop layer, which has a very low piezoelectric constant, additionally reduces ΔV_T by another 35%. This causes a decrease of the average piezoelectric field in the channel and the insulator. We find that with these two changes the improved heterostructure exhibits a decrease in H sensitivity to lower than 50% at short gate lengths when compared with the reference device.

The presence of the thick WSiN layer in the gate stack further lowers the H sensitivity to about 30% at a gate length of 0.1 μm and even lower at shorter gate lengths. This is shown in Fig. 6. Our simulations suggest that this is because the WSiN layer absorbs a large part of the stress caused by the expanding Ti-layer. This yields a reduction of the mechanical stress that affects the semiconductor by the same amount, causing a proportional reduction of the piezoelectric polarization in the semiconductor, and thus in ΔV_T.

From our simulations, we have found that a thicker WSiN layer reduces ΔV_T by a greater amount. This is shown in Fig. 7 which plots ΔV_T as a function of gate length for different thicknesses of WSiN layer. At short gate lengths, inserting the WSiN

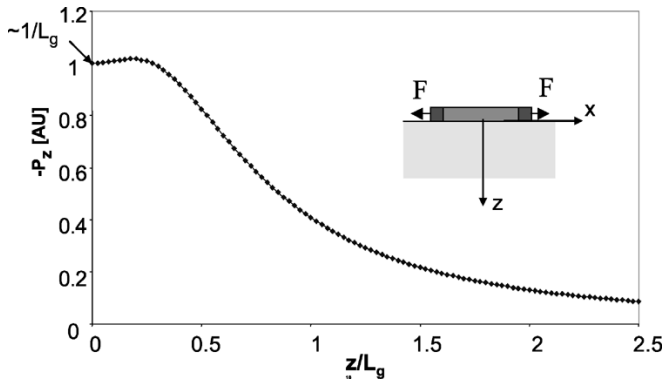

Fig. 8. Calculated $-P_z$ as a function of depth into the semiconductor at the center of the gate according to the model of Blech and Meieran [12]. The depth scales proportionally with L_g, while $-P_z(x = 0, z = 0)$ scales inversely proportional with L_g.

layer reduces the overall magnitude of ΔV_T. Interestingly, the evolution of ΔV_T with gate length changes character upon the introduction of the WSiN layer. In devices with the conventional gate stack, ΔV_T monotonically increases as the gate length decreases. In the devices containing WSiN in the gate stack, ΔV_T peaks at a certain gate length and then is reduced for shorter devices. This is consistent with experimental observations. This behavior is understood through the simple model that is described in the next section.

IV. Discussion

As seen in the previous section, InP HEMTs with a WSiN–Ti–Pt–Au gate show a maximum ΔV_T at a certain gate length (L_g). The peak ΔV_T occurs at a longer L_g for thicker WSiN. This gate length dependence is different from that of a conventional gate stack in which the expanding Ti layer is in direct contact to the semiconductor. In this later case, reducing the gate length results in an increase in ΔV_T. However, the peculiar dependence observed here for the WSiN–Ti–Pt–Au gate HEMTs can be fully explained from the physical understanding of the H-induced ΔV_T mechanism described in [6] coupled with a simple analytical model of the stress distribution in the semiconductor induced by an expanding layer.

Blech and Meieran developed a simple 2-D analytical model for the stress induced by an infinitely thin expanding film of finite length on an underlying semi-infinite elastic solid [12]. The stress exerted by the thin film on the underlying solid is modeled as being induced by two incremental forces acting at the two edges of the film. This is sketched in the inset of Fig. 8. The model predicts that the displacement parallel to the length of the film u_x at a distance x from the center of the gate and at a depth z, is given by

$$u_x(x,z)=\frac{2F}{\pi E}\left[(1-\nu^2)\ln\left(\frac{\left(\frac{L_g}{2}+x\right)^2+z^2}{\left(\frac{L_g}{2}-x\right)^2+z^2}\right)+(1+\nu)(3-4\nu)\times\left[\left(\frac{\left(\frac{L_g}{2}+x\right)^2}{\left(\frac{L_g}{2}+x\right)^2+z^2}\right)-\left(\frac{\left(\frac{L_g}{2}-x\right)^2}{\left(\frac{L_g}{2}-x\right)^2+z^2}\right)\right]\right] \quad (1)$$

where E is Young's modulus, ν is Poisson's constant and F is the force at the edge of the gate. In thin films, F is given by the product of the thickness of the film t and the stress in the film, σ

$$F = \sigma t. \quad (2)$$

From here, one can compute the z component of the polarization vector at the center of the gate, which is the input to our model for ΔV_T described in [6]. For a gate orientation parallel to the [011] orientation [13], P_z is given by

$$P_z(x,y) = -\frac{\mu d_{14}}{2}\frac{du_x}{dx}. \quad (3)$$

Hence, P_z at the center of the gate is

$$-P_z(x=0,z) = \frac{4F(1+\nu)\mu d_{14}}{L_g \pi E} \times\left[\frac{1-\nu}{\frac{1}{4}+\left(\frac{z}{L_g}\right)^2}+(3-4\nu)\frac{\left(\frac{z}{L_g}\right)^2}{\left(\frac{1}{4}+\left(\frac{z}{L_g}\right)^2\right)^2}\right]. \quad (4)$$

It is interesting to see that in this model, the depth dependence of the magnitude of the polarization vector appears normalized with L_g. Fig. 8 shows $-P_z(x = 0,\mathrm{z})$ as a function of z/L_g, as predicted by this model. The model also indicates that at the gate-semiconductor interface, $z = 0$, $-P_z(x = 0, z = 0)$ scales inversely proportional with L_g

$$-P_z(x=0,z=0) = \frac{16F(1+\nu)(1-\nu)\mu d_{14}}{L_g \pi E}. \quad (5)$$

This result is consistent with the evolution of ΔV_T with L_g observed experimentally and through 2-D simulations in TiPtAu conventional gates in which it is seen that ΔV_T increases in magnitude as the gate length shortens [6].

This simple formulation needs to be modified for gate stacks that include WSiN. In a case in which there is a WSiN layer of thickness, t, the heterostructure surface is placed at $z = t$. Hence, $-P_z$ at the heterostructure surface can be obtained by substituting $z = t$ in (4)

$$-P_z(x=0,z=t) = \frac{4F(1+\nu)\mu d_{14}}{L_g \pi E} \times\left[(1-\nu)\left(\frac{1}{\frac{1}{4}+\left(\frac{t}{L_g}\right)^2}\right)+(3-4\nu)\frac{\left(\frac{t}{L_g}\right)^2}{\left(\frac{1}{4}+\left(\frac{t}{L_g}\right)^2\right)^2}\right]. \quad (6)$$

This is what impacts ΔV_T. In long HEMTs, t is much smaller than L_g. Then, $-P_z(x = 0, z = t)$, and therefore the H-induced ΔV_T, depend weakly on t consistent with the model and results in [6], and [14]. This can be seen on Fig. 8.

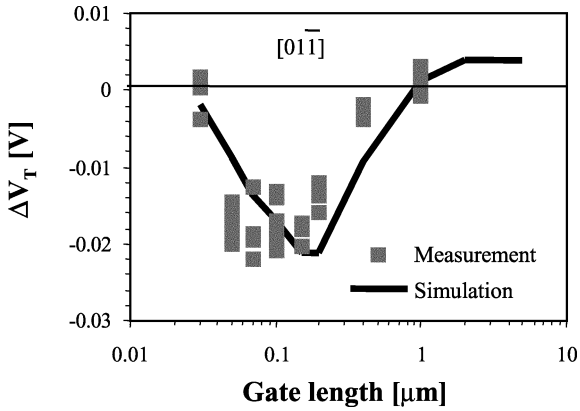

Fig. 9. Measured and simulated ΔV_T for the improved InP HEMTs with a WSiN-based gate stack and InP etch-stopper. Gate orientation is $[01\bar{1}]$.

When the thickness of the nonexpanding layer is larger than the gate length, $t/L_g \gg 0.5$, (6) can be approximated as

$$-P_z(x=0, z=t) \approx \frac{4F(1+\nu)\mu d_{14}}{\pi E}(4-5\nu)\frac{L_g}{t^2}. \quad (7)$$

In this short-gate length limit, $-P_z(x=0, z=t)$ scales as L_g/t^2.

In [6] we found that in short devices, ΔV_T scales proportional to $-P_z(x=0, z=t)$ and the gate length. Therefore, in the presence of a WSiN barrier layer of thickness t ΔV_T scales as L_g^2/t^2 in short devices. This is the result observed in the 2-D simulations in Fig. 7 for the devices with a thick WSiN layer in the gate stack and in the measurements in Fig. 4. The simple analytical model also explains why a thicker nonexpanding layer underneath the Ti layer reduces ΔV_T dramatically in short HEMTs and why ΔV_T peaks at gate lengths that depend on the thickness of the WSiN layer.

The simulated results shown in Fig. 6 for the advanced heterostructure with a WSiN gate can be compared to the experimental ones after appropriate scaling. This is shown in Fig. 9. Scaling is required because in the model, the simulated ΔV_T is linearly proportional to the magnitude of stress. However, the precise value of stress in the experiments is not known. Fig. 9 reveals excellent agreement between experimental and simulated results for the $[01\bar{1}]$ gate orientation. Interestingly, the simulations not only predict a large and negative ΔV_T centered around 0.1 μm, but a marked H insensitivity for 30-nm devices, just as observed in the experiments. When the gate length is significantly shorter than the thickness of the WSiN layer, the mechanical stress at the center of the gate is dramatically reduced.

By comparing Figs. 5 and 6 one sees that the shapes of the ΔV_T curves for the [011] and $[01\bar{1}]$ gate orientations are not exactly a mirror image of each another around the *x* axis. There appears to be a rigid shift of about -10 mV to the ΔV_T for the devices with a [011] gate orientation. This can not be explained by the framework presented here. For [011] oriented devices some other aspects of the device implementation come into play that are not understood and are not captured in the simulations.

The results presented in this paper are encouraging and important because they represent a device level solution to the reliability problems caused by the H-induced piezoelectric effect. Introducing WSiN or another suitable layer to the bottom of the gate stack can greatly mitigate this problem without requiring hermetic packages that are provided with hydrogen getterers.

V. Conclusion

We have found that InP HEMT designs with a WSiN layer at the bottom of the gate stack and InP etch-stop layers inside the intrinsic heterostructure feature a hydrogen sensitivity that is about one order of magnitude smaller than conventional InP HEMTs. This means the H-induced piezoelectric effect can be mitigated by suitable gate stack design. A simple model has been developed to explain the reduced hydrogen sensitivity of these devices for very short gate lengths.

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