Performance and Limitations of 65 nm CMOS for Integrated RF Power Applications

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Sponsors: IBM Faculty Award, IBM PhD Fellowship Program
Acknowledgements: Jack Pekarik

Outline

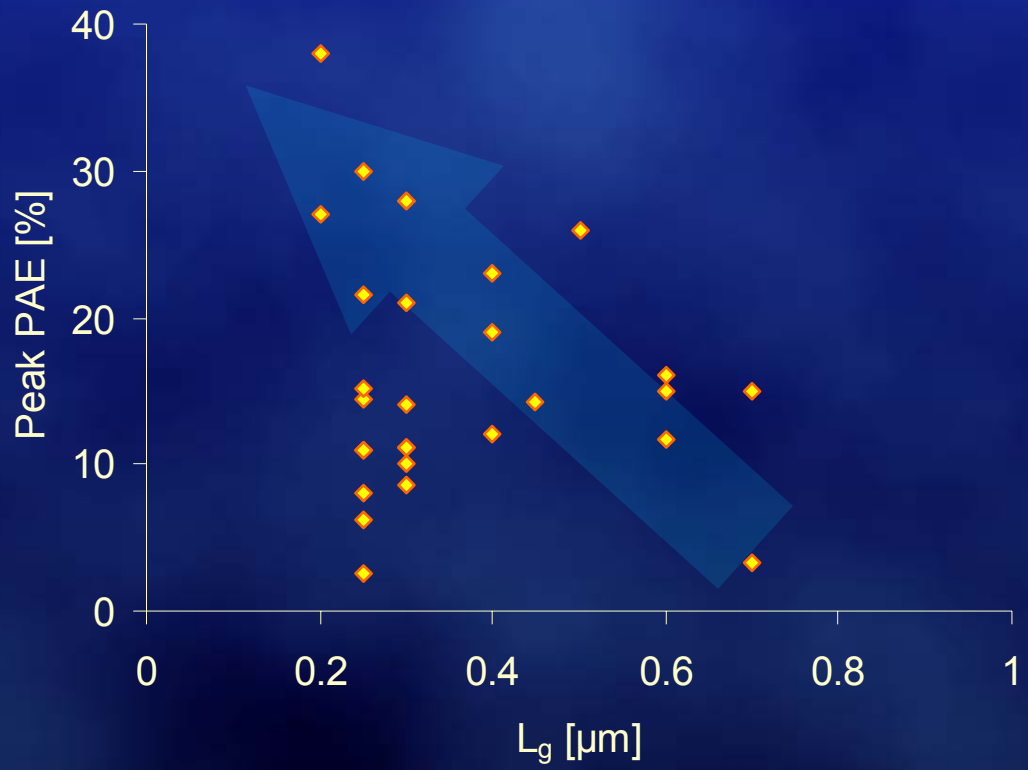
- **Why 65 nm CMOS for RF Power**
- Performance of Standard 65 nm Devices
- Output Power Scaling
- Optimizing Device Layout
- Comparison with 90 nm and 0.25 µm
- Conclusions

Why 65 nm CMOS for RF Power?

- System integration → 65 nm as a platform for digital
- High-volume, low cost consumer applications
  - Current: WLAN, Bluetooth, Cell-phone PA driver, WiMax / 802.16
- Moderate frequencies (2-10 GHz)
- Medium power (<100 mW)

Benefits of Scaling

- $L_g \downarrow \rightarrow f_t \uparrow f_{max} \uparrow \rightarrow$ Gain ↑ PAE ↑

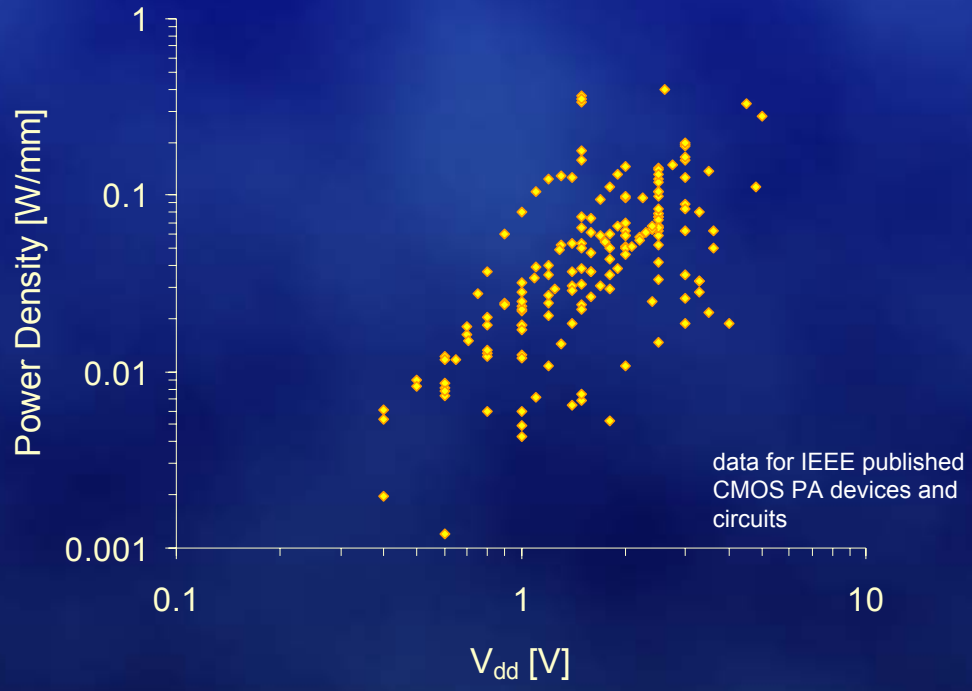


data for IEEE published GaAs MESFETs,
27 GHz < freq < 50 GHz

- 65 nm RF performance should benefit from scaling

Issues of CMOS for RF Power

- Concerns: CMOS Scaling → V_{dd} ↓ → P_{out} ↓



- Possible Solutions:
  - Raise V_{dd} ⇒ impact on reliability
  - Use I/O devices (if available) ⇒ process complexity (cost)
  - Increase device width

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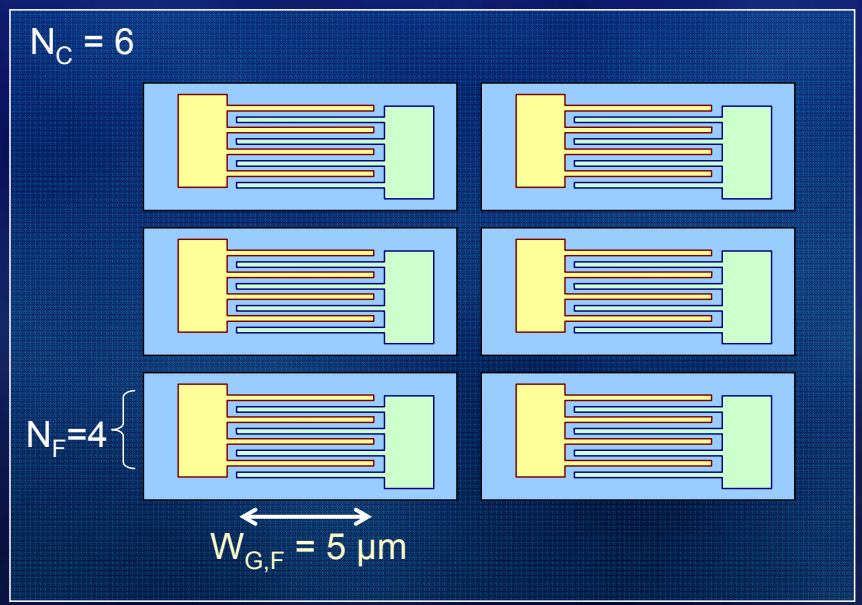
Experimental

- Devices designed and fabricated in IBM's 65 nm CMOS

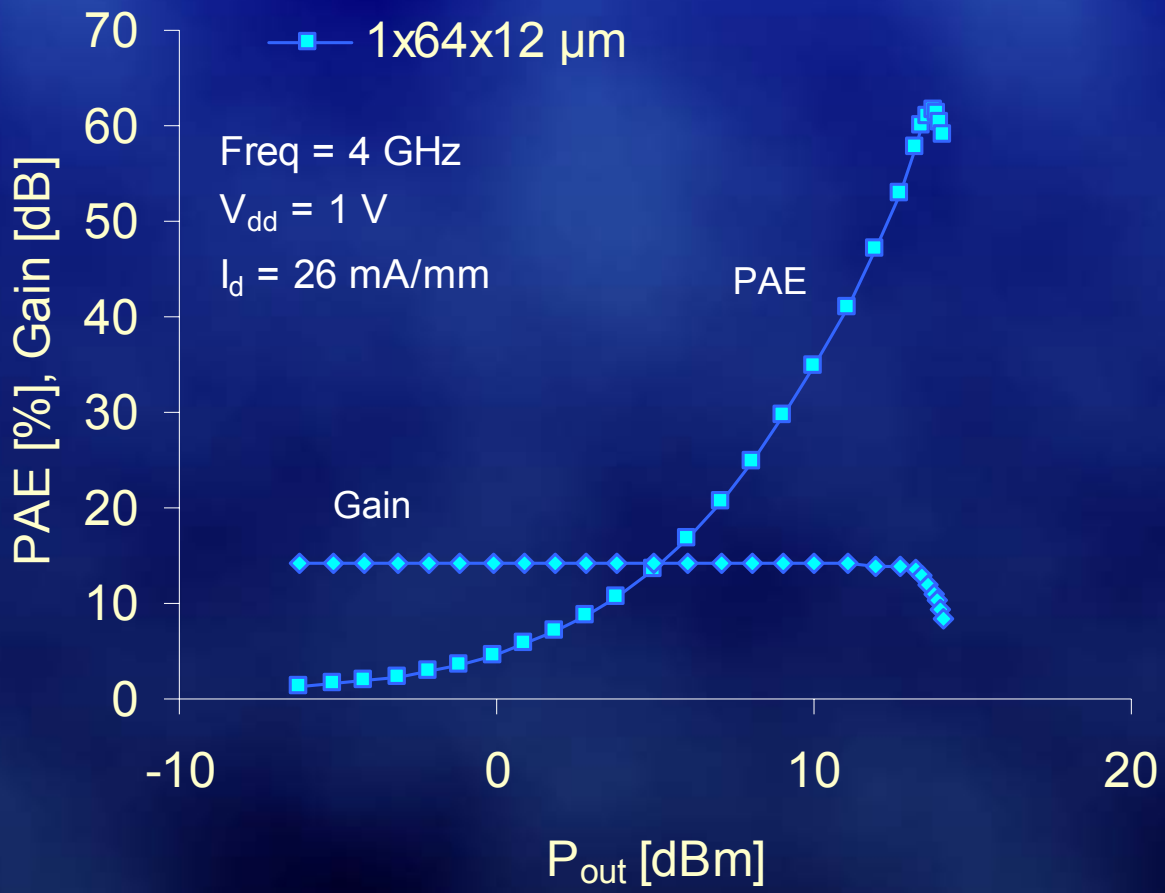
$W_{G,TOT} = N_C \times N_F \times W_{G,F}$

N_C = # of cells
N_F = # of fingers
$W_{G,F}$ = unit finger width



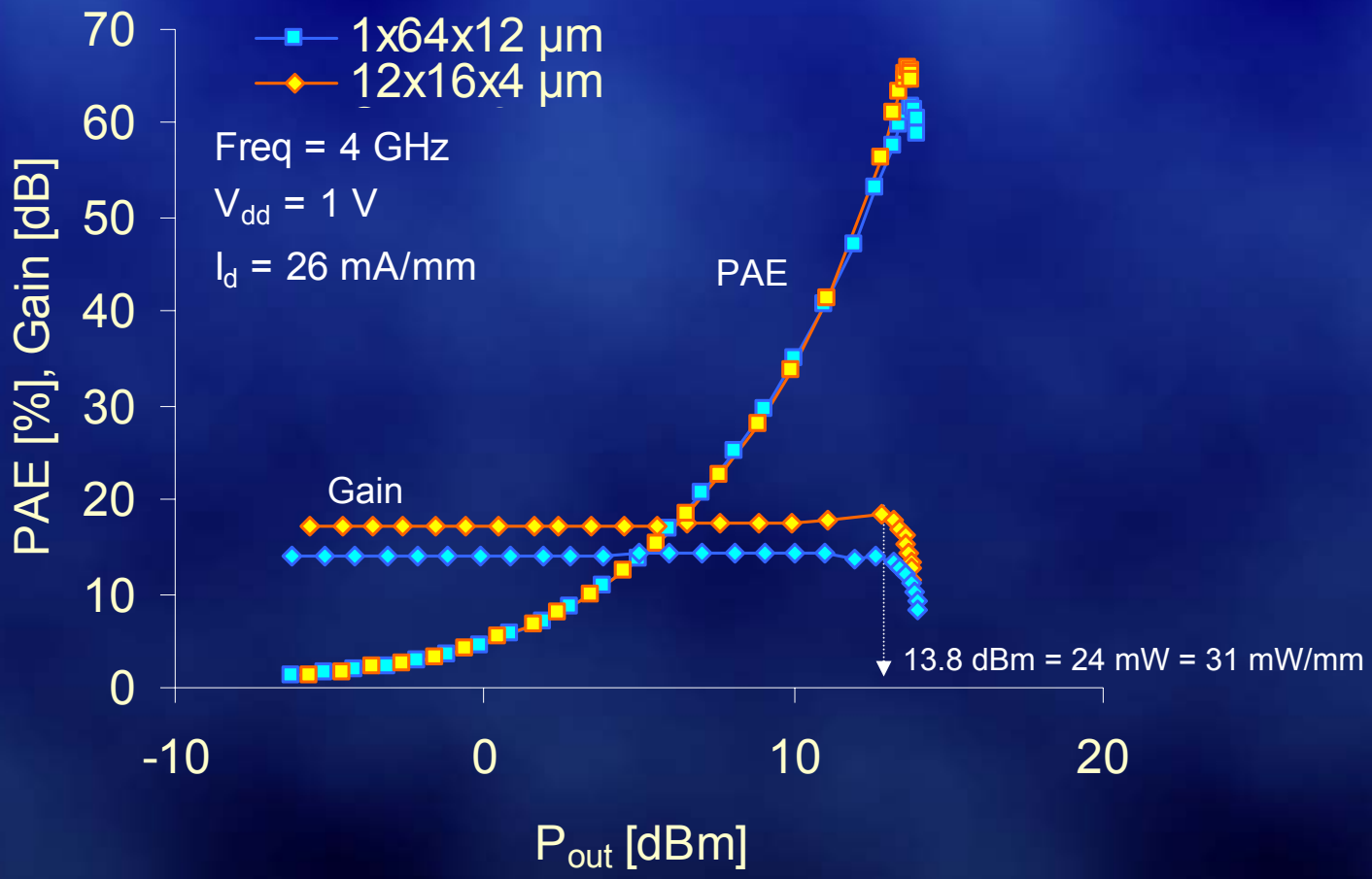
- Standard Device:
  - $W_{G,TOT}$ = 768 µm
  - $N_C \times N_F \times W_{G,F}$ = 1x64x12 µm
- Measurements:
  - Maury Load Pull System
  - 2-18 GHz

RF power performance of standard 65 nm devices



1x64x12 µm: Peak PAE = 62% at P_{out} = 13.8 dBm

RF power performance of standard 65 nm devices



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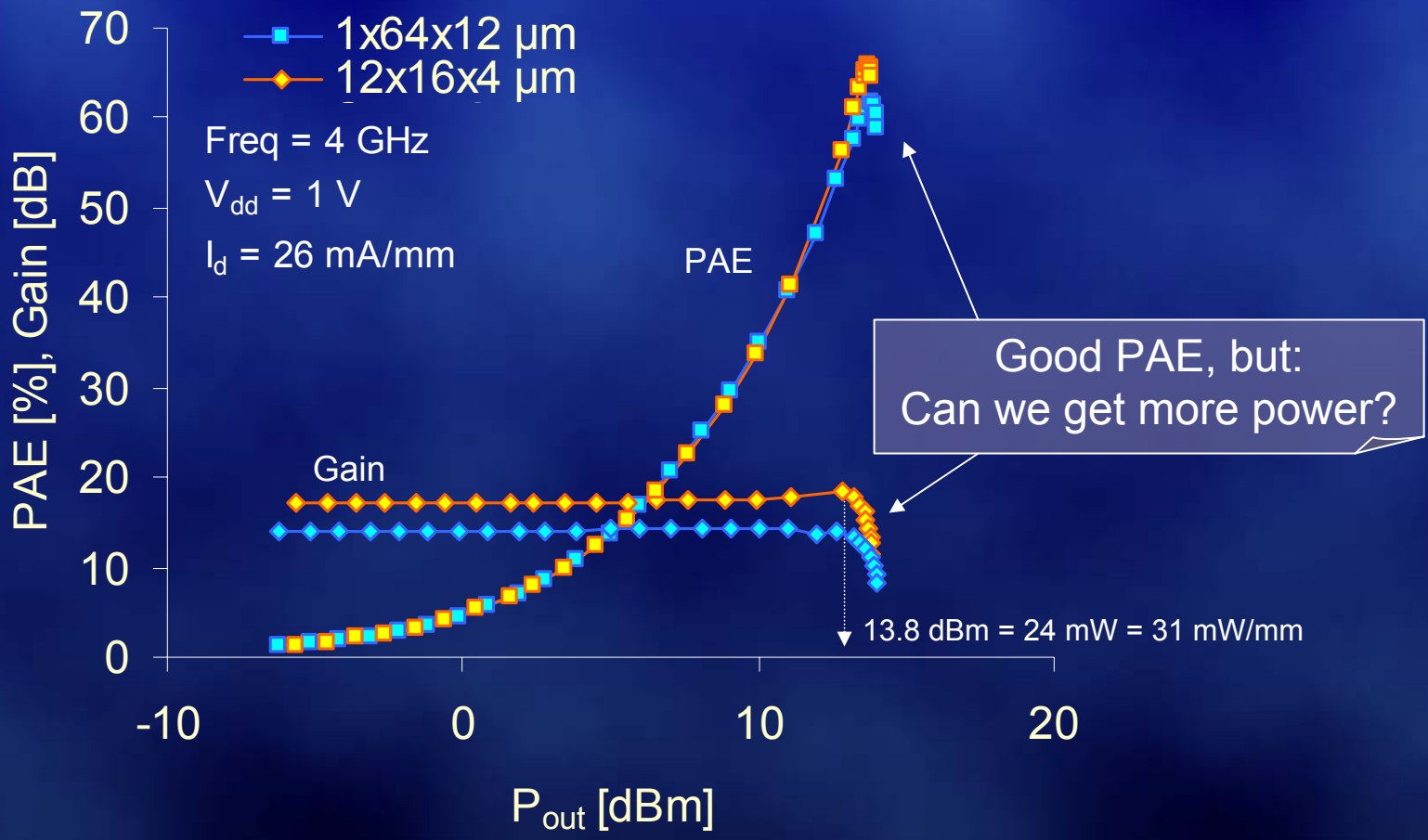
12x16x4 µm: Peak PAE = 66% at P_{out} = 13.7 dBm

RF power performance of standard 65 nm devices



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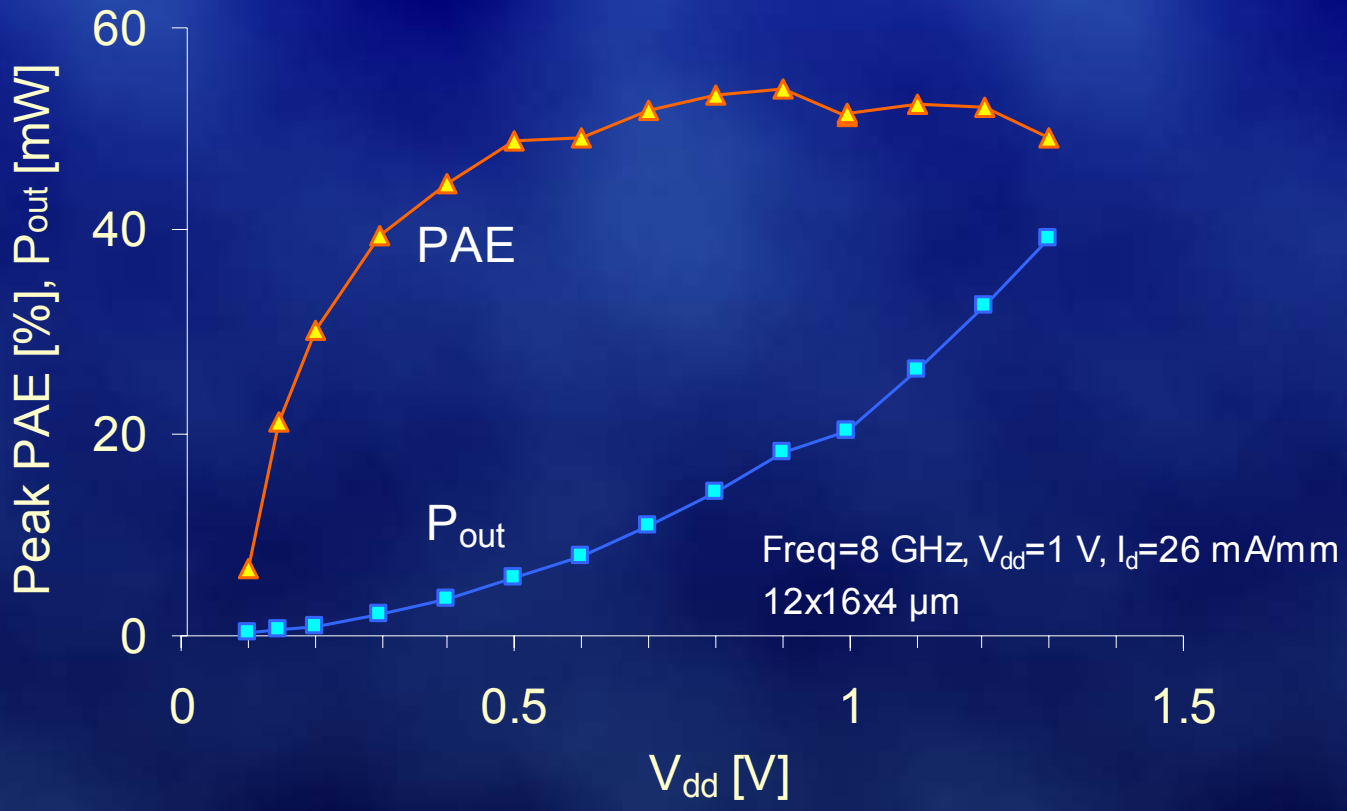
Increasing Output Power

- 65 nm CMOS features sufficient PAE
- Possibilities to increase P_{out}
  - Supply voltage (V_{dd})
  - Bias current (I_{dq})
  - Device width ($W_{G,TOT}$)
- Methodology:
  - Optimize for peak PAE

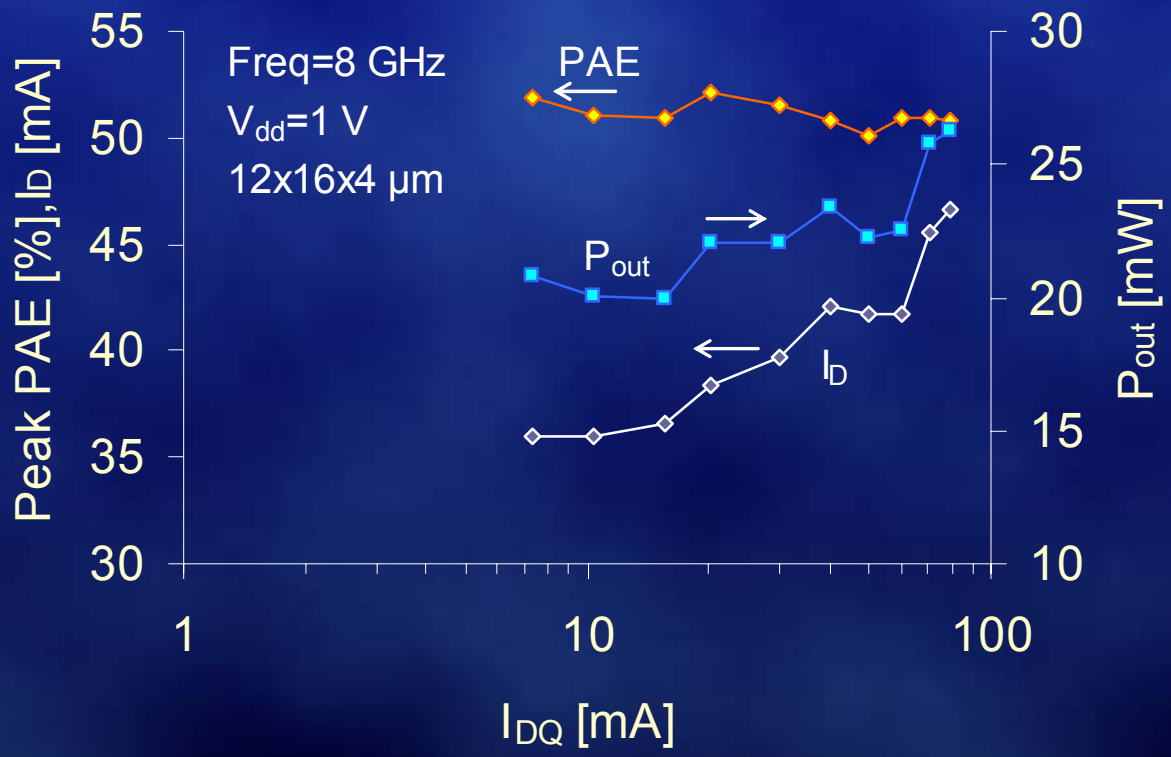
Increasing P_{out}: V_{dd}



- Increases P_{out} without impacting PAE
- Potential drawback: reliability

Increasing P_{out}: I_{DQ}

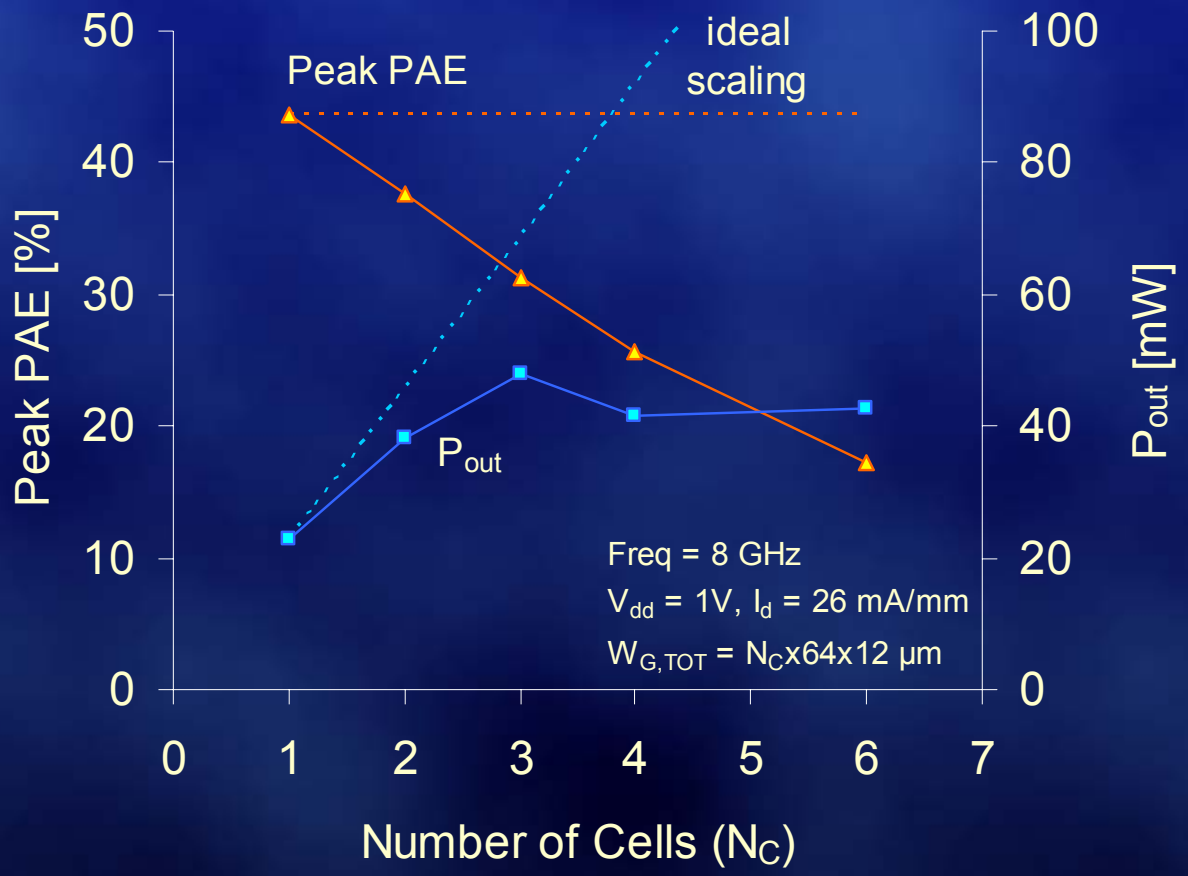
- Increase I_{DQ} → class AB to A



- P_{out} largely independent of I_{DQ}
  - Strong self-biasing: I_{DQ} 10x → I_D 1.3x

Increasing P_{out}: Device Width

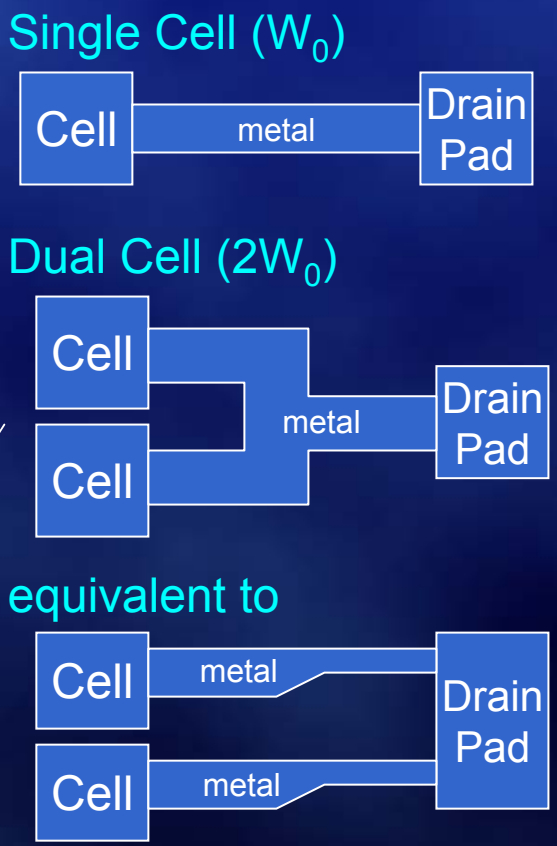
- $P_{out} \sim W_{G,TOT} = N_C \times N_F \times W_{G,F}$

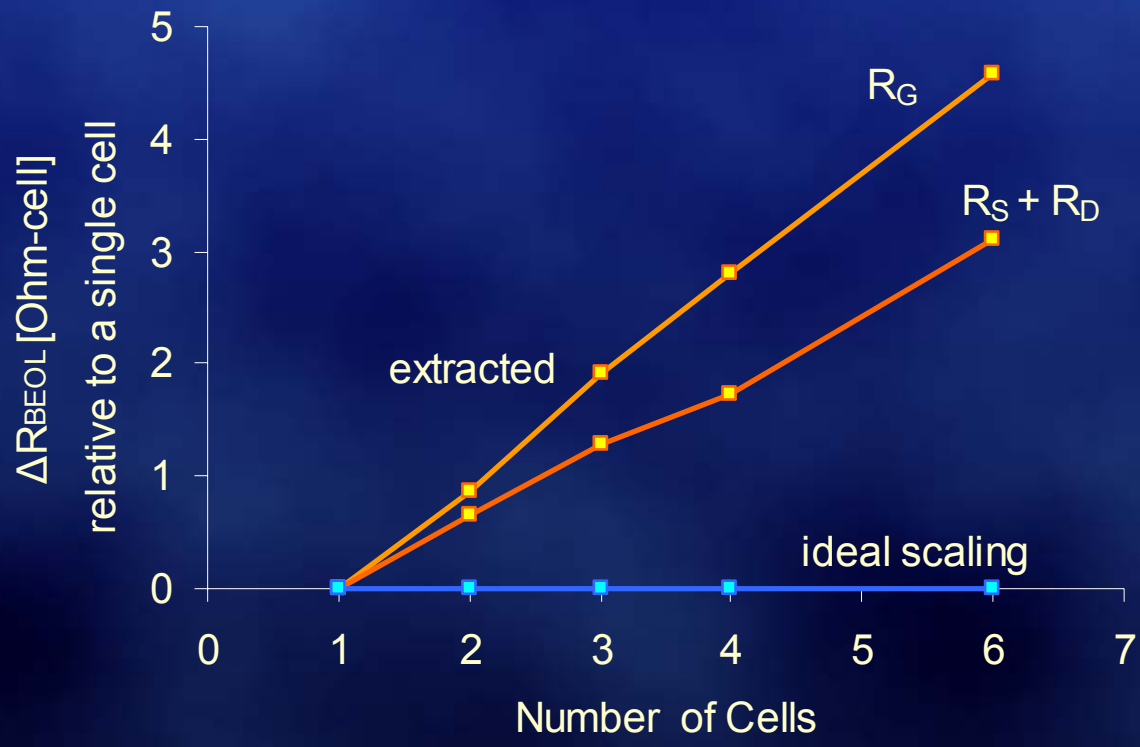


P_{out} saturates
PAE drops!

Parasitics in Parallel Cells

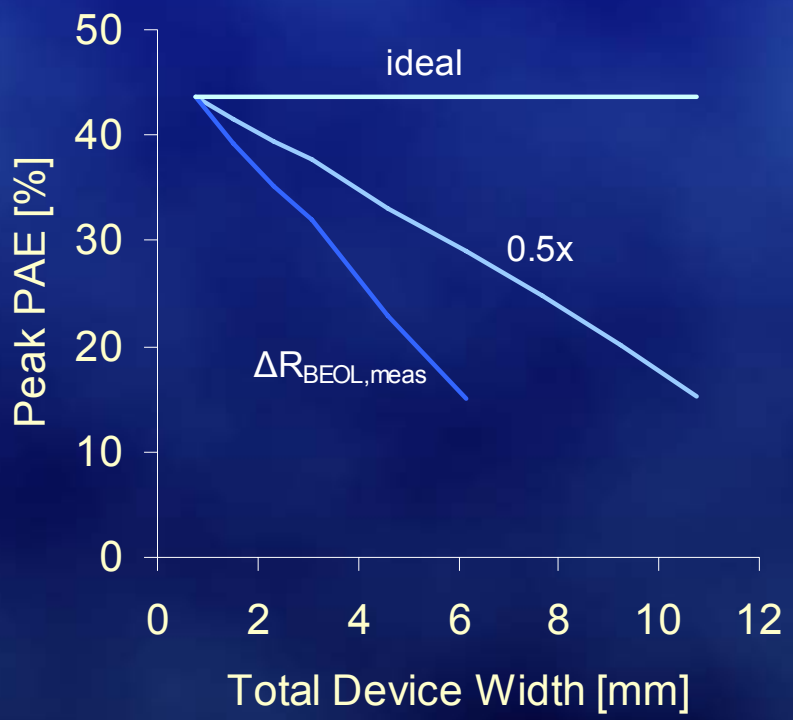
- Low V_{dd} → High I_D → High I-R drop in backend
  - Layout wires do not scale with $W_{G,TOT}$

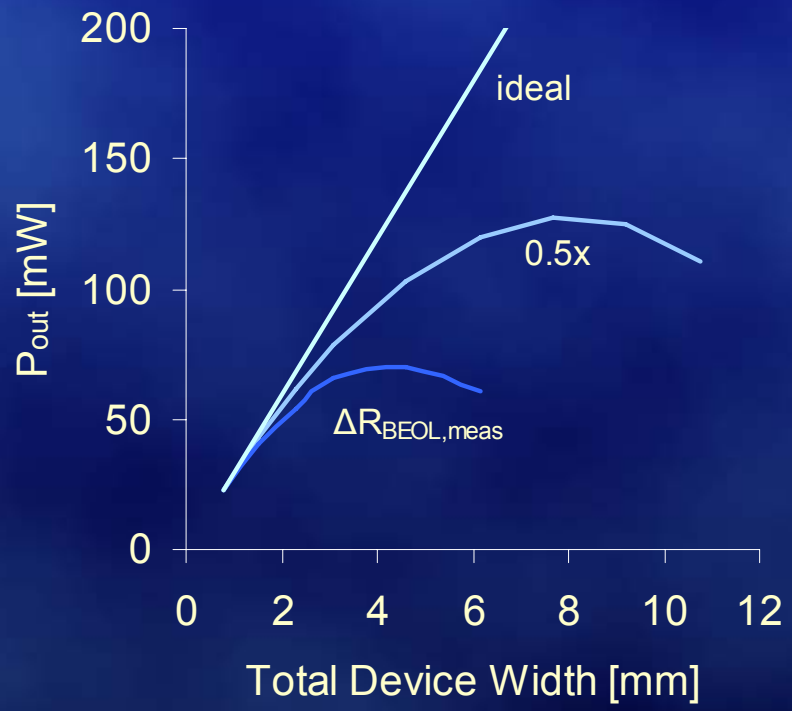




Modeling Parallel Cell Behavior

- Increasing R_{BEOL} → dissipate power → P_{out} ↓ for P_{DC}=const → PAE ↓





- Simple loss model: behavior matches data
  - PAE drops with number of cells
  - P_{out} saturates and eventually decreases

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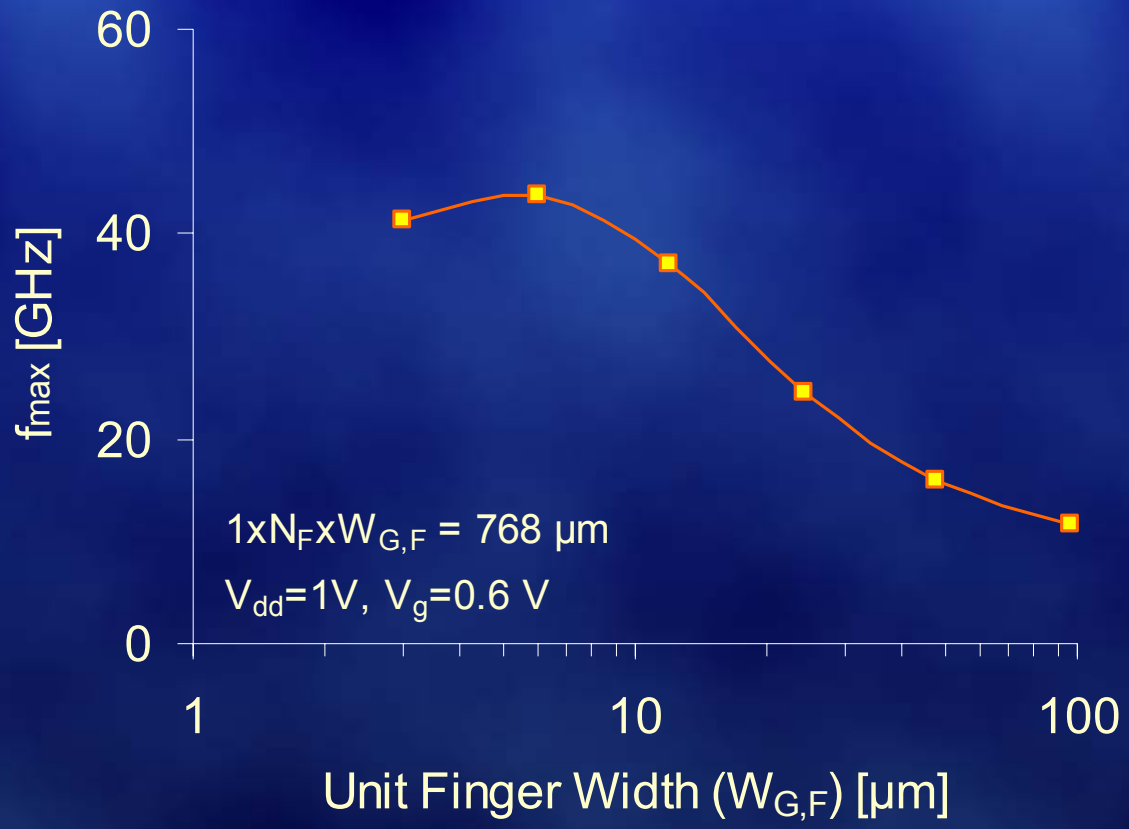
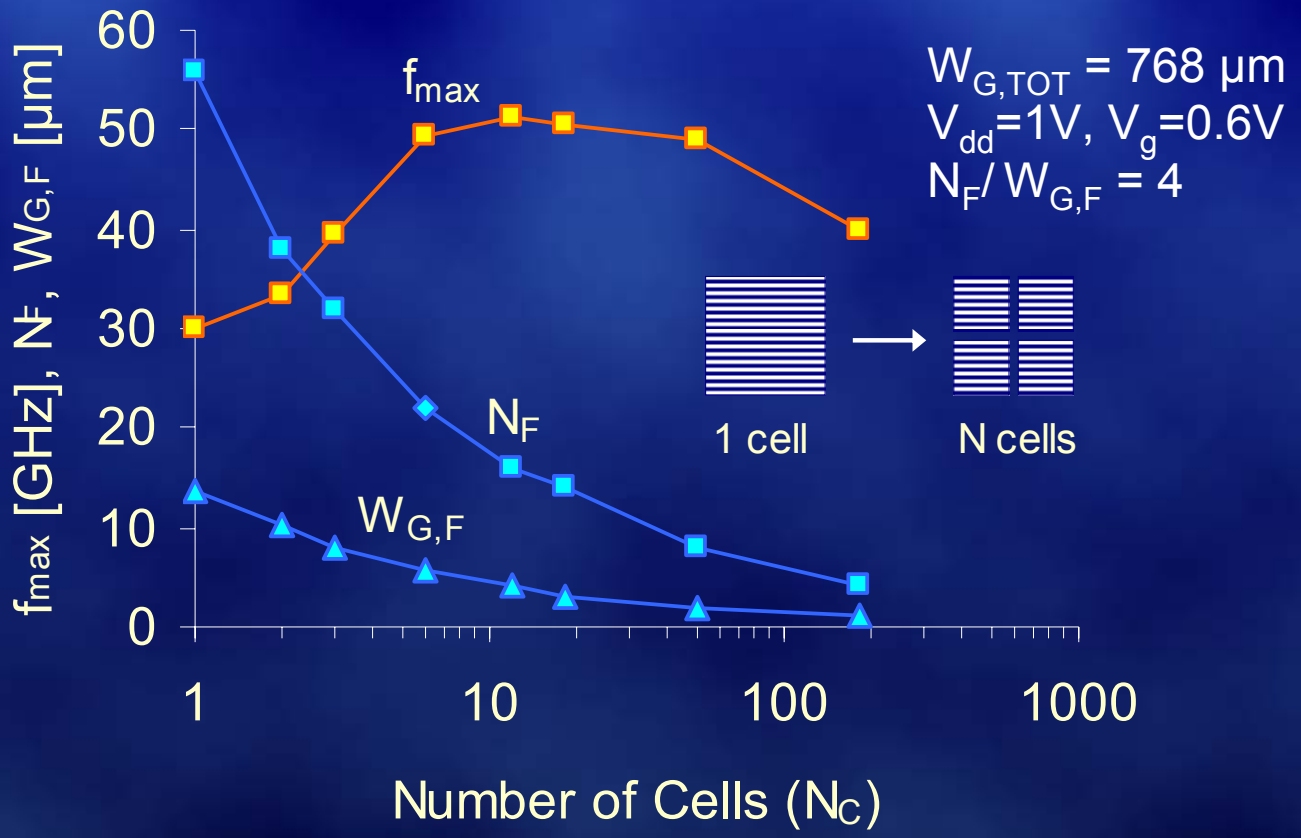
Maximizing 65 nm Performance



- Wide fingers → Parasitic R_G losses
- Many narrow fingers → Distributed effect losses

Maximizing 65 nm Performance: Power Cell Sizing

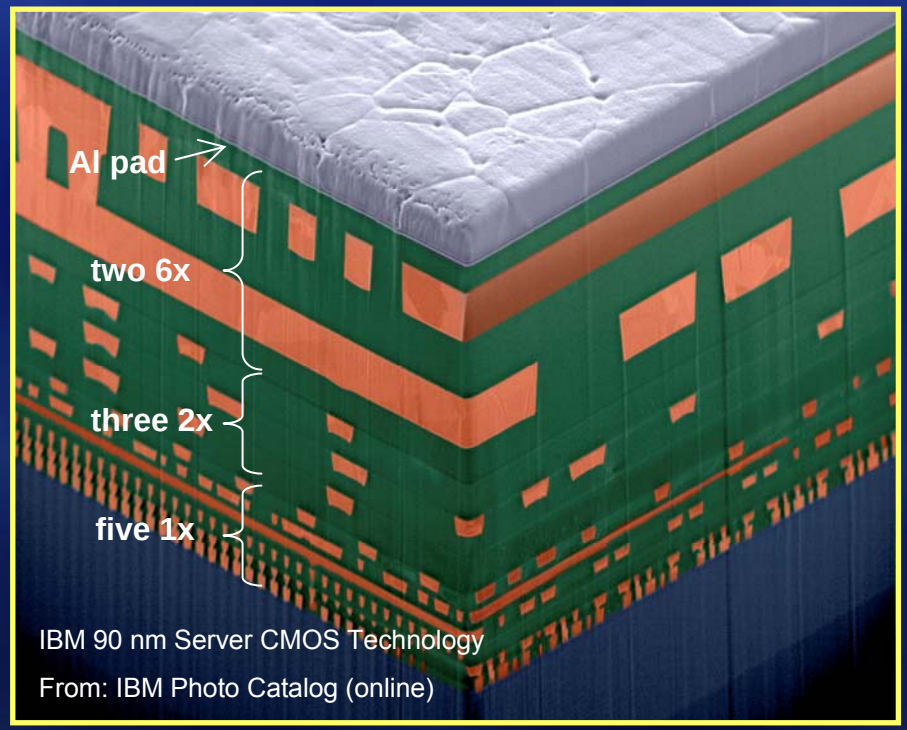


- Optimal unit cell size (N_F x $W_{G,F}$)
- Layout critical for optimizing f_{max} → PAE

Maximizing Performance

- P_{out}: Source/Drain Metallization
  - Must R_{BEOL} scale with $1/W_{G,TOT}$
    - Wider and stacked metal lines
    - Use of thicker high level layers

- PAE: Multi-cell approach (N_C)
  - R_G → Limit $W_{G,F}$
  - Distributed effects → Limit N_F



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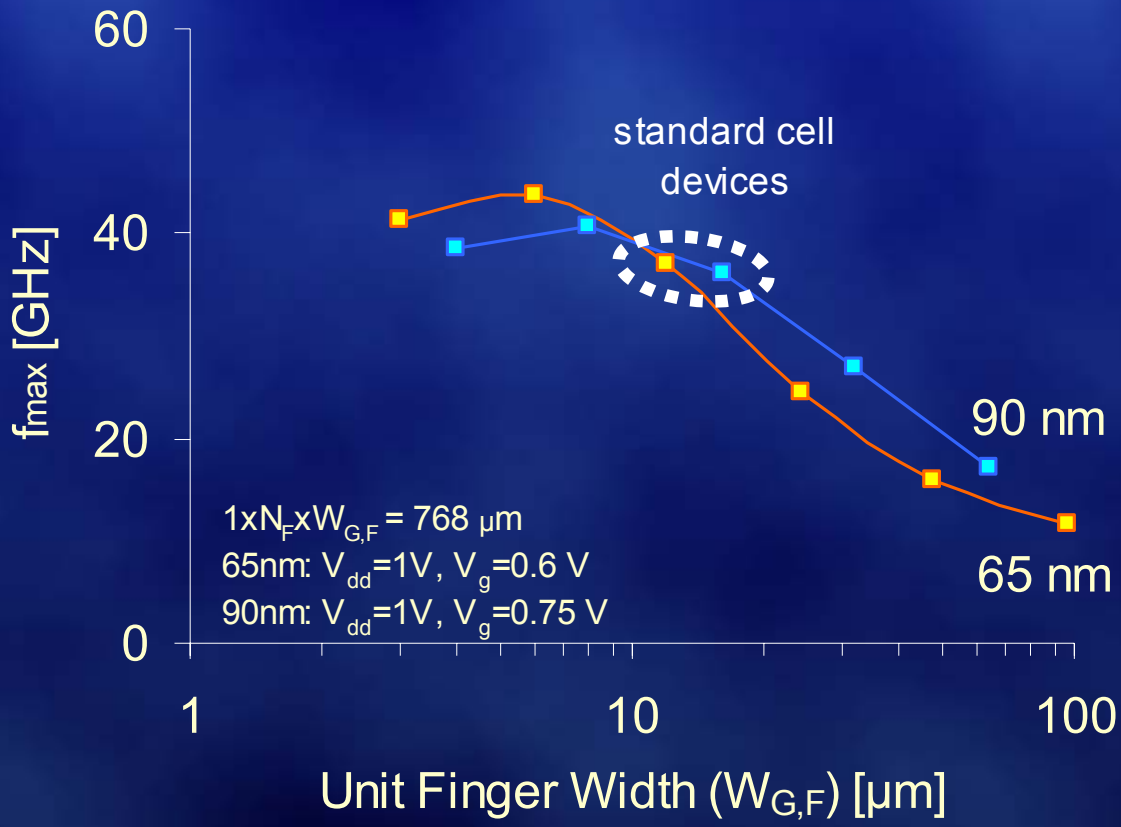
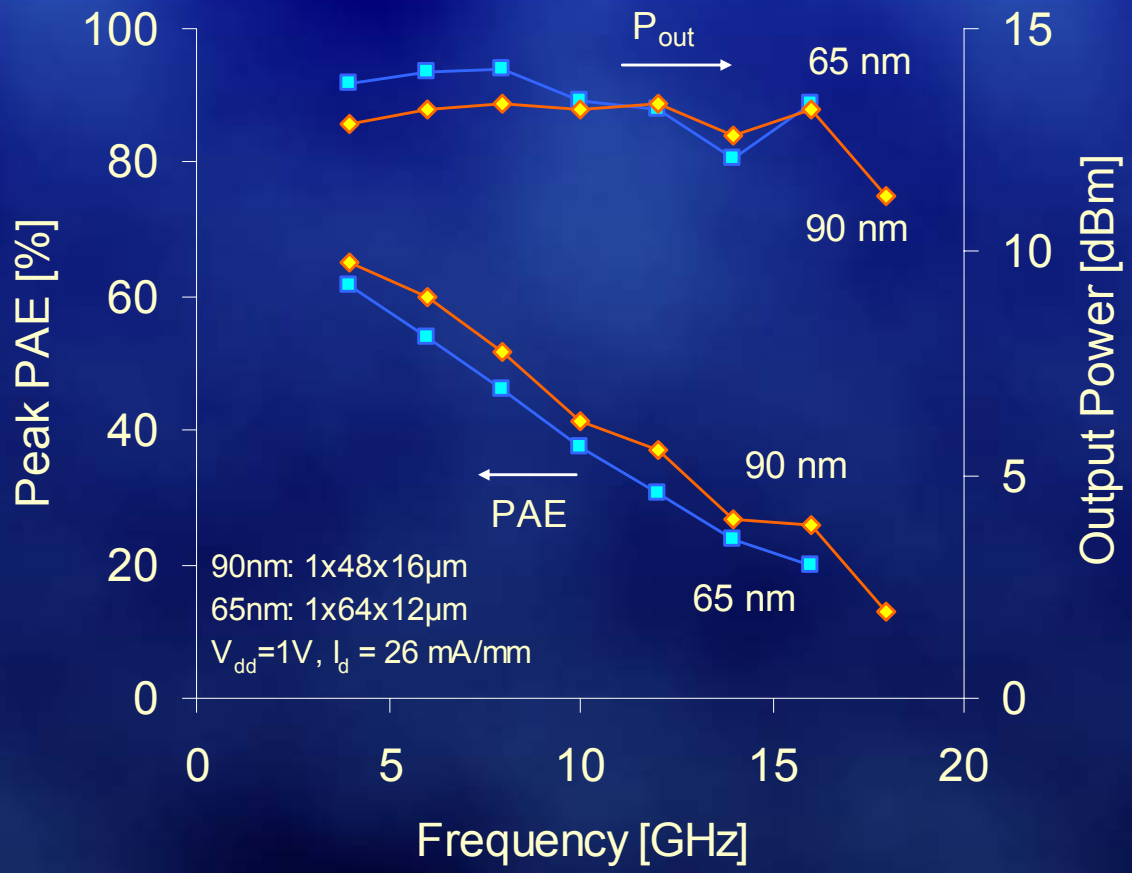
f_{max} Performance: 65 and 90 nm



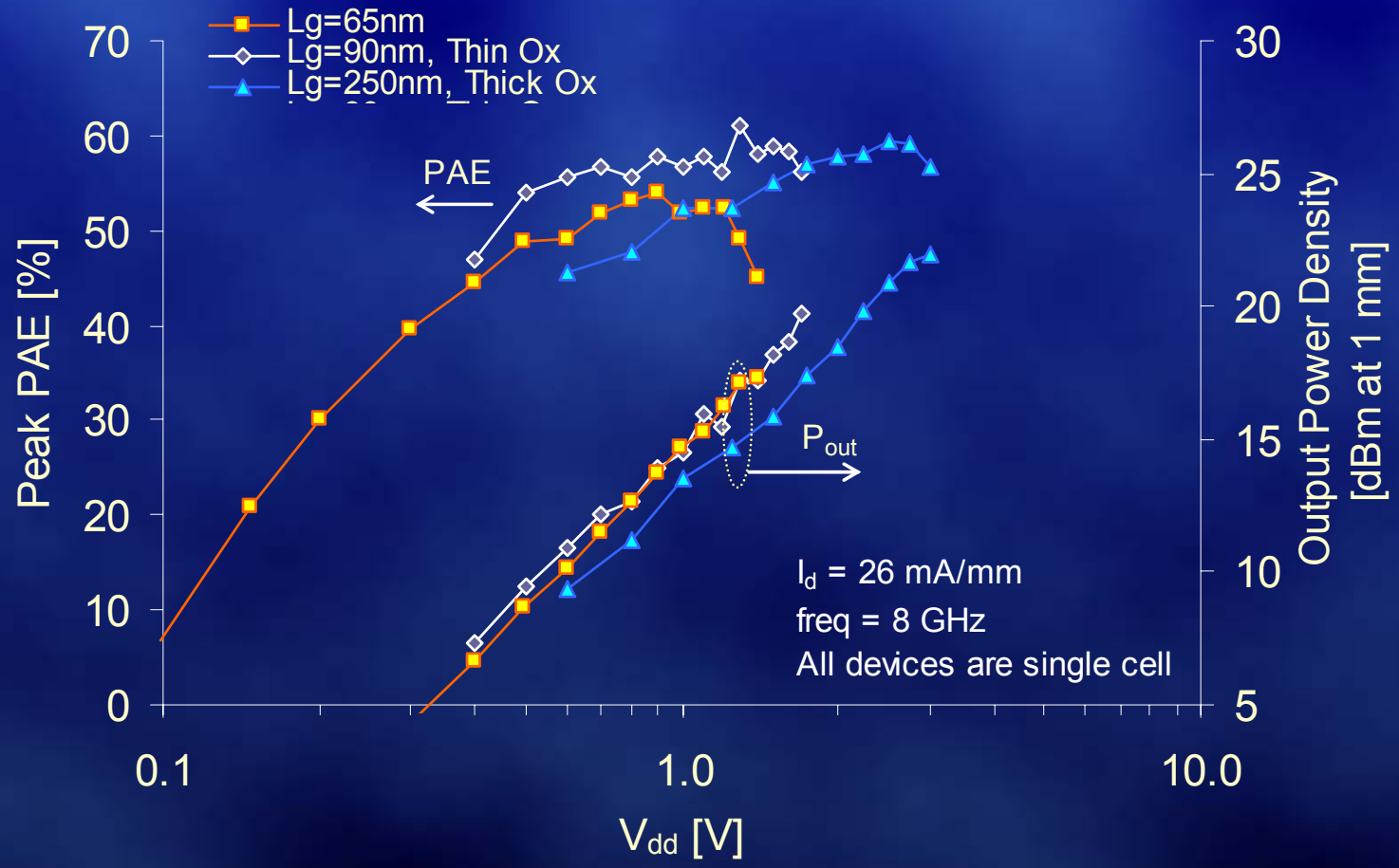
- Comparable f_{max} performance of 65 nm and 90 nm
- $L_G \downarrow \rightarrow$ optimum $W_{G,F} \downarrow$

Performance Similar Across Frequency



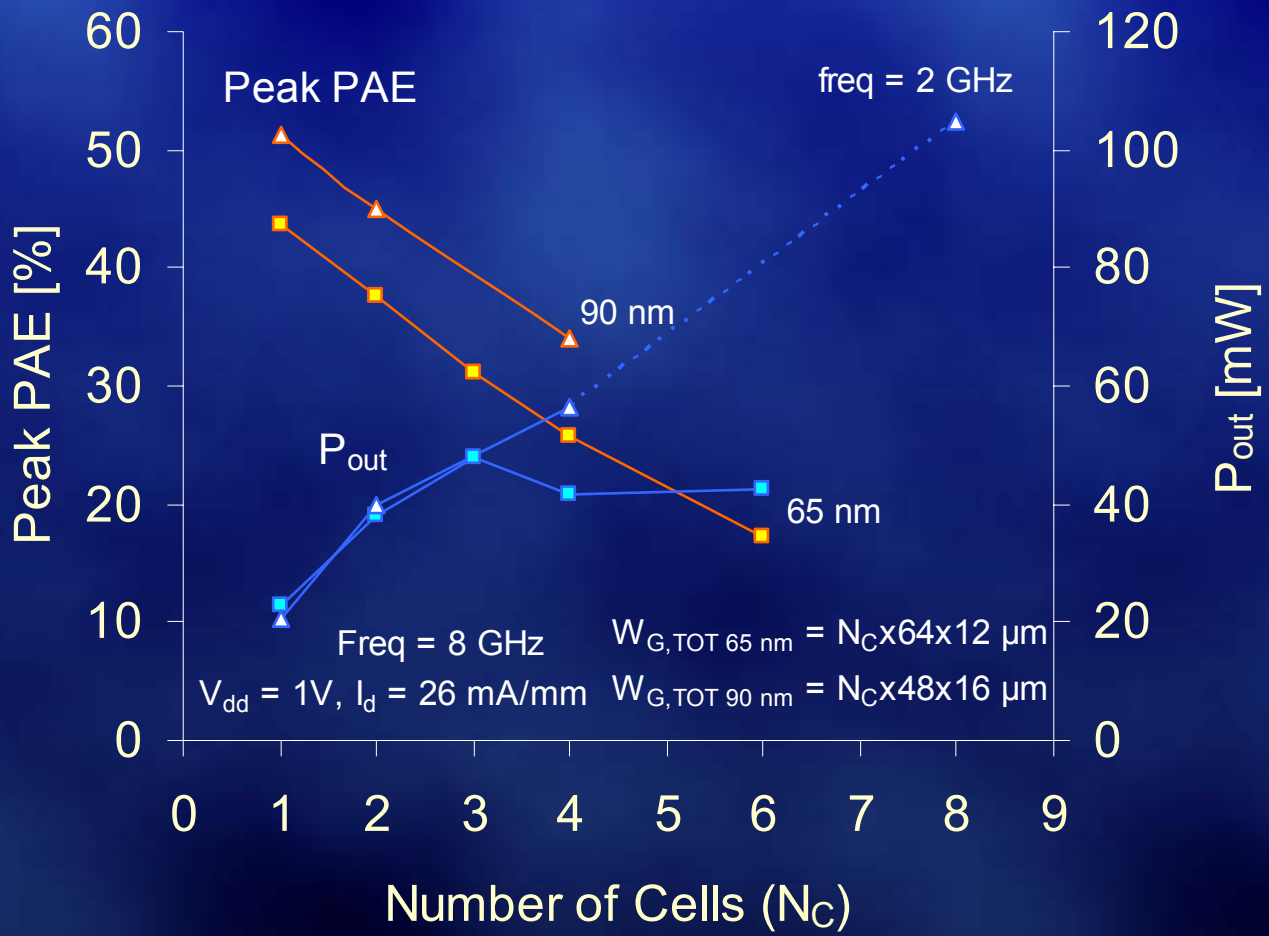
- Standard Cell: Similar P_{out} and PAE behavior

Performance Similar Across V_{dd}



- Similar P_{out} and PAE behavior for all three technologies
- Intrinsic devices: similar performance (freq, V_{dd})

Performance Differs Across $W_{G,TOT}$



65 nm: P_{out} saturates

90 nm: P_{out} increases

Conclusions

- 65 nm device
  - Similar voltage and freq. performance across 65, 90 nm and 0.25 µm
  - 4 GHz: 66% PAE, P_{out} = 31 mW/mm
  - 8 GHz: 54% PAE
- 65 nm BEOL: impact on $W_{G,TOT}$ scaling
  - Currently: power saturates
  - BEOL critical for performance
- Solutions
  - Use layout to reduce R_{BEOL}
  - Stacked metal lines
  - Use thick top level metal