Thermal, electrical and environmental reliability of InP HEMTs and GaAs PHEMTs

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Abstract

This paper reviews current understanding of reliability of InP HEMTs and GaAs PHEMTs. Operating temperature, bias point, and the environment are all known to affect the long-term stability of these devices. Identifying the dominant failure mechanism in a given situation is difficult because fundamental understanding is still insufficient, several mechanisms have a similar signature, and because often times, there are multiple mechanisms acting simultaneously. In spite of this, GaAs PHEMTs and InP HEMTs are already remarkably reliable and the prospect of further improvements are good.

Introduction

There has been intense research on the reliability of InP HEMTs and GaAs PHEMTs for some time. These devices are critical for radar, communications and scientific applications. Many reports detaile a myriad of changes in the characteristics of these devices under various stressing conditions. A comprehensive picture has yet to emerge. Contributing towards this is the purpose of this paper.

A rapid device design cycle demands that device reliability be evaluated under accelerated conditions with parts biased at or above the operating point at higher than operating temperatures. The conventional wisdom is that this speeds up device wearout. If a technology does not meet the reliability specs, a device redesign is required, usually at the expense of lower performance, higher cost, and delayed technology deployment. These trade-offs highlight the importance of understanding the nature of the dominant failure modes early in the development cycle.

There are three broad kinds of reliability mechanisms: 1) thermal, 2) electrical, and 3) environmental. In practical situations, it is common to observe failure modes in which several mechanisms are present at once, often in an interacting way. This paper reviews current understanding of fundamental failure mechanisms in GaAs PHEMTs and InP HEMTs with emphasis on power applications.

Thermal reliability

GaAs PHEMTs and often InP HEMTs use heterostructures that are intrinsically strained. In spite of this, these heterostructures are found to be thermally stable to temperatures up to 700-800 °C [1]. However, thermal stressing results in several deleterious effects in finished devices:

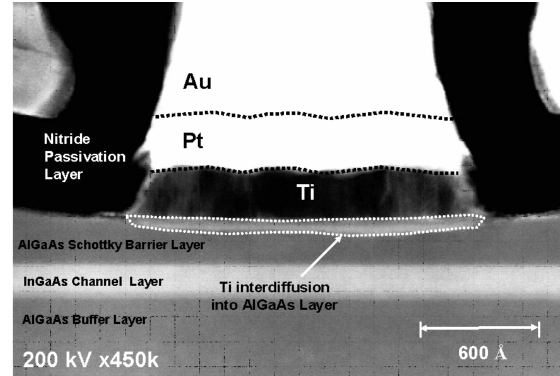

Figure 1: STEM micrograph of a 0.15 μm GaAs PHEMT subjected to lifetest showing evidence of Ti diffusion into the AlGaAs barrier layer (courtesy of Y. C. Chou [2]).

1. *Gate sinking* [2, 3]. In TiPtAu-gated HEMTs, Ti diffuses from the gate stack into the barrier layer (AlGaAs or InAlAs) resulting in the formation of intermetallic compounds (Fig. 1). The main consequence is a *positive* shift in V_t, which causes a drop in I_{dss} (Fig. 2) and P_{out} (though g_m does not necessarily increase). Gate sinking is a thermally activated mechanism with E_a in the 1.4-1.6 eV range, perhaps too high to be relevant at room temperature. Gate sinking evolves as $\sqrt{t}$, consistent with a diffusion mechanism. It is not recoverable. The impact of gate sinking is less severe for thicker barrier layers [2]. Gate sinking can also be alleviated by using refractory barrier metals, such as WSi, WSiN and Mo.

2. *Ohmic contact degradation* [4]. Most ohmic contacts are based on Au. Au can diffuse through the barrier metal(s), resulting in the formation of new intermetallic compounds and an increase in contact resistance. This is a thermally activated mechanism with $E_a \simeq 1.6\ eV$. Contact degradation evolves as $\sqrt{t}$ and it is not recoverable. Ohmic degradation can be alleviated by using refractory barrier metals, such as WSi, or using low InAs composition caps.

3. *Thermally activated electron detrapping* from deep traps in the barrier layer takes place across the entire device [5]. This produces a negative shift in V_t, and a reduction of R_s and R_d, bringing along with it an increase in the peak g_m. The impact of this in P_{out} is unclear since changes in the breakdown voltage have not been reported. This effect has been found to be completely reversible [5].

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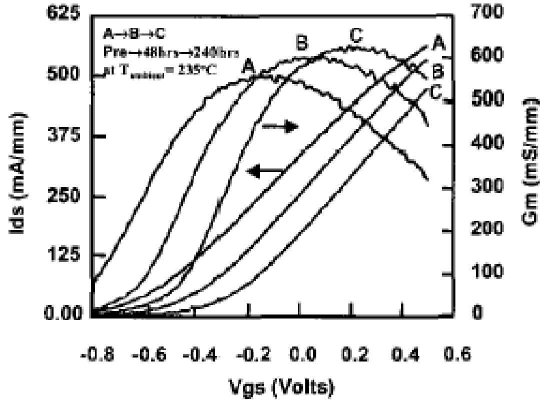

Figure 2: Progressive g_m and I_d evolution of a 0.15 μm GaAs PHEMT subjected to lifetest [2]. This is the classic electrical signature of gate sinking.

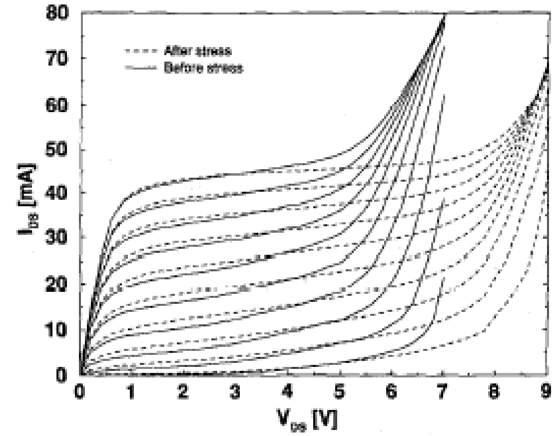

Figure 3: Output characteristics of a GaAs PHEMT before and after hot electron stress indicating *breakdown walkout* [10].

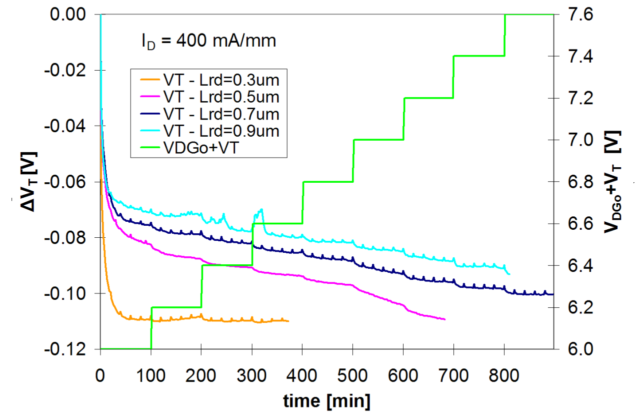

Figure 4: Time evolution of ΔV_T for voltage step-stress experiments at constant current performed on four different PHEMTs with different values of gate-drain gap [11].

4. *Surface state annealing* arises from a compositional modification of the surface oxides in the exposed GaAs or AlGaAs source and drain access regions. This increases the sheet carrier concentration in the extrinsic source and drain, n_s. The key electrical signature is a reduction in the kink effect and the frequency dispersion of the device, and a reduction in BV_{off} [6]. This occurs without a change in V_t. This mechanism tends to saturate and is irreversible. Because of the loss in BV_{off}, surface state annealing typically results in a drop in P_{out}. The obvious fix-up is to avoid the occurrence of surface states in the first place.

Electrical reliability

Severe and prolonged electrical stressing has been found to result in many changes to the electrical characteristics of GaAs PHEMTs. While the details are still controversial, hot electrons and impact ionization appear to be at the root of most of the mechanisms that have been identified. These are summarized next.

5. *Trap creation on the drain access region* is believed to occur as a result of hot electrons [7, 8, 9]. The subsequent electron occupation of these traps reduces n_s in the extrinsic drain next to the gate. The main electrical consequences are a reduction in I_d, an increase in R_d and an increase in BV_{off} (*breakdown walkout* [10], see Fig. 3). No changes are detected under the gate or on the source side of the device. The rate of trap formation has been found to be linear in V_{DG} and the impact ionization rate and quadratic in time. This phenomenon is not reversible. It is unclear exactly where these traps are located, i.e., at the barrier-channel interface or at the barrier surface. There is also no consensus about the details of the physical damage that leads to the creation of these traps.

6. *Trapped electron recombination* occurs when holes generated by impact ionization neutralize electrons trapped in the barrier or buffer layers under the gate [5]. This produces a negative shift in V_t. This mechanism tends to saturate with time because the traps can be completely emptied out [11] (Fig. 4). This mechanism is recoverable because the traps can get replenished with electrons. One would expect this mechanism to result in an *increase* in P_{out} though this has not been observed, probably because it is masked by other P_{out} degrading mechanisms.

7. *Hole trapping* has been observed in deep traps in the AlGaAs barrier or at the gate/AlGaAs interface under the gate [12]. This tends to produce a negative shift in V_t and an increase in I_{dss} and I_{max}. g_{mpk} does not change. The shift in V_t takes place in the scale of seconds, it is linear in V_{DG} and is not recoverable.

8. *Surface corrosion* in the drain access region of GaAs PHEMTs can take place when electrons or holes overcome the energy barrier presented by the AlGaAs barrier layer

and reach the semiconductor surface where they produce an electrochemical reaction [13]. Surface corrosion results in the formation of surface oxides and the consumption of a fraction of the AlGaAs barrier (Fig. 5). This produces an increase in R_d, and a reduction in I_{max}, impact ionization, and P_{out}. This mechanism does not saturate in time and is not reversible. It is also accelerated in air. Surface treatments have been shown to alleviate this problem [13].

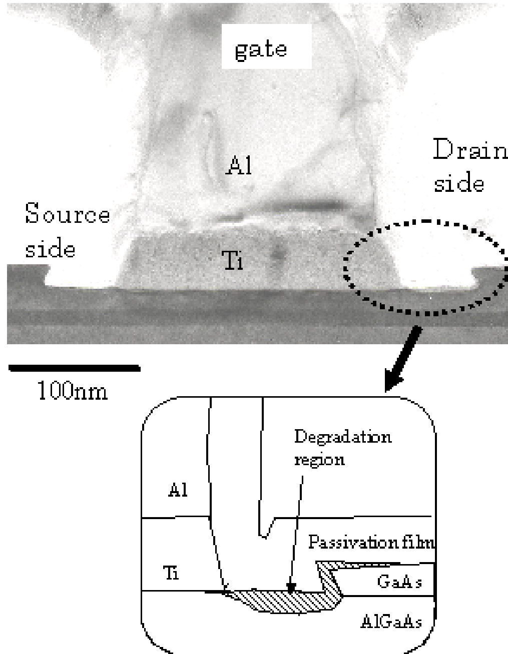

Figure 5: TEM micrograph of a PHEMT after RF life test. Corrosion is evident on the drain side (courtesy of T. Hisaka [13]).

9. *Charge injection and trapping in the passivation layer* on the drain access region of the device can arise as a result of hot electron injection from the channel or simply electron injection from the gate itself. This mechanism results in a reduction of I_{max} and P_{out}, and an increase in R_d and BV_{off}. In its early stages, charge trapping in the passivation is seen to be reversible. The recovery rate is thermally activated with $E_a \simeq 1.4\ eV$. This is referred to as *power drift* [14]. In a more advanced stage, charge trapping becomes irreversible. This situation is referred to as *power slump*. It is postulated that power slump occurs when trapped electrons recombine with injected holes and the energy that is released frees up hydrogen in the insulator creating Si dangling bonds [14]. To complicate matters, charge trapping in the insulator is believed to impact charge trapping at the insulator/semiconductor interface with consequences similar to mechanism 5 above.

Hot electron degradation of the drain access region is the most widely reported failure mechanism of PHEMTs. Understanding electrical stress damage is complicated by the

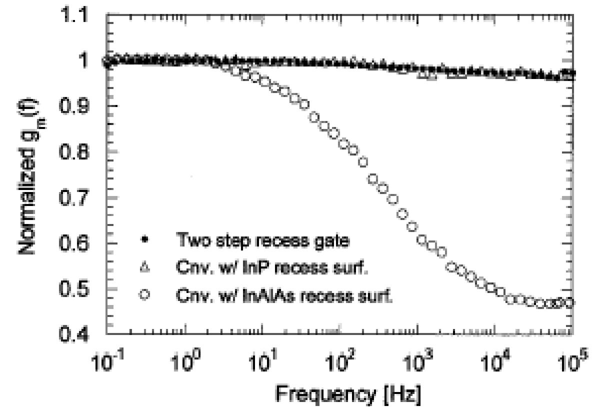

Figure 6: Frequency dispersion of transconductance of InP HEMTs having a two-step recess gate, conventional gate with InP recess surface, and conventional gate with InAlAs recess surface. Only the device with exposed InAlAs shows dispersive behavior [18].

fact that self-heating during stress can cause electron detrapping [5]. Hot electron stress has also been correlated with surface contamination. Suitable surface treatments appear to mitigate it [13, 15]. Since hot electron degradation is associated with the exposed portion of the drain, wide-recess devices are found to be less reliable than narrow recess devices [16], an important consideration in device design. Hot electron stress in InP HEMTs has been mitigated by using an InP etch stopper [17, 18] (Fig. 6).

Environmental reliability

The environment also plays a role in the reliability of HEMTs. H_2 and F have received a lot of attention recently.

10. *Hydrogen* is now well understood to become catalyzed by the Pt layer in the Ti/Pt/Au gate stack and react with Ti producing TiH [19, 20, 21]. H also affects the Ti layer of Ti/Al gates. The formation of TiH creates tensile stress in the semiconductor heterostructure that shifts V_t. The sign of the V_t shift depends on the gate orientation. The time evolution is initially $\sim \sqrt{t}$ (reflecting H diffusion in the Ti) and then saturates (Fig. 7). Under some conditions, this mechanism is reversible as the TiH dissolves. A potential solution consists of separating the Ti layer from the semiconductor surface using a WSi barrier layer [22].

11. *Fluorine dopant passivation* is a severe problem in InP HEMTs [23]. F is a widely used element in the processing of semiconductor devices. It is also readily present in air. Through annealing at moderate temperatures, F diffuses into n-type InAlAs and passivates the dopant atoms. This results in a reduction of n_s and an increase in R_s and R_d. F dopant passivation has only been observed in n-InAlAs (Fig. 8). Hence an effective solution for this problem is to use a different carrier supply layer material, such as InP,

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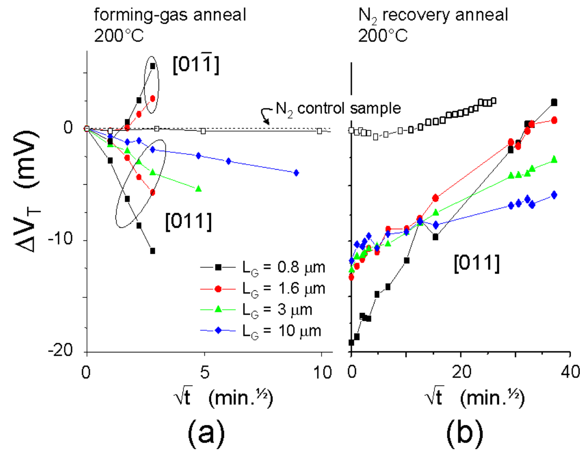

Figure 7: ΔV_t of InP HEMTs measured *in situ* (a) during the anneal in forming-gas at 200 °C, and (b) during the subsequent recovery anneal in N_2 at 200 °C. The orientation dependence of ΔV_t during forming-gas anneal is a key signature of the piezoelectric effect, indicating stress in the gate metal. Control samples annealed in N_2 (shown in open symbols) display negligible effects [20].

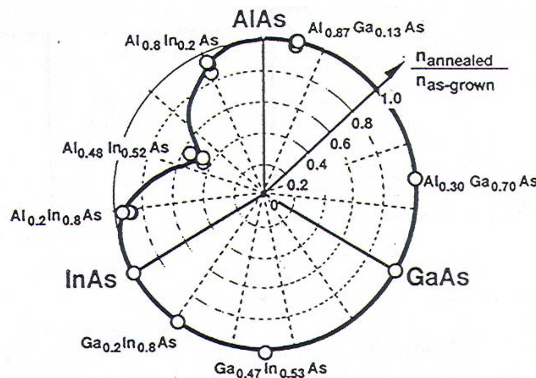

Figure 8: Material dependence of carrier concentration change by F contamination and thermal annealing for Si-doped materials consisting of AlAs, GaAs, and/or InAs components (from Hayafuji).

InAlP, or AlAs/InAs SL [24]. Understanding F passivation is complicated by the fact that F diffuses as a negatively charged species. As a result, in a biased HEMT, F tends to accumulate towards the gate edge of the source access region and towards the drain contact end of the drain access region [24] (Fig. 9). This has been reported to result in an increase in R_s that is thermally activated ($E_a = 1.1\ eV$). It is also expected to result in a degradation of the drain ohmic contact, though this is often masked by the large hot-electron induced increase in R_d.

In spite of the long list of failure mechanisms, the prospects for the development of reliable GaAs PHEMTs and InP HEMTs appear good. GaAs PHEMTs that are projected to operate reliably for over 10^9 hours at 125 °C and at 4.2 V have been reported [25]. For InP HEMTs, 3 V reliability has been demonstrated for over 10^7 hours at 125 °C [26].

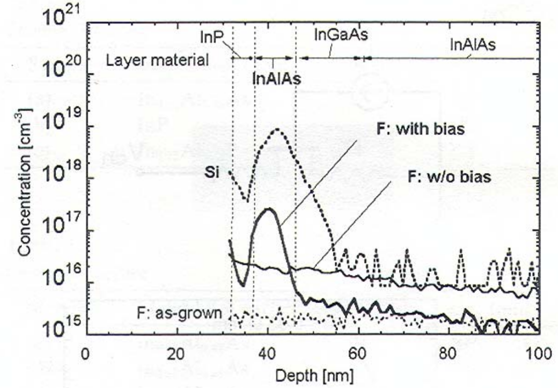

Figure 9: Impurity profiles obtained by SIMS in an InP HEMT subject to F contamination and 195 °C storage for 700 h. Voltage bias was applied to one sample during storage. The biased sample exhibits a pile up of F in the Si-doped InAlAs layer [24].

Conclusions

Much remains to be understood about the thermal, electrical and environmental reliability of GaAs PHEMTs and InP HEMTs. There is broad consensus around several failure mechanisms, but other important ones are still shrouded in mystery. In spite of this, the long term prospect for the development of reliable GaAs and InP HEMT technologies are good.

Acknowledgements

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