Experimental Comparison of RF Power LDMOSFETs on Thin-Film SOI and Bulk Silicon

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***Abstract*—We have simultaneously fabricated RF power LDMOSFETs on thin-film SOI and bulk silicon wafers. This work compares their DC current–voltage (I–V), capacitance–voltage (C–V), S-parameter, and 1.9-GHz load-pull characteristics and explains differences between them. The SOI LDMOSFET performance is shown to be largely similar to the performance of an equivalent bulk silicon LDMOSFET, but there are important differences. The SOI LDMOSFET has moderately lower on-state breakdown voltage due to increased body resistance. It also has significantly improved power-added efficiency due to reduced parasitic pad losses.**

***Index Terms*—Power MOSFET, silicon-on-insulator (SOI) technology.**

I. INTRODUCTION

SILICON-ON-INSULATOR (SOI) MOS technology has proven to be successful in many diverse applications from digital CMOS [1] to high voltage power devices [2]. Most recently, thin-film SOI lateral double-diffused MOSFETs (LDMOSFETs) have been explored for use in radio frequency power amplifiers (RF PAs). The RF PA is a critical component of all wireless systems, and bulk silicon LDMOSFETs are widely used in both cellular handsets [3] and in cellular base-stations [4]. Thin-film SOI LDMOSFETs have received particular attention for highly integrated wireless system-on-a-chip (SOC) applications. This paper concerns the design and fabrication of LDMOSFETs on SOI for handset RF power applications.

Thin-film SOI technology is interesting for RF PAs for three primary reasons. The buried oxide in the SOI structure reduces capacitive coupling to the substrate, which improves power efficiency [5]. The SOI buried oxide also provides improved isolation between adjacent circuits [6], making it attractive for highly integrated power amplifiers in which substrate cross talk is a concern. A third advantage is that it allows for the use of high resistivity substrates [7] that enable the fabrication of low loss on-chip inductors.

Previous work on thin-film SOI LDMOSFETs for RF PAs is encouraging. In [8] and [9], we demonstrated an RF LDMOSFET on SOI that had DC and small-signal RF characteristics that are suitable for RF PAs. The f_t of the devices approach 15 GHz and the breakdown voltage exceeds 20 V. In [7], [10]–[12], LDMOSFETs were also demonstrated on SOI with substantially different designs and varying levels of performance. In [12], SOI LDMOSFETs were demonstrated with an off-state breakdown voltage of 14 V and a remarkable power-added efficiency (PAE) of more than 50% at 5.8 GHz. Complete integrated RF PAs on SOI were demonstrated in [13] and [14].

In this paper, we study the SOI LDMOSFET through a direct comparison with an equivalent bulk silicon LDMOSFET, a proven RF power device. We fabricated thin-film SOI and bulk silicon LDMOSFETs simultaneously using an identical process. The devices are compared through DC current–voltage (I–V), capacitance–voltage (C–V), S-parameters, and large-signal RF measurements. We focus on explaining the differences that are seen in the devices' characteristics. Our work suggests clear advantages of SOI LDMOSFETs for handset type RF PA applications.

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II. DEVICE FABRICATION

The bulk silicon and SOI LDMOSFETs were fabricated simultaneously following an identical process. A cross section of the devices is shown in Fig. 1. The SOI LDMOSFETs are partially depleted and were fabricated on p-type ⟨100⟩ full-dose SIMOX wafers with an active silicon thickness of 200 nm, a buried-oxide thickness of 400 nm, and a resistivity of 10–20 Ω-cm. The wafer doping level of the bulk silicon devices is the same. In all wafers, LOCOS isolation was used and a 25 keV boron dose of 5×10^{12} cm^{-2} was implanted into the field region to properly isolate the devices. The gate oxide thickness is 30 nm. The polysilicon gate length of the SOI device is 0.6 μm, and the bulk silicon gate length is about 0.1 μm longer due to photolithographic variations.

The lateral body doping profile was formed by masking the drain of the device, implanting the source with boron of dose 1.3×10^{13} cm^{-2} and energy 25 KeV, and annealing the wafers for 300 min at 1000 °C. The 0.5 μm n$^-$ LDD region was created by a phosphorous implant of dose 3×10^{12} cm^{-2} and energy 55 KeV. The n$^+$ source and drain regions were formed by a masked implant of dose 5×10^{15} cm^{-2} and energy 25 KeV. The n$^+$ implant mask defined the length of the n$^-$ region. Dopant activation was achieved by a 20 s, 1000 °C RTA process.

After processing, the SOI devices feature a silicon thickness beneath the gate of 180 nm. The n$^+$-junction depth beneath the source is 100 nm. The body doping process creates a p-type link region in the 80 nm of silicon beneath the n$^+$-source. This region provides a low resistance path between the body and the source

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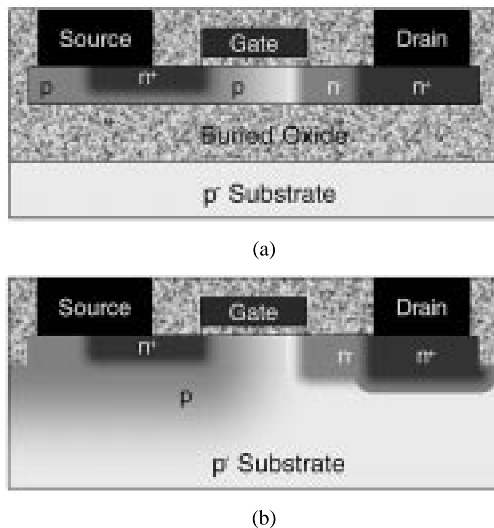


Fig. 1. Cross section of fabricated LDMOSFET on (a) SOI and (b) bulk silicon.

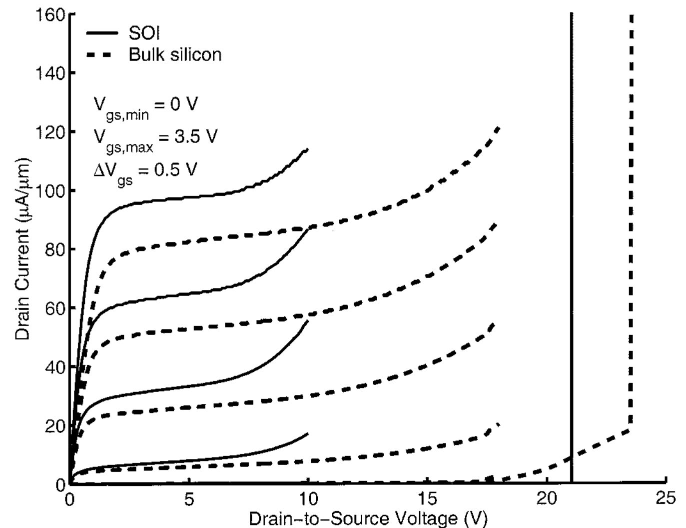


Fig. 2. Measured output characteristics of fabricated SOI and bulk silicon LDMOSFETs.

that is critical for obtaining a high on-state breakdown voltage and for suppressing the kink effect [8], [9].

III. Device Characterization and Comparison

The SOI and bulk silicon LDMOSFETs were thoroughly characterized using DC I–V, C–V, S-parameters, and large-signal RF measurements. Several differences are seen and the reasons for these differences are explained in this section.

The SOI and bulk silicon DC output characteristics are shown in Fig. 2. The device characteristics are similar but some minor differences are noticeable. These are due to both the effect of the buried oxide and to normal process variations. Both devices have a threshold voltage of about 1.6 V. The SOI device's transconductance and output conductance is higher because its gate length is shorter.

Both devices exceed the 20 V breakdown that is required of 3.6 V cellular handset applications. Though the n^- LDD implant and the drift length of the SOI and bulk devices are the same, the off-state breakdown of the bulk silicon device is higher than that of the SOI device. The reason for this is that the buried oxide minimizes the RESURF effect [15] in the SOI devices. In the bulk device, the p-type doping beneath the LDD region vertically depletes the n-type doping in the LDD. The buried oxide reduces the depletion of the LDD giving the bulk devices a higher breakdown voltage for the same LDD dose. Measurements of n^- implanted-resistor test structures confirmed that the RESURF effect is responsible for the reduced n^- carrier density in the bulk devices.

The bulk devices suffer from soft breakdown effects that are common in power devices. Soft breakdown effects are caused by local breakdown at the periphery of the device where the LOCOS isolation implant comes in contact with the LDD implant. These effects do not occur in the SOI LDMOSFET because the device is isolated from the substrate by the buried oxide. This was verified through light emission measurements that showed emission during soft breakdown at the LOCOS/gate intersection on only the bulk silicon devices.

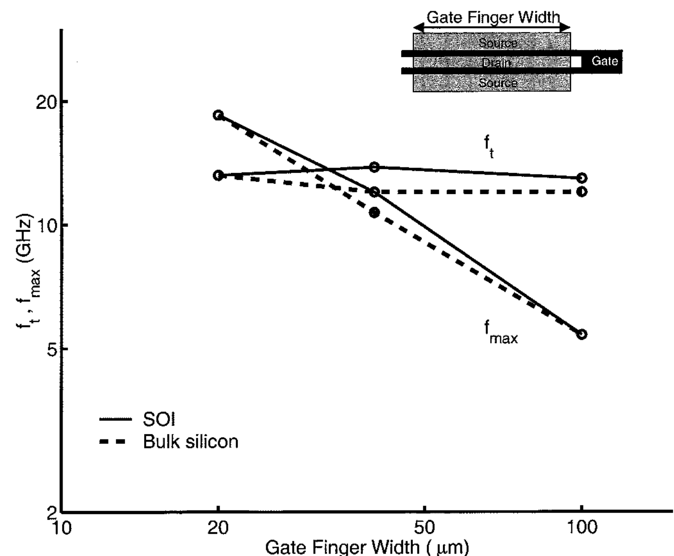


Fig. 3. f_t and $f_{\max}$ of SOI and bulk LDMOSFETs as a function of the gate finger width.

The on-state breakdown voltage of the SOI device is lower than the breakdown voltage of the bulk silicon device. This is because the SOI device has both a lower off-state breakdown voltage and a higher body resistance. In the SOI device, the body contact resistance is increased by the constriction of the p-type body contact by the buried oxide. Higher body contact resistance hurts on-state breakdown, caused by the turn-on of the parasitic n-p-n transistor that is embedded in an NMOSFET [16].

The S-parameters of the devices were measured to 6 GHz using an HP8753 network analyzer. Fig. 3 shows the f_t and $f_{\max}$ as a function of the gate finger width for a drain bias of 3.6 V. In these measurements, parasitic pad capacitances were de-embedded using a dummy pad structure and f_t and $f_{\max}$ of the devices were calculated by extrapolating from 6 GHz at a 20 dB/decade slope from the short circuit current gain (h_{21}) and

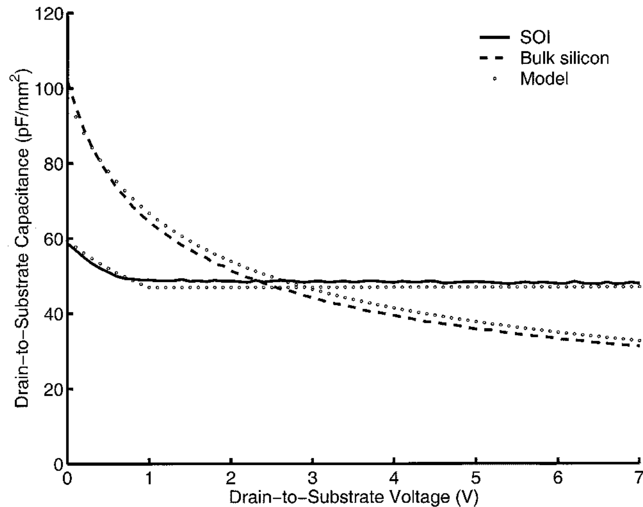


Fig. 4. Experimental and modeled drain-to-substrate capacitance of the SOI and bulk silicon LDMOSFETs.

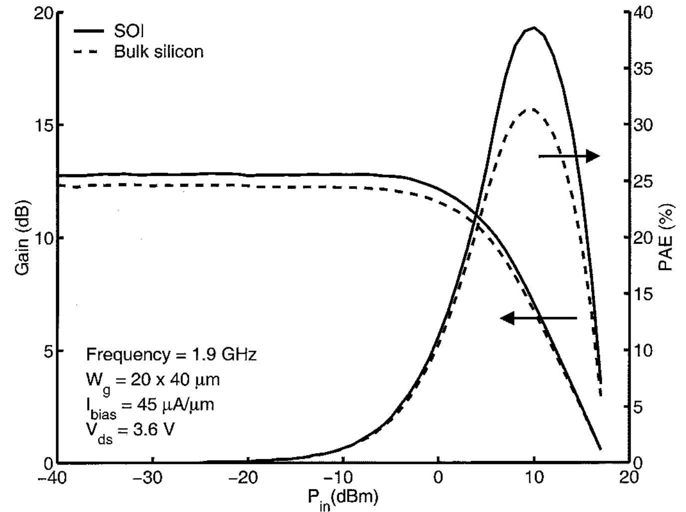


Fig. 5. Load-pull characteristics of the devices at 2 GHz. The source is conjugately matched and the load is set for maximum PAE.

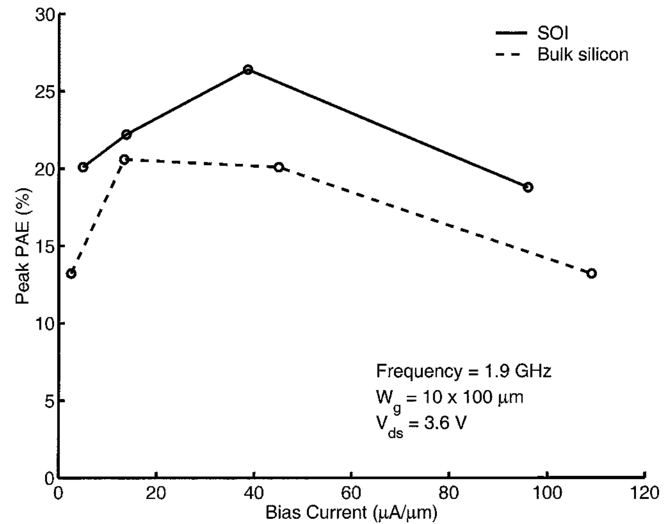


Fig. 6. Dependence of the peak PAE on the bias current for bulk and SOI LDMOSFETs. The PAE of the SOI device is systematically higher.

the maximum available power gain (g_{ma}), respectively. The f_t and $f_{\max}$ of the SOI devices were almost identical to those of the bulk silicon devices. As expected from first-order theory, f_t of the device is not a function of the gate finger width. On the other hand, $f_{\max}$ rolls off in an inverse linear manner with the gate finger width, indicating that the resistance of the polysilicon gate dominates the power gain.

The drain-to-substrate capacitance of the devices was measured with an HP4192, at 100 MHz, and is shown in Fig. 4. In RF power amplifier applications, low drain capacitance increases power efficiency due to reduced parasitic power loss and decreases the difficulty of designing the device's output matching network. As is seen in the figure, the SOI device and the bulk silicon device have substantially different drain-substrate capacitance behavior. A simple analytical model, derived directly from Poisson's equation and appropriate boundary conditions, correctly predicts the behavior of the capacitance. The substrate doping level used in the model of the bulk silicon and SOI devices is 1×10^{15} cm^{-3} and 7×10^{14} cm^{-3}, respectively, both within the 10–20 Ω-cm resistivity specification of the wafers. The bulk device's drain capacitance has the expected $1/\sqrt{V_D}$ dependence of a reverse biased p-n-junction. The SOI device has a $1/\sqrt{V_D}$ dependence for low voltages and flattens out at higher voltages due to inversion of the silicon beneath the buried oxide.

Load-pull measurements were performed at 1.9 GHz using an ATN load-pull system from Agilent Technologies. The results for devices with 20 fingers with a gate finger width of 40 μm per finger (20 $\times$ 40 μm) are shown in Fig. 5. The source was conjugately matched, and the load was matched to maximize the PAE. The drain voltage was 3.6 V, and the bias current was set for Class-A operation. The gain of the SOI and bulk devices is similar, but the PAE of the SOI device is substantially higher than the bulk silicon PAE, by almost 10% points.

The PAE advantage of the SOI devices was consistently observed for devices of many different layouts and at several different current bias conditions. The PAE as a function of the bias current is shown in Fig. 6 for devices with 10 $\times$ 100 μm gates. The PAE of the SOI device is systematically higher than the PAE of the bulk device.

Throughout our measurements, there were few indications of detrimental self-heating effects, commonly cited as a disadvantage of SOI in RF power applications. The comparison of the SOI and bulk silicon load-pull measurements shows that self-heating effects do not limit the performance of the SOI devices for the power densities that we studied.

IM3 of the devices was measured with 100 MHz signal spacing, and the results are shown in Fig. 7. Within the conditions that have been studied, the linearity of the two devices as indicated by IM3 is identical.

IV. Discussion

The measurements described in the previous section demonstrate that the performance of an SOI LDMOSFET is largely similar to an equivalent bulk silicon LDMOSFET. However, two significant differences were shown. The SOI device has substantially higher PAE, but the on-state breakdown voltage is lower. These two differences are discussed in this section.

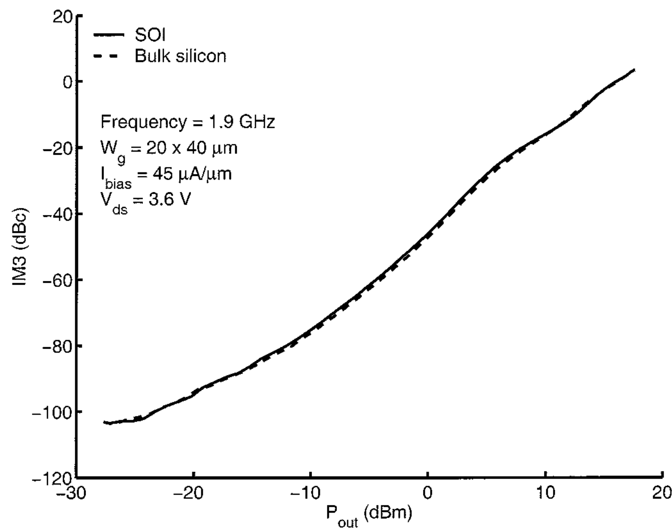
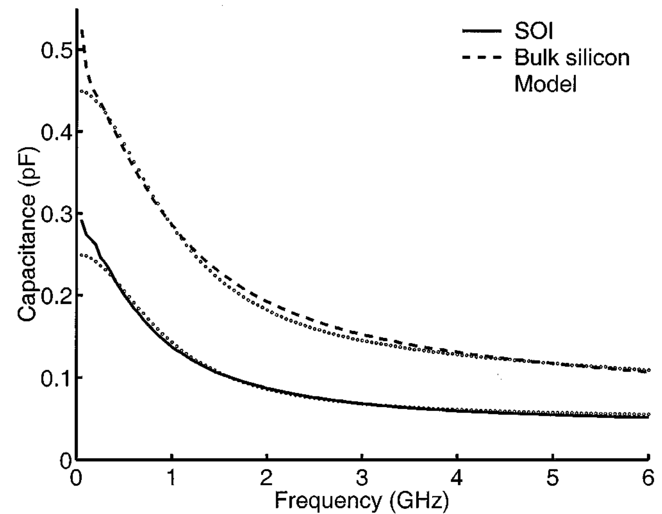
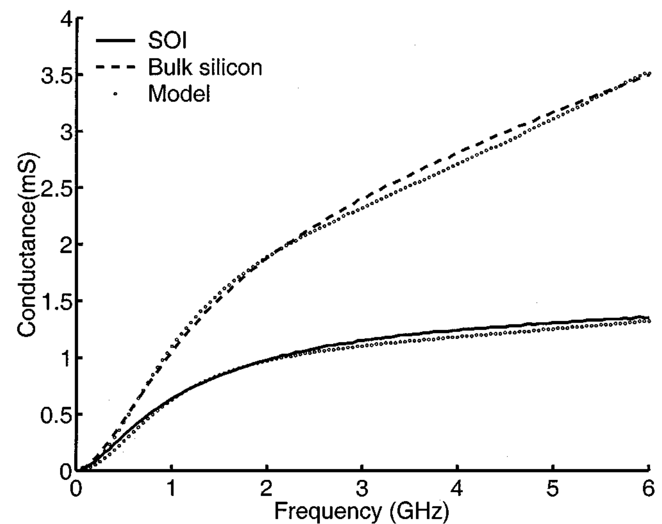


Fig. 7. Dependence of the third-order intermodulation distortion on the output power.



(a)



(b)

Fig. 8. Experimental and modeled (a) capacitance and (b) conductance of a drain pad as a function of frequency.

The on-state breakdown voltage achieved in the SOI LDMOSFETs is excellent, considerably higher than what has been achieved in other published thin-film RF LDMOSFETs. Additionally, the kink effect is entirely suppressed. The reason for this is the usage of the under source body contact. Its resistance is considerably lower than other body contacting schemes. However, the on-state breakdown voltage is substantially higher in the bulk device. The difference in on-state breakdown is both because the bulk device has a higher off-state breakdown voltage and because the SOI device has a higher body resistance. Adjusting the n^- LDD dose will eliminate the difference in the off-state breakdown voltage. The increase in the body resistance is caused by the constriction of the p-type body contact between the n^+ implant and the buried oxide. This is an intrinsic disadvantage of the SOI structure relative to bulk silicon.

The 10 V on-state breakdown of the SOI devices may deliver the ruggedness (resistance to breakdown at high output impedance mismatch) that is desired in PAs, but a lower body resistance may be required. The body resistance can be substantially reduced below the levels that were achieved in this work by optimization of the body doping process, but it is unknown if the low levels of body resistance that are achieved in bulk devices can be achieved in thin-film SOI. Further study is required to understand these issues.

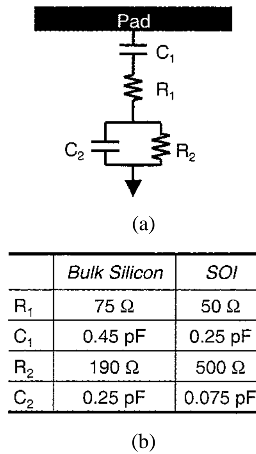
A specific advantage of SOI LDMOSFET technology is revealed in this work. The SOI devices have substantially higher PAE, and we have found that this improvement is related to the pads. Metal pads exist in the layout of the device to enable on-wafer probing. Similar structures are present in the layout of all RF power devices, most often as bond pads or to connect to other devices. These parasitic elements can be large. For example, on the 20 $\times$ 40 μm bulk silicon LDMOSFET in this work, the output pad capacitance is approximately 30% of the total output capacitance. These pads consume a significant amount of power and affect the power efficiency.

To study the pad issues, S-parameters of the gate and drain pads were measured using open test structures. The S-parameters of the pads are not a function of the DC voltage at which the pads were measured. The capacitance and conductance of the pads were extracted from the Y-parameters of the drain pads and are plotted in Fig. 8. Measurements obtained on the gate pads exhibit similar behavior.

Pads reduce the efficiency and gain of an amplifier because they are lossy and consume power. The "lossiness" of a pad is directly related to its conductance. As can be seen from Fig. 8, the pads on SOI have a significantly lower conductance, indicating that the SOI pads have lower loss.

A small-signal lumped circuit model of the pads was created to understand their behavior. The topology of the model is shown in Fig. 9. The values of the elements of the model were determined by fitting to the S-parameter data. The fit of the model to the capacitance and conductance measurements is shown in Fig. 8. The extracted element values are shown in Fig. 9. The model reveals that the pads on SOI have a lower series capacitance and higher parallel resistance.

The reason for the differences between the pads on SOI and bulk silicon is clear when the structure of the layers beneath the



	Bulk Silicon	SOI
R1	75 Ω	50 Ω
C1	0.45 pF	0.25 pF
R2	190 Ω	500 Ω
C2	0.25 pF	0.075 pF

(b)

Fig. 9. (a) A lumped circuit model of a pad and (b) the extracted values of the model elements.

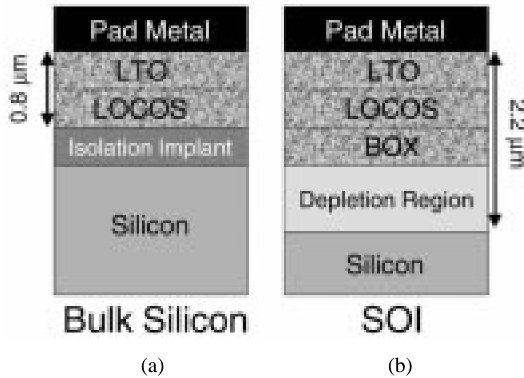


Fig. 10. Cross-section of the layers beneath pads on (a) bulk silicon and (b) SOI.

pads is examined. Fig. 10 depicts the region beneath the pads on the two wafer types. On the bulk silicon wafer, the pad metal is separated from the substrate by an LTO oxide and a LOCOS oxide. On the SOI wafer, there is an additional buried oxide. The surface of the bulk silicon wafer beneath the buried oxide is highly doped by the isolation implant. However, the surface of the SOI wafer remains lightly doped because the isolation implant is stopped by the buried oxide and does not reach the silicon surface. This allows a depletion region to form at the surface of the silicon in the SOI wafer. As a result, the capacitance of a pad on SOI is substantially lower than on bulk silicon and the absence of the isolation implant makes the SOI substrate more resistive. Both of these factors contribute to reducing the loss of the pad on SOI.

MEDICI simulations confirmed this understanding of the pad loss on SOI and bulk silicon. Two-dimensional (2-D) simulations of the pads shown in Fig. 10 were conducted. Fig. 11 shows the simulated real part of the y-parameters of the pads on SOI and bulk silicon. The MEDICI simulations correctly reflect the difference in the loss between the pads on SOI and bulk silicon, as well as the variation of the conductance with frequency. Fig. 11 also shows the results of a simulation in which the isolation implant that was used in the LOCOS process is removed. As can be seen, this implant plays a key role in the high conductance of the pads on bulk silicon.

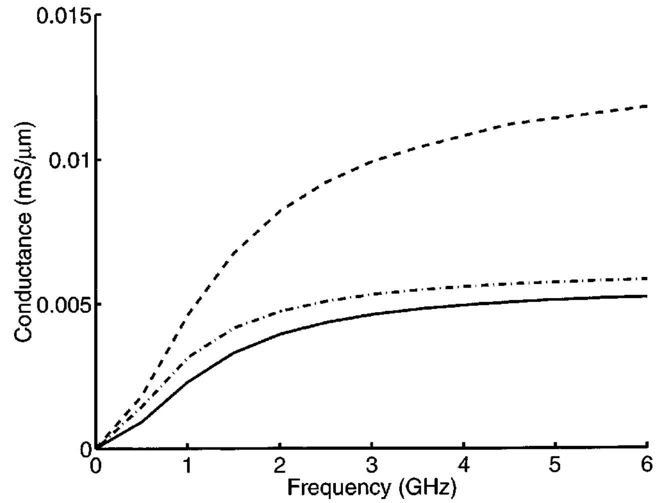


Fig. 11. Two-dimensional (2-D) MEDICI simulations of pads on bulk silicon and SOI. For bulk silicon, a simulation is shown indicating the effect of elimination of the isolation implant.

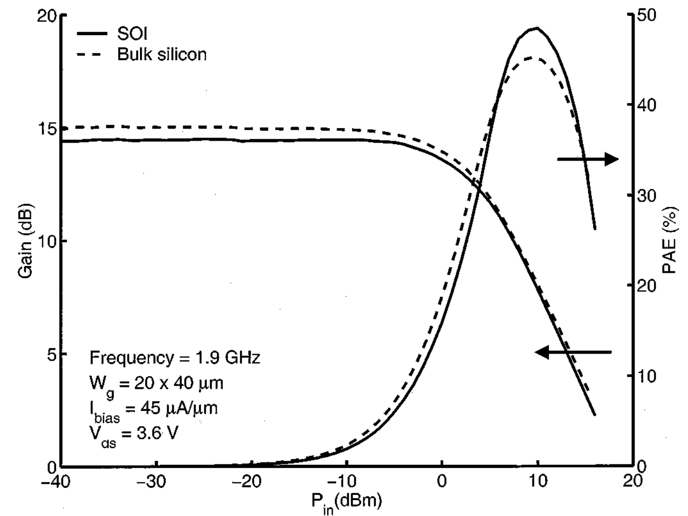


Fig. 12. Experimental data from Fig. 5 with parallel pad loss de-embedded.

The difference in pad loss on SOI and bulk silicon accounts for a large part of the difference in the PAE that have been observed between the two devices. To demonstrate this, the pads were de-embedded from the load-pull data using the pad S-parameter measurements. The relationship between the applied available input power (P_{inav}) and the de-embedded input power (P'_{inav}) is

$$P'_{inav} = P_{inav} \times \frac{G_{MS}}{G_{MS} + G_{PS}}. \quad (1)$$

G_{MS} is the conductance or the real part of the Y-parameters of the source-matching impedance, and G_{PS} is the conductance of the source pad. The relationship between the output power P_{out} and the de-embedded output power (P'_{out}) is

$$P'_{out} = P_{out} \times \frac{G_{ML} + G_{PL}}{G_{ML}}. \quad (2)$$

G_{ML} is the conductance of the load-matching impedance, and G_{PS} is the conductance of the load pad. These relations explic-

itly show the importance of the real parts of the pad Y-parameters on understanding pad power loss.

De-embedded load-pull measurements corresponding to the data in Fig. 5 are shown in Fig. 12. With the pads de-embedded, the gain of the SOI device is slightly lower than that of the bulk device. The de-embedded PAE of the bulk device nearly reaches that of the SOI device. The de-embedded results show that much of the improvement of the PAE of the SOI devices fabricated in this work is indeed due to reduced lossiness of the pads on the SOI substrate.

The quantitative improvement in power efficiency of an RF LDMOSFET on SOI will vary depending on the details of the device layout and pad implementation. Increasing the thickness of the dielectric under the pads or shrinking the size of the pads will reduce pad loss. However, this paper suggests that the pads on SOI will generally be less lossy.

V. Conclusions

We have simultaneously fabricated LDMOSFETs on bulk silicon and thin-film SOI wafers. We have compared their DC I–V, C–V, S-parameter, and load-pull characteristics. The performance of the LDMOSFET on a standard thin-film SOI wafer is similar that of an equivalent bulk silicon LDMOSFET. Although the on-state breakdown voltage of the SOI device is lower because of increased body resistance, its power efficiency is higher than that of an equivalent bulk silicon LDMOSFET because of reduced pad loss. The comparison of a thin-film SOI LDMOSFET to a proven RF power technology demonstrates the promise of thin-film SOI technology for future highly integrated RF power applications.

Acknowledgment

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