Technologies for RF Power LDMOSFETs Beyond 2 GHz: Metal/poly-Si Damascene Gates and Low-Loss Substrates

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Abstract

This work studies technologies to extend the frequency range of RF power LDMOSFETs. A metal/poly-Si damascene gate with a very low resistance was developed in an effort to reduce gate loss. Using this technology, three alternatives for reducing RF substrate loss were critically examined: high-resistivity bulk Si, SOI, and high-resistivity SOI. LDMOSFETs on all three low-loss substrates are shown to have higher PAE than LDMOSFETs on bulk silicon. The effectiveness of high resistivity SOI, however, was found to be limited by the formation of an inversion layer at the buried oxide/handle wafer interface. The combination of metal/damascene gates and low-loss substrates enables high PAE with long gate fingers at frequencies up to 4 GHz.

Introduction

LDMOSFETs are widely used today in 900 MHz and 1.9 GHz RF power amplifiers [1]. However, wireless applications at higher frequencies are rapidly developing. Technology innovations are needed to enable LDMOSFETs to address these markets.

This work focuses on the two most important sources of RF loss in LDMOSFETs: the gate and the substrate. A metal/poly-Si gate was developed to provide a very low gate resistance. LDMOSFETs using this gate were fabricated on three types of low-loss substrates. This paper evaluates these technologies for their potential to extend the frequency range of RF power LDMOSFETs.

Previous work in this area has demonstrated good performance at high frequencies by: a) reducing finger length [2], which lowers gate resistance but limits output power, or b) scaling gate length and gate oxide thickness and/or reducing drift length [3], [4], which increases RF performance at high frequencies but worsens reliability and ruggedness. Previous studies of low-loss substrates, including high-resistivity bulk silicon (HRS) [5], SOI [2], and high-resistivity SOI (HRSOI) [2], were inconclusive. Low-loss substrates have been shown to significantly improve the performance of passive RF components [5], but the benefit of a low-loss substrate to an RF LDMOSFET has not been clearly shown.

Process Technology

The LDMOSFETs fabricated in this work are based on the process described in [6] to which a metal/polysilicon damascene gate was added. Metal/poly-Si damascene gates are promising for digital CMOS [7], but they have never before been used in RF power applications. They have many advantages; they are self-aligned, they are implemented in the back-end of a process, and they have very low sheet resistance.

Our fabrication process is shown in Fig. 1 and a SEM picture is shown in Fig. 2. For reference, devices with standard n^+ poly-Si gates were also fabricated. Devices were built on four kinds of p-type wafers: standard bulk silicon (10-20 Ω-cm), HRS (2 kΩ-cm), SIMOX thin-film (CMOS compatible) SOI (10-20 Ω-cm), and 'Smart Cut' thin-film HRSOI (2 kΩ-cm). The layout includes RF test devices with two gate fingers and RF power device cells with 36 fingers. The nominal gate length of the LDMOSFETs was 0.6 μm. Devices were fabricated with either a 20 nm or a 30 nm gate oxide thickness.

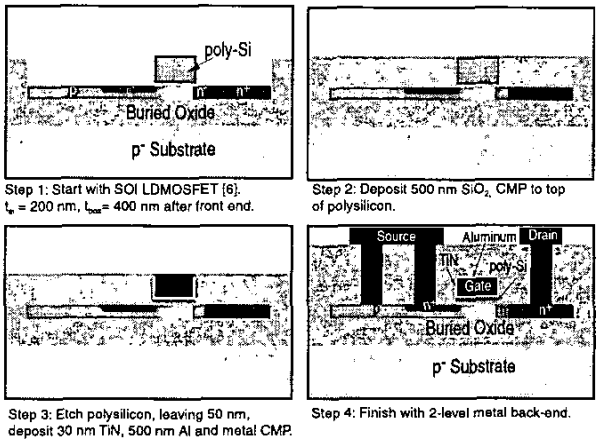

Fig. 1. Fabrication process of the metal/poly-Si damascene gate LDMOSFET. Basic LDMOSFET process described in [6].

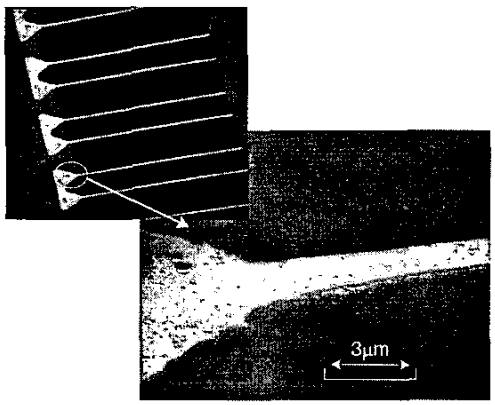

Fig. 2. SEM picture of damascene gate directly after metal CMP. Picture shows top view of a multi-finger RF power cell.

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Results and Discussion

The devices are examined using DC and CV measurements, S-parameters, and load-pull measurements. The load-pull measurements were done with an ATN system, using class-AB bias, and matching for maximum PAE. Unless specified otherwise, all data is from LDMOSFETs with a 30 nm gate oxide.

A. Metal/poly-Si Damascene Gate

Output characteristics of a 36 × 90 μm metal/poly-Si damascene gate LDMOSFET on HRSOI are shown in Fig. 3. The DC characteristics of the LDMOSFETs on the other wafers were similar. The use of an under-source body contact [6] suppressed the kink and enabled a high breakdown voltage.

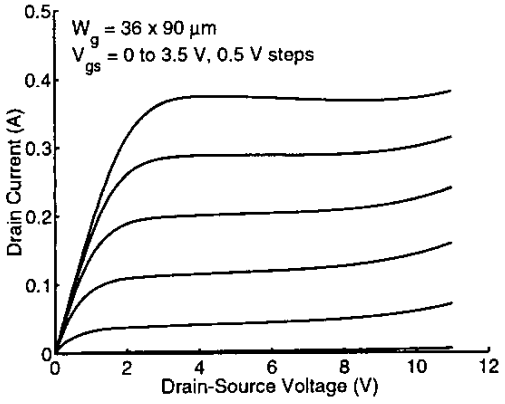

Fig. 3. DC output characteristics of damascene gate LDMOSFET on HRSOI. For LDMOSFETs on all wafers, $BV_{on} > 11V$, $BV_{off} > 19V$.

Fig. 4 shows the gate sheet resistance. The gate had a 0.2 Ω/sq. sheet resistance, 50 times lower than n^+ poly-Si, and 5 times lower than the tungsten silicide gate of state-of-the-art RF LDMOSFETs [1]. Figs. 5 and 6 compare the RF performance of damascene gate LDMOSFETs to that of identical devices with n^+ poly-Si gates. The low resistance of the damascene gate translates directly into high f_{max} and high peak PAE. The advantage of the damascene gate is especially prominent for long fingers, essential for RF power applications.

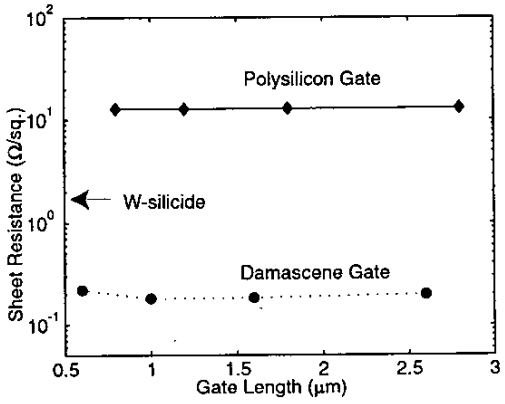

Fig. 4. Sheet resistance of metal/poly-Si damascene gate. Resistance of 0.2 Ω-cm was achieved, 5 times lower than W-silicide from a state-of-the-art RF LDMOSFET process [1].

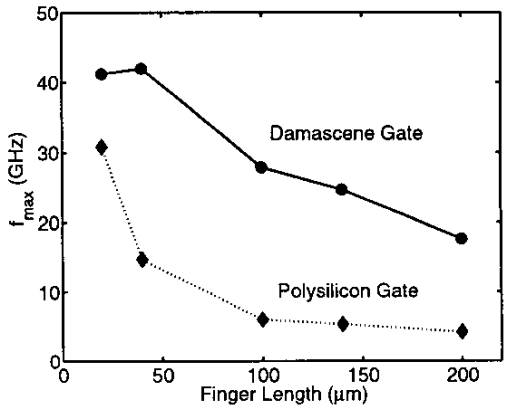

Fig. 5. Comparison of the f_{max} of two-fingered LDMOSFETs on SOI with a polysilicon gate and with a metal/poly-Si damascene gate. V_{dd} = 3.6 V, V_{gs} set at maximum g_m.

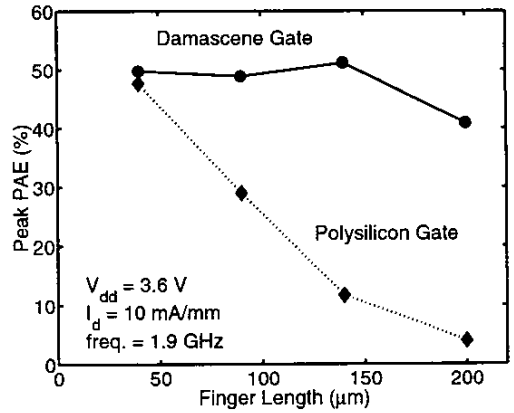

Fig. 6. Comparison of the peak PAE of 36-fingered LDMOSFETs on SOI with a polysilicon gate and with a metal/poly-Si damascene gate.

B. Low-Loss Substrates

Fig. 7 shows the peak PAE at 1.9 GHz of LDMOSFETs on bulk Si and the three different low-loss substrates. The LDMOSFET on SOI has higher PAE than the LDMOSFET on bulk Si, confirming the result obtained in [6]. The LDMOSFET on HRS has significantly improved PAE compared to the LDMOSFET on bulk Si, and it also has higher PAE than the LDMOSFET on SOI. Interestingly, the use of a high-resistivity handle wafer with SOI does not improve the PAE. This last result mirrors the finding in [2].

These results can be understood using the small-signal model shown in Fig. 8. PAE is degraded by substrate loss from two sources: loss from the n^+ drain to the substrate ("drain loss") and loss from the drain metal interconnects and pad to the substrate ("drain pad loss"). These two sources of substrate loss are described in the model by separate networks connected to the drain node. From the model, we extracted the substrate loss (Re(Y(1.9 GHz))) associated with the drain and drain pad for 2 × 100 μm test devices. These devices were used (instead of the 36 finger power cell) because the losses can be more accurately extracted from small devices. Fig. 8 shows the losses for each substrate type. All three low-loss substrates have both lower drain loss and lower drain pad loss than bulk Si. The use

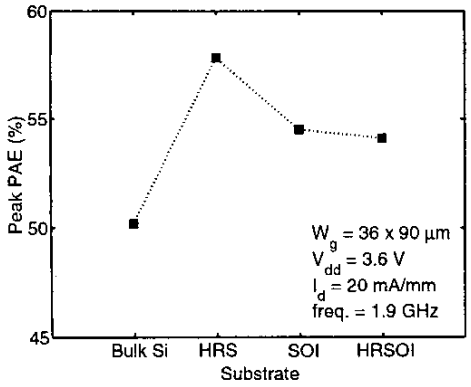

Fig. 7. Peak PAE of LDMOSFETs on four different substrates: bulk Si (10 - 20 Ω-cm), high-resistivity bulk Si (2 kΩ-cm), SOI (10 - 20 Ω-cm), and high-resistivity SOI (2 kΩ-cm).

of high-resistivity silicon reduces drain pad loss on SOI significantly, but only moderately on bulk Si. This is believed to be because of the presence of the isolation implant, as discussed in [6]. The 36 × 90 μm cells are affected more by drain loss than by drain pad loss. Interestingly, the use of a high-resistivity substrate decreases drain loss significantly for bulk Si, but only slightly for SOI. This result explains why the PAE of HRS is improved over bulk Si, but the PAE of HRSOI is not improved over SOI.

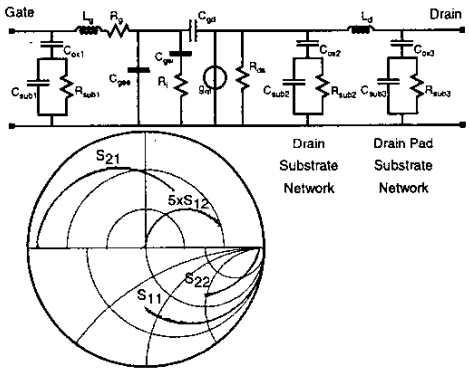

Fig. 8. Small-signal model of a 2 × 100 μm RF LDMOSFET. Typical fit of model S-parameters (de-embedded) is shown. Data is for an LDMOSFET on SOI. V_{dd} = 3.6 V. Frequency range is 50 MHz to 20 GHz.

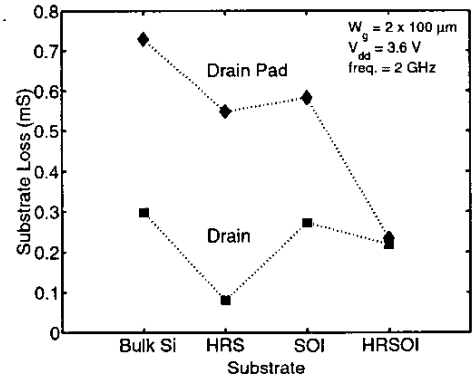

Fig. 9. Substrate loss of the drain and drain pad of LDMOSFETs as a function of substrate type. Devices are 2 × 100 μm. V_{gs} is at maximum g_m.

We postulate that drain loss is insignificantly reduced on HRSOI relative to SOI because of the existence of an inversion layer at the substrate/buried oxide interface. Surface inversion has been previously reported to increase the loss of transmission lines on HRS [8], but its impact on RF power SOI LDMOSFETs has not been recognized. Fig. 10 shows the capacitance on an HRSOI wafer of a n^+/buried oxide/handle wafer test structure as a function of the substrate voltage. For a low or a high substrate voltage, the substrate inverts or accumulates. Inversion or accumulation causes an increase in the drain substrate loss and thus reduces peak PAE. This is observed in S-parameter and load-pull measurements as a function of the substrate bias, shown in Fig. 11. Under normal operation conditions (zero substrate voltage) the silicon under the buried oxide is inverted. This inversion layer shunts RF current to ground, increasing loss, and muting the benefit using of a high-resistivity handle wafer for SOI. Surface inversion does not impact *drain pad* loss because of the large lateral distance between the pad and an adjacent ground.

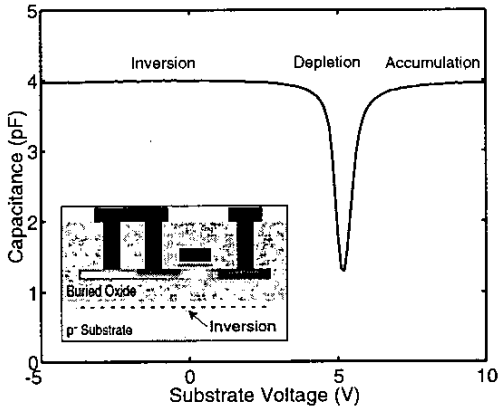

Fig. 10. Capacitance of a 100 μm square n^+/buried oxide/handle wafer test structure on HRSOI. Low or high substrate bias inverts or accumulates the silicon surface beneath the buried oxide. Measurement frequency = 100 kHz. X-axis is shifted by 3.6 V to account for the drain bias of the load-pull measurements.

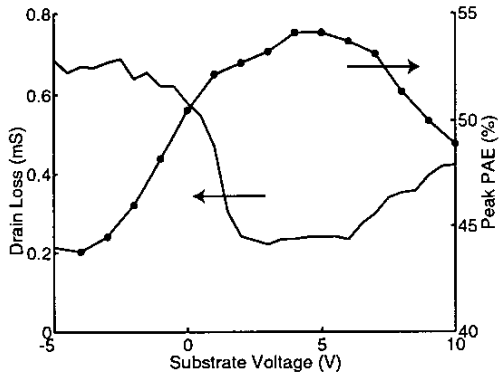

Fig. 11. Conductance of a 2 × 100 μm LDMOSFET and peak PAE of a 36 × 90 μm LDMOSFET as a function of the substrate voltage on HRSOI. Surface inversion or accumulation increases drain loss and decreases the PAE. Gate oxide thickness was 20 nm. For both measurements freq. = 3 GHz, V_{dd} = 3.6 V.

C. Performance Beyond 2 GHz

Fig. 12 shows peak PAE as a function of frequency for metal/poly-Si damascene gate LDMOSFETs on each of the substrates. The improvement of the PAE due to the low-loss substrates is larger at higher frequencies. Low-loss substrates are therefore key for high frequency operation of LDMOSFETs.

An LDMOSFET on HRSOI with a 20 nm gate oxide thickness achieved the highest performance of any device in this work (20 nm devices on HRS were not fabricated). Fig. 13 shows load-pull measurements of this device at 1.9, 3, and 4 GHz; and Fig. 14 shows a summary of the performance. The combination of the metal/poly-Si damascene gates and the HRSOI substrate yield excellent LDMOSFET performance beyond 2 GHz: PAE greater than 60 % at 1.9 GHz, greater than 50 % at 3 GHz and nearly 45 % at 4 GHz. This performance is seen even with large finger lengths, enabling high output power levels.

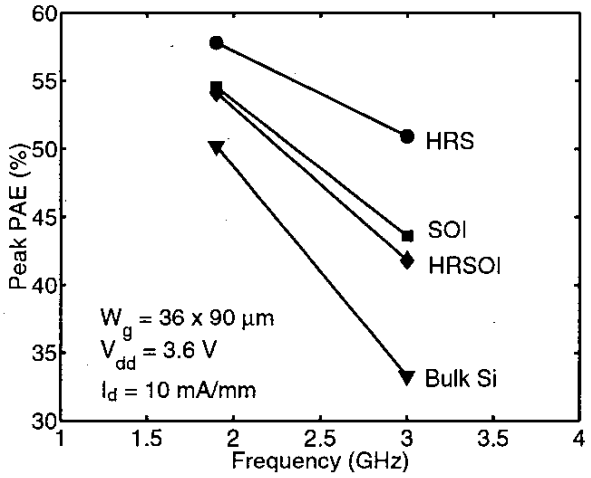

Fig. 12. Peak PAE as a function of frequency for metal/damascene gate LDMOSFETs on bulk Si and the three low-loss substrates.

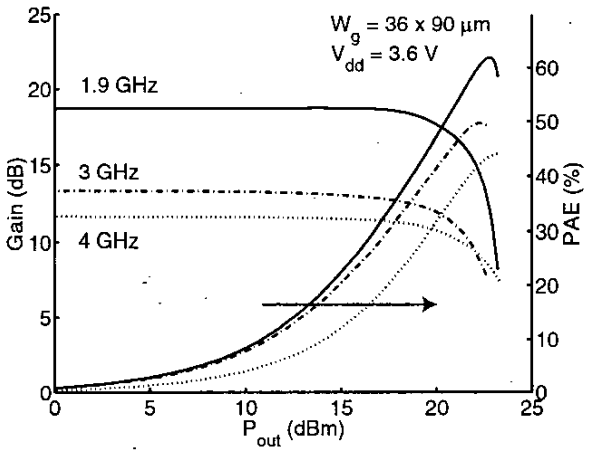

Fig. 13. Load-pull measurements of a 36 × 90 μm LDMOSFET on HRSOI at 1.9, 3, and 4 GHz. Gate oxide thickness was 20 nm. I_d = 10 mA/mm at 1.9, 3 GHz, and I_d = 20 mA/mm at 4 GHz.

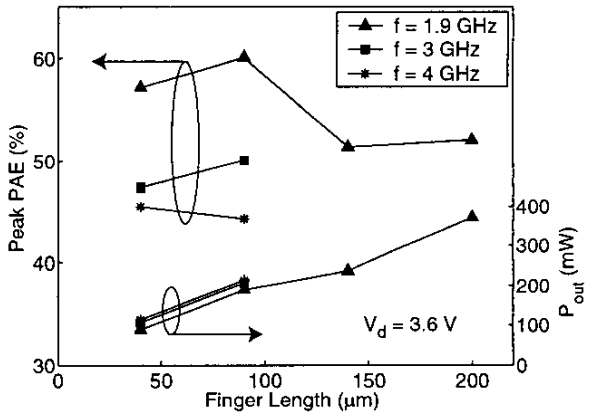

Fig. 14. Peak PAE of LDMOSFETs on HRSOI at 1.9, 3, and 4 GHz. High PAE was achieved at frequencies beyond 2 GHz and for large finger lengths. Gate oxide thickness was 20 nm. I_d = 10 mA/mm at 1.9, 3 GHz, and I_d = 20 mA/mm at 4 GHz.

Conclusion

In summary, this work studies two critical issues for extending RF power LDMOSFET operation beyond 2 GHz: gate resistance and substrate loss. We have developed metal/poly-Si damascene gates with a sheet resistance that was 5 times lower than state-of-the art W-silicide, and have shown that they are very effective in RF power applications. The work examines three alternatives for reducing substrate loss: high-resistivity silicon, SOI, and high-resistivity SOI. All three alternative substrates where shown to reduce substrate loss and improve PAE, though high-resistivity SOI was affected by inversion beneath the buried oxide. The combination of the metal/poly-Si damascene gate and low-loss substrates was shown to be a viable path to enable high efficiency, high power operation up to 4 GHz.

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References

[1] G. Ma, W. Burger, and M. Shields in *IEEE MTT-S Dig.*, pp. 1195–1198, 1999.
[2] S. Matsumoto and T. Sakai *TED*, vol. 48, pp. 2911–2916, Dec. 2001.
[3] K. E. Ehwald, B. Heinemann, W. Roepke, W. Winkler, H. Rucker, F. Fuernhammer, D. Knoll, R. Barth, B. Hunger, H. E. Wulf, R. Pazirandeh, and N. Ilkov in *IEDM*, pp. 895–895, 1996.
[4] S. Matsumoto, Y. Hiraoka, and T. Sakai *TED*, vol. 48, pp. 1270–1274, June 2001.
[5] T. Ohguro et al. in *IEDM*, pp. 757–760, 2000.
[6] J. G. Fiorenza and J. A. del Alamo *TED*, vol. 49, pp. 687–692, Apr. 2002.
[7] T. Matsuki, K. Kishimoto, K. Fujii, N. Itoh, K. Yoshida, K. Ohto, S. Yamasaki, T. Sinmura, and N. Kasai in *IEDM*, pp. 261–264, 1999.
[8] H. S. Gamble, B. M. Armstrong, S. J. N. Mitchell, Y. Wu, V. F. Fusco, and J. A. C. Stewart *IEEE Mic. Guided Wave Let.*, pp. 395–397, 1999.