Hydrogen sensitivity of InP HEMTs with WSiN-based gate stack

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Abstract

We have investigated the hydrogen sensitivity of InP HEMTs with a WSiN/Ti/Pt/Au gate stack. We have found that the impact of hydrogen on the threshold voltage of these devices is one order of magnitude smaller than conventional Ti/Pt/Au-gate HEMTs. This markedly improved reliability has been studied through a set of quasi-2D mechanical and electrostatic simulations. These showed that there are two main causes for the improvement of the H-sensitivity. First, the separation of the Ti-layer from the semiconductor by a thick WSiN layer significantly reduces the stress in the active layer. Additionally, the thinner heterostructure and the presence of an InP etch-stop layer with a small piezoelectric constant underneath the gate reduces the amount of threshold voltage shift that is caused by the mechanical stress.

I. Introduction

The goal of this research is to study the H-sensitivity of state-of-the-art InAlAs/InGaAs HEMTs specifically designed for ultra-high speed optical fiber communication systems [1]. H degradation has been identified as a reliability concern in III-V MESFETs [2] and HEMTs [3]. H is known to alter the electrical characteristics of the devices ultimately leading to parametric failure. One of the paths through which H affects III-V FETs is the formation of TiH_x in the Ti/Pt/Au gate stack [4]. This creates tensile stress in the heterostructure underneath which through the piezoelectric effect causes a threshold voltage shift.

In InP HEMTs with a Ti/Pt/Au gate stack, the experimentally observed H-induced threshold voltage shifts can be very substantial dependent on the gate length (Fig. 1). Since the Ti-layer is currently thought to be the source of the stress, the introduction of WSiN at the bottom of the gate stack is expected to mitigate H sensitivity by separating the Ti-layer from the heterostructure. However, to date, no data has been reported that can shed light on this hypothesis. The goal of this work is to study the H sensitivity of InP HEMTs with a WSiN/Ti/Pt/Au gate stack [1] and to compare it to that of more conventional Ti/Pt/Au gate stack designs.

II. Experiments

A cross-section of the investigated InP HEMTs is shown in Fig. 2. In contrast with conventional InP HEMTs, these devices feature a WSiN/Ti/Pt/Au gate stack and an InP gate recess etch-stop layer in the intrinsic heterostructure [1].

In studying the H sensitivity of these devices, we have followed a methodology similar to that of [4]. The experiments basically consist of three phases. First, the devices were baked in N_2 at 195°C for over 60 hours to saturate all thermally induced effects. In a second phase, the thermal stability was evaluated by baking the devices again at 195°C for 2 h under N_2. Finally, the devices are baked at 195°C for 2h [4] in forming gas. This allows us to compare the effects of a 2-hour thermal bake in N_2 and H_2 and thus estimate the H effects in a single device. A few devices were monitored in-situ during the N_2 and H_2 anneals (V_T was measured at regular intervals). In some cases, after the forming gas bake, we evaluated the effect of a 2h recovery anneal in N_2 at 200°C.

Device characterization was carried out at room temperature before and after every phase. For this purpose, we developed a rather "benign" device characterization test suite that does not affect the device characteristics. This characterization suite involves measurements of the parasitic resistances, the output, transfer and subthreshold characteristics and the threshold voltage.

The studied devices had gate lengths between 30 nm and 1 µm. The devices have been designed and optimized for the $[01\bar{1}]$ gate orientation, but there were also devices along the [011] direction. Fig. 3 shows the transfer characteristics of a 0.1 µm device with a $[01\bar{1}]$

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orientation, after 60 h pre-bake in N_2 at 195°C, and after subsequent 2 h bakes in N_2 and H_2 at 195°C. The effect of H exposure is mostly a shift in V_T.

Fig. 4 shows the time evolution of V_T for a 0.1 μm InP HEMT with a $[01\bar{1}]$ gate orientation in-situ during N_2 anneal, H_2 exposure and N_2 recovery. It clearly shows that V_T shifts negatively during the forming gas anneal, while it is largely unaffected by the bakes in a N_2 atmosphere at the same temperature. Also, the impact of H_2 is basically saturated after about 50 minutes of exposure to forming gas. Furthermore, there is no indication of any recovery in a post-H exposure N_2 anneal.

For the standard devices with a $[01\bar{1}]$ gate orientation, Fig. 5 shows ΔV_T as a function of the gate length. N_2 treatment seems to shift V_T slightly positive. H_2 treatment causes a distinct and statistically significant negative ΔV_T, which is largest in magnitude for the 0.1 μm devices. Fig. 6 shows ΔV_T in devices with a [011] gate orientation under identical conditions. Here, N_2 treatment also causes a small ΔV_T. The H_2 bake causes a negative shift with a gate length dependence that is almost a mirror image of that of Fig. 5, except that it is shifted by about –8 mV.

The maximum value of ΔV_T for short gate length devices is of the order of 15 to 20 mV. This is about an order of magnitude smaller than previous observations on InP HEMTs of this gate length under similar conditions [6-8] (Fig. 1).

III. Simulation

In order to understand these results, we have carried out device simulations using the techniques described in [5] which involve 2D finite element simulations using ABAQUS and 1D electrostatics calculations using MATLAB. To compare with [5], we first simulated a "reference" device with a standard Ti/Pt/Au gate stack and a 2500 Å InAlAs/300 Å InGaAs/ 200 Å InAlAs (from bottom to top) layer structure [5]. Then we examined the impact of changing the heterostructure to a 2000 Å InAlAs/150 Å InGaAs/ 100 Å InAlAs/ 60 Å InP (from bottom to top) layer structure [9]. The main changes are a general thinning down of the heterostructure and the addition of an InP etch-stop layer. This is referred to as "improved heterostructure". Subsequently we added a thick WSiN layer at the bottom of the gate stack. The results of these simulations are shown in Figs. 7 for a [011] gate orientation. Identical results are predicted for the $[01\bar{1}]$ gate orientation, except for an opposite sign in ΔV_T.

Consistent with our measurements, we found that the InP HEMT with a WSiN-based gate-stack and an improved heterostructure exhibits a H-sensitivity that is about an order of magnitude smaller than the reference device (Fig. 7). There are two causes for this. The improved heterostructure is thinner and it contains an InP layer. Also, the gate includes a thick WSiN layer. We have separately studied the effects of these changes on the H-induced ΔV_T.

As Fig. 7 shows, by thinning the semiconductor structure from the reference device to a thinner heterostructure (2000 Å InAlAs/150 Å InGaAs/160 Å InAlAs), ΔV_T is reduced by about 20 %. The introduction of the 60 Å InP etch-stop layer, which has a very low piezoelectric constant, reduces ΔV_T by another 35 %. We find that with these two changes the improved heterostructure exhibits a decrease in H-sensitivity by more than a factor of 2 at short gate lengths when compared with the reference device.

The presence of the thick WSiN layer in the gate stack further lowers the H-sensitivity by about a factor of 3 at a gate length of 0.1 μm and even more at short gate lengths (Fig. 7). This is because the WSiN layer absorbs a large part of the stress caused by the expanding Ti-layer, which results in a reduction of the mechanical stress in the semiconductor by the same amount. This causes a proportional reduction of the piezoelectric polarization in the semiconductor and thus in ΔV_T. From our simulations, we have found that the thicker the WSiN layer, the more ΔV_T is reduced (Fig. 8).

The combined effect of all these changes is a reduction of ΔV_T by an order of magnitude. This is seen in Fig. 9 that shows the piezoelectric polarization across the heterostructure at the center of the gate as a function of the depth.

The simulated results shown in Fig. 7 for the advanced heterostructure with a WSiN gate can be compared to the experimental ones. This is shown in Fig. 10 where excellent agreement is found for the $[01\bar{1}]$ gate orientation after appropriate scaling of the simulations. Interestingly, the simulations not only predict a large and negative ΔV_T centered around 0.1 μm, but a marked H insensitivity for 30 nm devices, just as observed in the experiments.

By comparing Figs. 5 and 6 one sees that the shapes of the ΔV_T curves for the [011] and $[01\bar{1}]$ gate orientations are not exactly a mirror image of each another around the x-axis. There appears to be a rigid shift of about –8 mV to the ΔV_T for the devices with a [011] gate

orientation. We do not know the origin of this difference but it might be related to the fact that the fabrication process has been optimized for the [01$\bar{1}$] gate orientation.

IV. Conclusions

In summary, we have found that InP HEMT designs with a WSiN layer at the bottom of the gate stack and InP etch-stop layers inside the intrinsic heterostructure feature a hydrogen sensitivity that is about one order of magnitude smaller than conventional InP HEMTs.

Acknowledgements

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References

[1] T. Suemitsu et al., IEDM, p.191, 2000.

[2] E. Chang et al., IEEE TED, vol. 35, no. 9; p.1412, 1988.

[3] J.A. del Alamo et al., Trans. IEICE, Vol. E-84-C, no. 10, p.1289, 2001.

[4] R.R. Blanchard et al., IEEE Electron Device Lett., vol. 20, no. 8, p. 393, 1999.

[5] S.D. Mertens and J. A. del Alamo, IPRM, p. 452, 2001.

[6] R.R. Blanchard and J.A. del Alamo, IPRM, p. 79, 2000.

[7] P. Chao et al., IEEE Electr. Dev. Lett., vol. 15, no. 5, p. 151, 1994.

[8] M. Chertouk et al., IEEE Electr. Dev. Lett., vol. 21, no. 3, p. 97, 2000.

[9] T. Suemitsu et al., Electronics Letters, vol. 35, no. 24, p. 2141, 1999.

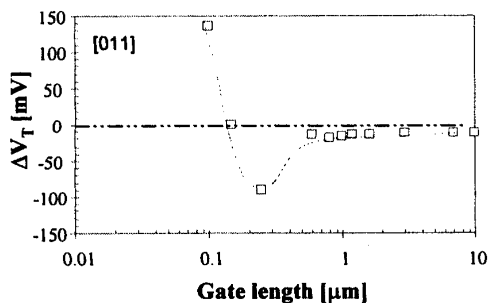

Fig. 1: Reported ΔV_T caused by hydrogen degradation as a function of gate length for InP HEMTs with Ti/Pt/Au gates oriented along the [011] direction [6-8].

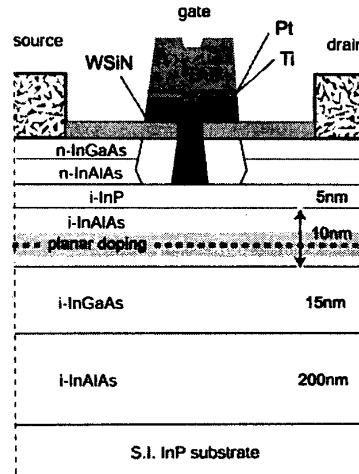

Fig. 2: Cross-section of InP HEMT studied in this work [1,9].

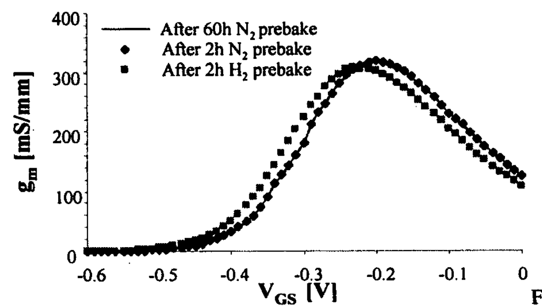

Fig. 3: Transfer characteristics of a 0.1 μm InP HEMT with a [01$\bar{1}$] gate orientation after 60 h prebake in N_2 at 195 °C, after a subsequent 2 h bake in N_2 at 195 °C and after another 2 h bake in forming gas at 195 °C (V_{DS}=0.1 V).

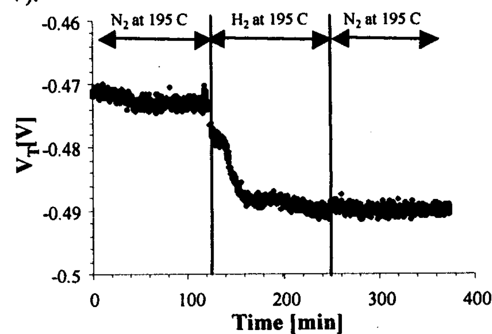

Fig. 4: Time evolution of V_T during a typical experiment. The device has a 0.1 μm gate length and a [01$\bar{1}$] gate orientation.

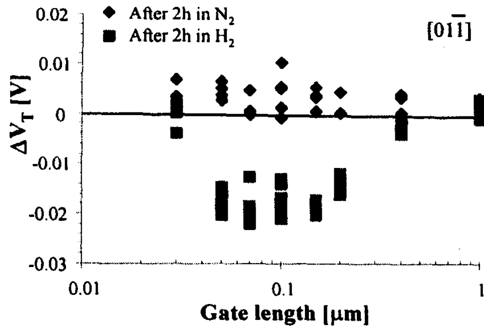

Fig. 5: Threshold voltage shifts caused by a 2h bake at 195°C in N_2 and in forming gas. The devices have a [01$\bar{1}$] gate orientation.

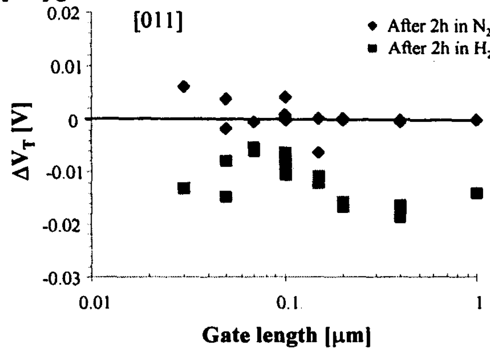

Fig. 6: Threshold voltage shifts caused by a bake at 195°C in N_2 and in forming gas. The devices have a [011] gate orientation.

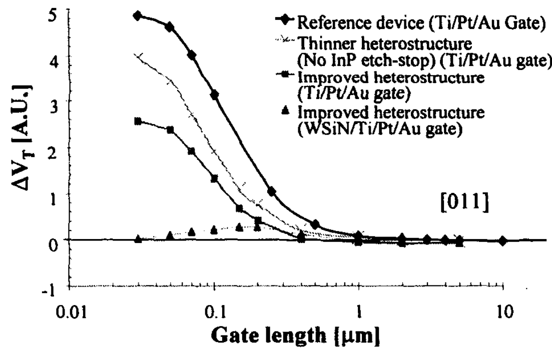

Fig. 7: Calculated ΔV_T vs. gate length for: 1) reference structure with Ti/Pt/Au gate; 2) improved heterostructure with Ti/Pt/Au gate, where the InP etch-stop layer is replaced by an InAlAs layer; 3) improved heterostructure with a Ti/Pt/Au gate, and 4) improved heterostructure with a WSiN/Ti/Pt/Au gate. Gate orientation is [011].

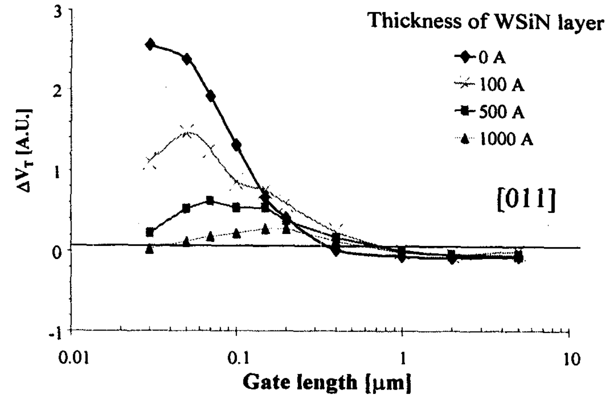

Fig. 8: Calculated ΔV_T vs. gate length for InP HEMTs with the improved heterostructure with a WSiN/Ti/Pt/Au gate for different thicknesses of the WSiN layer (0 Å, 100 Å, 500 Å and 1000 Å). Gate orientation is [011].

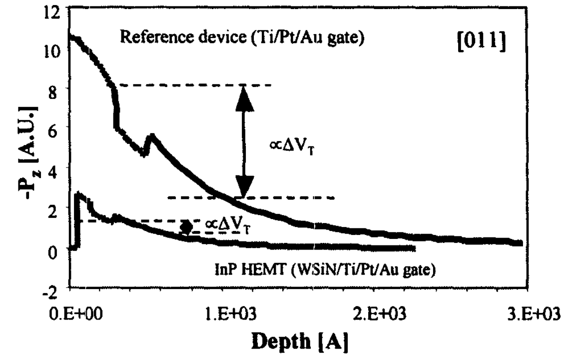

Fig. 9: Calculated piezo-electric polarization field at the center of the gate for reference InP HEMT with a Ti/Pt/Au gate and InP HEMT with WSiN in the gate stack. L= 0.1 μm. gate orientation is [011].

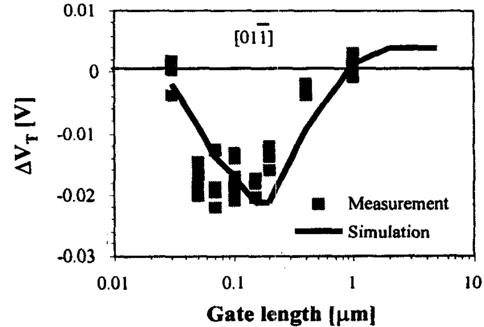

Fig. 10: Measured and simulated ΔV_T for the impoved InP HEMTs with a WSiN-based gatestack and InP etch-stopper. Gate orientation is [01$\bar{1}$].