Electrical Degradation of
InAlAs/InGaAs Metamorphic High-Electron Mobility Transistors

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Abstract

We have studied the electrical degradation of InAlAs/InGaAs Metamorphic HEMTs. The main effect of the application of a bias for an extended period of time is a severe increase in the drain resistance, R_D, of the device. We have identified two different degradation modes: a reduction in the sheet-electron concentration of the extrinsic drain and an increase of the drain contact resistance. Both mechanisms are found to be directly related to impact-ionization. The metamorphic nature of the substrate does not seem to play a role in the observed degradation.

Introduction

InAlAs/InGaAs metamorphic HEMTs hold great promise for 40 Gb/s photonics applications. A major reliability concern in these devices is the electrical degradation that occurs when the device is electrically stressed for a long time even at operating bias conditions. The main reported effect is an increase in the drain resistance R_D [1,2]. Several other device parameters, such as the threshold voltage, V_T, [3] and the source resistance, R_S, [4] have also been reported to degrade during bias stress. The R_D degradation has also been found to be related to impact-ionization [5], but the detailed
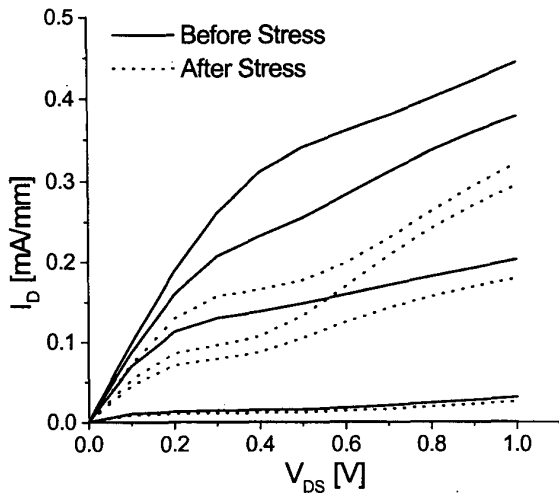

Fig. 1: Output characteristics before and after 714 minutes of stress at room temperature at a constant $V_{DGo}=1.5$ V and a constant $I_D=250$ mA/mm.
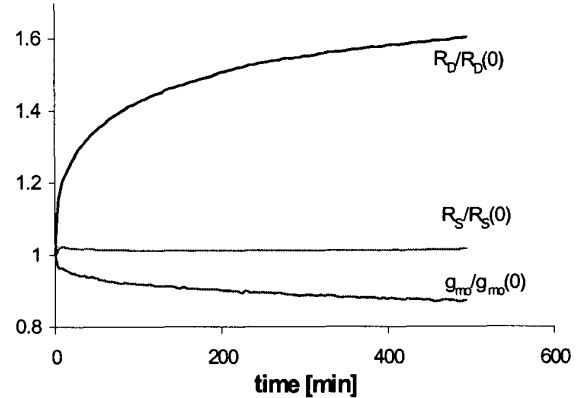

Fig. 2: Time evolution of the drain resistance R_D, source resistance R_S and intrinsic transconductance g_{mo} normalized to their initial values during stress at room temperature at a constant $V_{DGo} + V_T=1.6$ V and $V_{GS}-V_T = 0.3$ V.

degradation mechanism remains largely unknown. In metamorphic HEMTs, there is the additional concern of degradation associated with crystalline defects that might have propagated through the buffer.

In this work, we have investigated the electrical reliability of metamorphic HEMTs, by performing extensive degradation experiments on both HEMTs and TLMs. In these experiments we have measured the time evolution of a wide array of device parameters during bias stress degradation. By developing a physically meaningful degradation scheme, we have firmed up the connection between R_D degradation and impact-ionization. We have also identified two separate degradation mechanisms that take place in the extrinsic drain side of the device. In our work, we have not seen a direct connection between the metamorphic nature of the substrate and the electrical degradation of the devices.

Experimental results

A. HEMTs

InAlAs/InGaAs metamorphic HEMTs with a 0.12 μm gate length were stressed at room temperature. In order to investigate the connection between R_D degradation and impact-ionization, we developed a stressing scheme that keeps the impact-ionization rate constant. This was
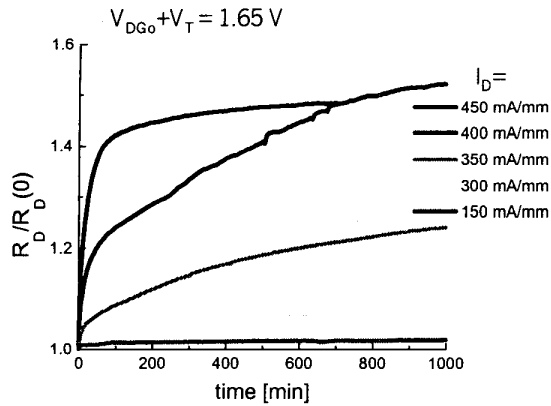
$V_{DGo}+V_T = 1.65\ V$

$I_D=$
— 450 mA/mm
— 400 mA/mm
— 350 mA/mm
300 mA/mm
— 150 mA/mm

Fig. 3: Time evolution of the drain resistance R_D, normalized to its initial value during stress at room temperature for different I_D at a constant $V_{DGo}+V_T=1.65\ V$.

accomplished by holding constant the sum of the intrinsic drain-to-gate voltage plus the threshold voltage, $V_{DGo}+V_T$ and either the drain current, I_D, or the gate voltage overdrive, $V_{GS}-V_T$ (both approaches yielded the same results). In this stressing scheme we continuously keep track of changes in V_T and R_D and adjusts the bias voltages in real time accordingly. During these stress tests, the devices were fully characterized at regular intervals.

Fig. 1 shows typical degradation in the I-V characteristics. Most figures of merit associated with the drain side of the device were found to degrade under bias stress, while the intrinsic portion did not degrade as much, and the source side was almost unaffected (Fig. 2). In particular, R_D was observed to increase significantly.

Conditions that yield a higher impact-ionization rate were found to cause a faster and more significant degradation of R_D. In FET's, impact-ionization is mainly controlled by I_D

$V_{DGo}+V_T=$
— 1.7 V
- - - - 1.6 V
...... 1.5 V
— · — 1.4 V
— ·· — 1.3 V
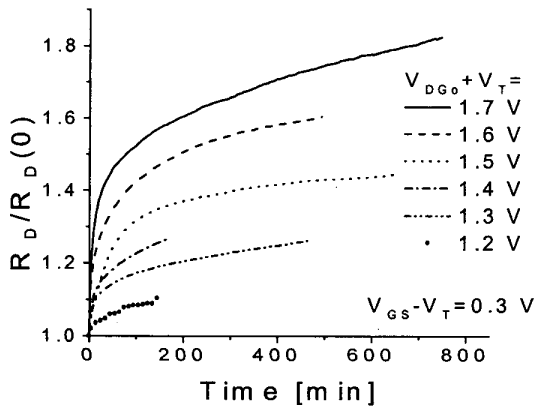· 1.2 V

$V_{GS}-V_T = 0.3\ V$

Fig. 4: Time evolution of the drain resistance, R_D, normalized to its initial value during stress at room temperature for different $V_{DGo}+V_T$ at a constant $V_{GS}-V_T=0.3\ V$.

$V_{DGo}+V_T=$
— 1.7 V
- - - - - 1.6 V
.... 1.5 V
— 1.4 V
— — 1.3 V
· 1.2 V

$V_{GS}-V_T = 0.3\ V$

Fig. 6: $BV_{DGoff}/BV_{DGoff}(0)$ vs. $R_D/R_D(0)$ during degradation for six devices stressed at room temperature at $V_{GS}-V_T=0.3\ V$ and $V_{DGo}+V_T=1.2\ V$ to 1.7 V.
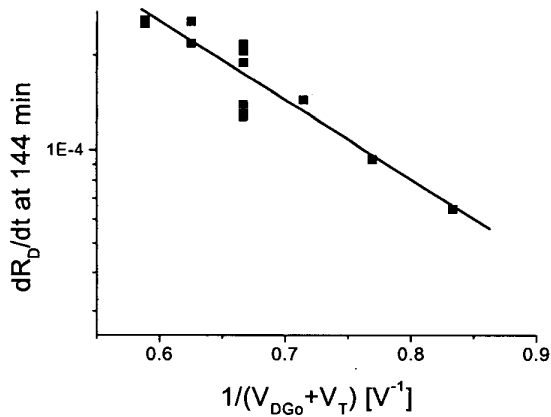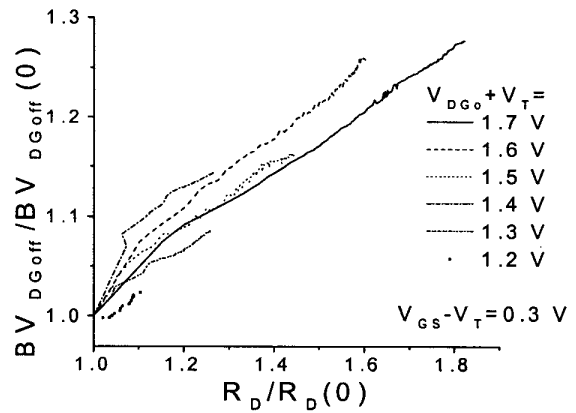

Fig. 5: Semi-log plot of the degradation rate dR_D/dt after 144 min, as a function of $(V_{DGo}+V_T)^{-1}$ for several devices that were stressed at room temperature at $V_{GS}-V_T=0.3\ V$ and a constant $V_{DGo}+V_T$.
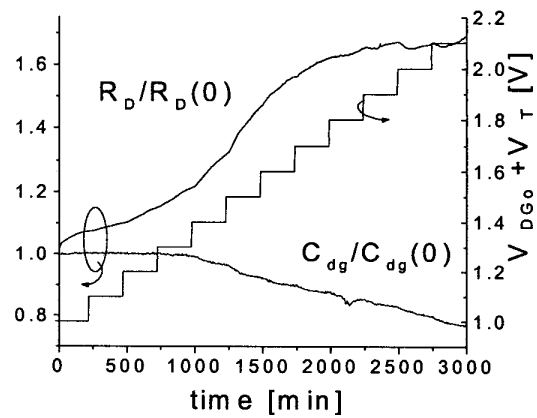

$R_D/R_D(0)$

$C_{dg}/C_{dg}(0)$

Fig. 7: Time evolution of $R_D/R_D(0)$ and $C_{dg}/C_{dg}(0)$ for a MHEMT stressed at room temperature at $V_{GS}-V_T=0.3\ V$ and $V_{DGo}+V_T=1$ to 2.1 V, stepped up with 0.1 V increments in 250 minute time intervals.

9.2.2

and $V_{DGo}+V_T$ [6]. In our experiments we find that R_D degradation depends strongly on these biasing parameters (Figs. 3 and 4).

As further unmistakable evidence of the connection between R_D degradation and impact ionization, the degradation rate of R_D was observed to exhibit a classic exponential dependence on $1/(V_{DGo}+V_T)$, characteristic of impact-ionization (Fig. 5) [6].

Other device figures of merit associated with the drain side of the device were also found to degrade during electrical stressing. In particular, we observed a significant increase in the off-state breakdown voltage of the device, BV_{DGoff}, that was directly correlated to that of R_D (Fig. 6). The only common parameter of these two figures of merit is n_s, the sheet carrier concentration [7]. Hence our experiments suggest that n_s at the drain side is decreasing during degradation. Furthermore, C_{dg} was found to drop as R_D degrades (Fig. 7). This suggests that the semiconductor
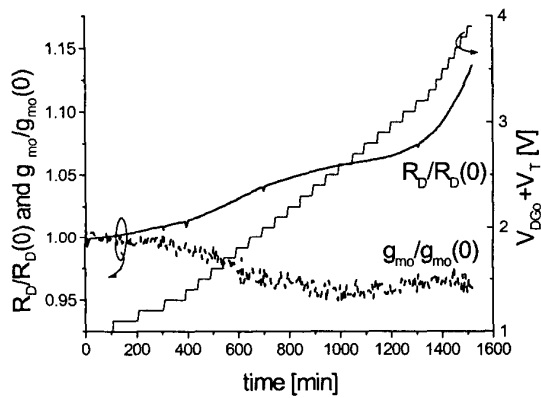
surface near the gate edge is affected in a severe way.

In order to increase the productivity of the electrical stress experiments, we developed a step stress scheme in which the degradation voltage was increased at regular intervals (Figs. 7 and 8). This approach revealed that there are two different degradation mechanisms at play (Fig. 8). For low voltages, when $V_{DGo}+V_T$ is below 2.6 V, there is a soft degradation in R_D that tends to saturate. At high voltages, a second, sudden and very rapid degradation of R_D is observed.

B. TLMs

In order to understand the physical origin of R_D degradation, we studied simpler TLM structures that have the same device layer structure as the HEMTs, but in which the cap has not been recessed. These measurements were performed at a lower temperature, as the lower amount of impact-ionization, enables a more precise measurement of the TLM saturation current, I_{sat}, without degrading the device.

Bias stress in the TLMs caused both the low-voltage resistance, R, (Fig. 9) and the saturation current, I_{sat}, (Fig. 10) to degrade. These measurements also revealed two different degradation mechanisms. At lower bias, when V_{stress} is below 4.5 V (for the 12 μm gap separation of Figs. 9 and 10), both R and I_{sat} degraded in a similar way over a similar voltage range. At high bias, only R degraded, while I_{sat} remained unaffected.

If we plot the onset voltages of these two degradation mechanisms as a function of the TLM length (Fig. 11), we find that there is a critical voltage for degradation, regardless of TLM length. When the impact of contact resistance is subtracted, this critical voltage is found to be about 1.1 V. This value is close to the impact ionization threshold for InGaAs [8].

Fig. 8: Time evolution of R_D and g_{mo} during a step stress experiment on a MHEMT with a constant I_D=250 mA/mm during stress at room temperature.
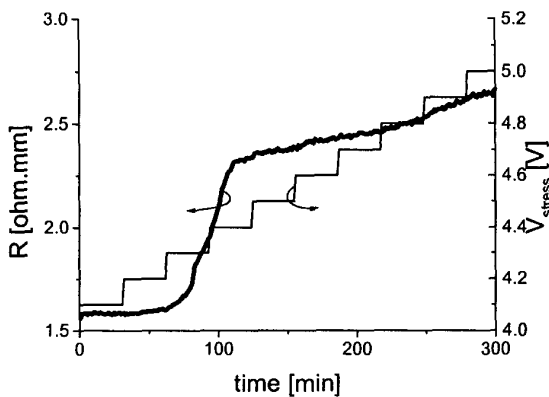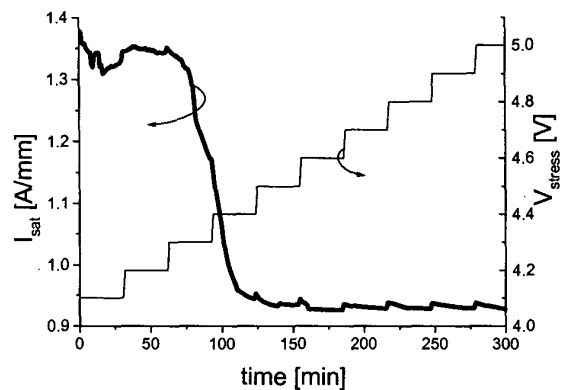

Fig. 9: Time evolution of low-field resistance, R, during step-stress of a 12 μm TLM at –65 °C. The voltage over the TLM (not excluding the drop over the probes) was stepped as a function of time.

Fig. 10: Time evolution of the saturation current, I_{sat}, during step-stress of a 12 μm TLM at –65 °C (same experiment as Fig. 9). The voltage over the TLM (not excluding the drop over the probes) was stepped as a function of time.

Discussion

All experimental results in this work are consistent with previous research in InP HEMTs [9]. Nothing in our experiments suggests that the metamorphic substrate might play a role in the degradation. There are two possible mechanisms behind the observed behavior: drain contact resistance (R_c) degradation and sheet resistance (n_s) degradation of the extrinsic drain region. We have separated these mechanisms by exploiting the linear dependence of I_{sat} on n_s in a TLM ($I_{sat}=qn_sv_{sat}$). In this way we can trace the evolution of $n_s/n_s(0)$ and $R_C/R_C(0)$, where $n_s(0)$ and $R_C(0)$ represent the values at t=0 [10].

For low voltages, we found that both n_s and R_C degrade. In fact we observe a "universal" relationship between the degradation of n_s and that of R_C for all gaps in a TLM (Fig.
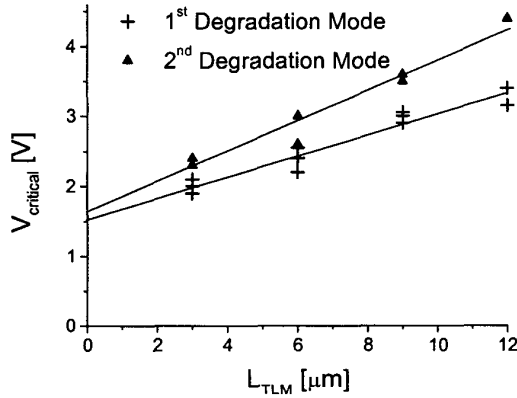

Fig. 11: Critical voltages for the first and second degradation modes, as a function of the channel length of the TLM, measured at room temperature.
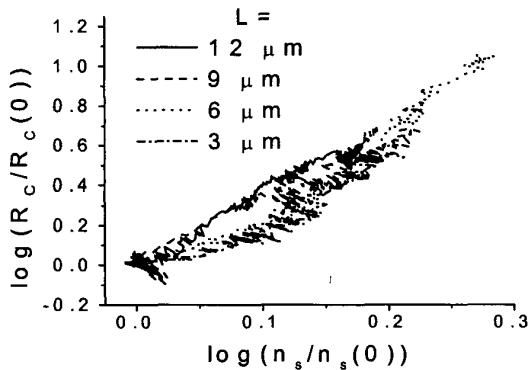

Fig. 12: $\log(R_C/R_C(0))$ vs. $\log(n_s/n_s(0))$ for different length TLMs, showing a universal dependence of R_C on n_s during degradation, measured at room temperature. The datapoints are at different times during degradation, for voltages lower than the critical voltage for the second degradation mechanism.

12). This suggests that R_C increases *because* n_s drops. This is consistent with ohmic contact theory [11]. At higher voltages, R_C increases while n_s does not change. This suggests that the second degradation mechanism affects the drain ohmic contact directly. Consistent with these observations, bias reversal after degradation did not produce significant new degradation at low voltages, while it produced further degradation at higher voltages.

The detailed physical mechanisms behind the degradation of n_s at low voltages and R_C at high voltages are not known. Several alternatives seem possible: hot-hole or hot-electron trapping at the surface [12], recombination-induced surface chemical reactions and a resulting surface potential modification, recombination-induced defect growth in the heterostructure, among others. It is significant that TLM degradation is observed even with the cap present. This suggests that an exposed InAlAs barrier layer near the gate is not essential for electrical degradation, as is commonly believed [9]. The correlation between C_{dg} and R_D degradation in the HEMT further suggests that degradation takes place above the channel if not at the surface itself and that the metamorphic buffer is not involved.

Conclusions

In conclusion, we have found that metamorphic InAlAs/InGaAs TLMs and HEMTs exhibit two different electrical degradation modes: one reduces the sheet carrier concentration on the drain side of the device, the second one degrades the drain ohmic contact. Both are directly related to impact-ionization. The metamorphic substrate does not seem to play a role in the degradation.

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