# Sub-40nm V-groove MOSFETs

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In past years opinions about the ultimate scaling limits of MOSFETs have often been revised, and experimentalists have proven that aggressive scaling results in high performance devices in the sub-50nm channel length regime.[1–5] The question of how far the reduction of MOSFET size can be driven - while obtaining improved device characteristics - remains open.

In a previous article,[6] we showed that a V-groove design can be used to achieve sub-0.1$\mu$m MOSFETs. A thick raised source/drain structure of highly n-doped silicon on top of an ultra-thin $p^-$ silicon channel (see Fig. 2) combines the advantages of low contact resistances with the suppression of short channel effects. Here, we present most recent results on V-groove MOSFETs with a source/drain separation down to $L_g$ = 36nm exhibiting state of the art electrical characteristics.[4,5] We therefore demonstrate that the V-groove MOSFET has potential for sub-40nm operation.

Using an anisotropic etch, V-grooves can be generated in silicon with the flanks of the groove defined by the {111} silicon planes. Combining this with an MBE grown, highly Sb-doped $n^{++}$ region ($\approx 10^{20}cm^{-3}$, grown at 600°C) on top of a 15nm lightly p-doped ($5 \times 10^{14}cm^{-3}$) channel layer (being part of an SOI structure), allows one to define source, drain and an ultra-short channel in a single step. Provided that the V-groove opening is chosen according to the doped silicon thickness, the V-groove can be engineered such that the n-doped layer is fully cut through - thus defining source and drain - while leaving the $p^-$ channel layer untouched. Since no annealing step is necessary for the definition of source and drain, an extremely abrupt doping profile results. Using an electron beam patterned etch mask as shown in Fig. 1, MOSFETs with nominal V-groove openings $L_0$ varying from 100nm to 160nm and a channel width of $W_0$ = 700nm have been fabricated. A typical cross section for the smallest V- groove opening is shown in Fig. 2. The channel length $L_g$ for this device is 36nm, much smaller than the actual lithographic pattern defining $L_0$. (Due to the processing details the final V-groove opening is approximately 40% larger than the nominal design.). After source/drain and channel definition a low-temperature gate oxide of $\approx$ 26Å was grown and a tungsten metal gate is defined.

Fig. 3 shows the output characteristic of a 36nm V-groove MOSFET (100nm V-groove opening). Figs. 4 and 5 illustrate the corresponding sub-threshold and transfer characteristics (straight black lines) as well as the characteristics for 110nm and 120nm V-groove openings. For our smallest devices we find a sub-threshold slope of 150mV/dec, $I_d$ = 415$\mu$A/$\mu$m and a specific transconductance value of around 1000$\mu$S/$\mu$m (both for $V_{gs}$ =$V_{ds}$ = 1V). From the output conductance data of Fig. 6, we calculate an intrinsic output resistance of only 500Ω-$\mu$m. In total, we characterized four transistors with sub-40nm gate length and similar electrical behavior. Comparing these results with recent publications[4,5], we find that our transconductance value for the same gate voltage over-drive is state of the art, in particular, taking into account that both, the gate oxide ($\approx$26Å) and the $p^-$ layer (15nm) are rather thick. The large channel layer thickness also is responsible for the slope of the sub-threshold swing. Reduction of $p^-$ thickness is expected to significantly improve the device performance in terms of DIBL.

Figs. 4 and 5 also contain our results on wider V-groove openings of 110nm (dotted black lines) and 120nm (straight gray lines) again for a nominal channel width of $W_0$ = 700nm. For V-groove openings beyond 120nm no transistor action was observed. This is the case since for large values of $L_0$ the channel layer gets fully consumed. Drain currents and transconductances ($G_m$) decrease very strongly with V-groove opening, as shown in Figs. 4 and 5, for openings of 100nm, 110nm and 120nm. Clearly part of this is caused by an increase in channel length, as supported by the improved sub-threshold characteristics shown in Fig. 4, but the increased opening also has an impact on the channel width. At larger $L_0$ the $p^-$ layer gets partly consumed by the etch due to non-uniformities, resulting in a decreased effective channel width. The critical dimensions of these devices will be determined, by destructive analysis, once all electrical measurements are done.

In conclusion, we have demonstrated that a V-groove MOSFET concept is capable of generating high performance transistor characteristics of sub-40nm MOSFETs.

[1] H. Kawaura et al. , Appl. Phys. Lett. **76**, 3810 (2000).

[2] G. Timp et al. , *International Electron Devices Meeting 1999*, Technical Digest, IEEE, 1999, page 55.

[3] K. Ishii et al. , Electronics Letters **34**, 2069 (1998).

[4] R. Chau et al. , *International Electron Devices Meeting 2000*, Technical Digest, IEEE, 2000, page 45.

[5] H. Wakabayashi et al. , *International Electron Devices Meeting 2000*, Technical Digest, IEEE, 2000, page 49.

[6] J. Appenzeller et al. , Appl. Phys. Lett. **77**, 298 (2000).

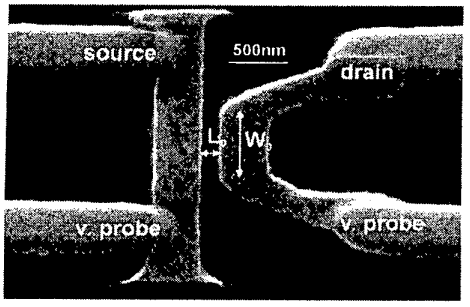


FIG. 1. SEM top view of a V-groove MOSFET before gate oxidation and gate metal deposition. $L_0$ is the V-groove opening, $W_0$ the nominal transistor width of around 700nm. Two source and two drain contacts are connected to allow to perform four-terminal measurements.

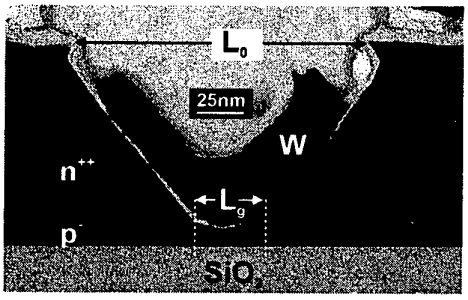


FIG. 2. TEM image of a 36nm MOSFET V-groove device. Tungsten (W) is used as a metal gate in our approach. Mention the flat bottom part of the V-groove allowing for optimum transport conditions in the channel of length $L_g$ in the $p^-$ region.

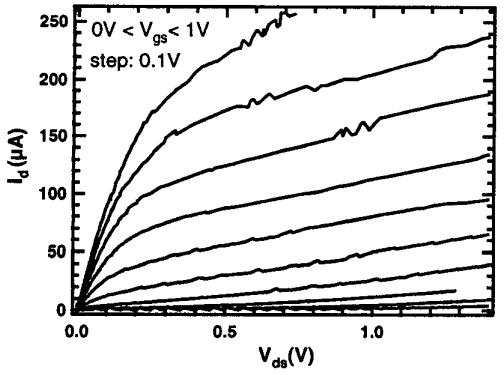


FIG. 3. Output characteristics of a 36nm ultra-short channel lengths MOSFETs (Corresponding to a nominal V-groove opening of 100nm.). The jogs in the output characteristics resulted from the interpolation of our four-point measurements.

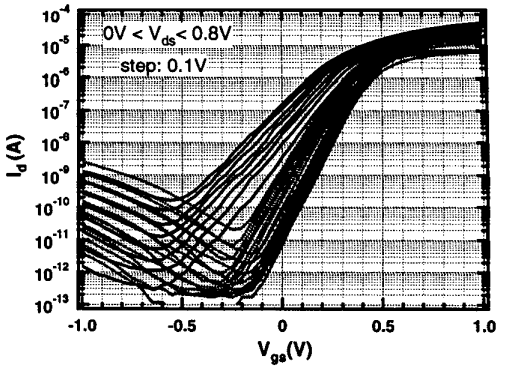


FIG. 4. Sub-threshold characteristics for V-groove openings of 100nm (straight black), 110nm (dotted black) and 120nm (straight gray).

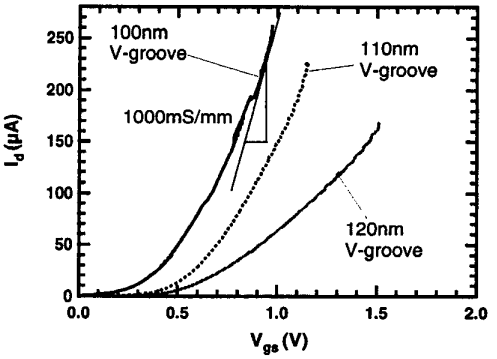


FIG. 5. Transfer characteristics of the three device classes under investigation. Line types as in Fig. 4. As in Fig. 3, the jogs result from the interpolation of our data.

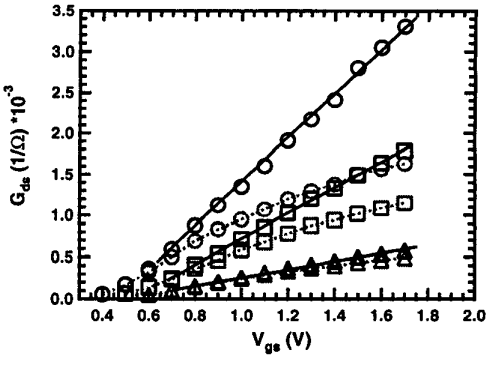


FIG. 6. Conductance in the linear output region for the three device classes under investigation (circles: 100nm, squares: 110nm, and triangles: 120nm nominal V-groove opening). The straight black lines are the result of subtracting a constant 310Ω spreading resistance due to the $n^{++}$ contact regions.