RF POWER PERFORMANCE OF LDMOSFETs ON SOI: AN EXPERIMENTAL COMPARISON WITH BULK Si LDMOSFETs

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ABSTRACT

We have simultaneously fabricated RF power LDMOSFETs on SOI and bulk-silicon wafers using an identical process. This paper directly compares their RF power performance at 1.9 GHz. We use this comparison to assess the suitability of SOI for RF power applications. The gain and linearity of the SOI LDMOSFETs match those of the bulk-silicon devices. The SOI devices exhibit substantially improved power efficiency, up to 8 percentage points. This improvement in PAE is shown to be related to reduced parasitic substrate loss in the SOI LDMOSFETs.

INTRODUCTION

Bulk-silicon RF power LDMOSFETs (Laterally Diffused MOSFETs) [1] have been very successful in RF power applications in wireless handsets. Recently, RF power LDMOSFETs have been implemented on SOI (Silicon-on-Insulator) [2,3,4]. In fact, a highly integrated 2-stage RF power amplifier has been fabricated on SOI, and its performance appears promising [5]. SOI has unique attributes for highly integrated wireless systems [6], and may enable the integration of the PA onto the same die with the other elements of the wireless system.

To date, there has been no direct assessment of the relative performance of SOI vs. bulk-silicon LDMOSFETs. Such a comparison would be very helpful in evaluating the usefulness of SOI in RF power applications. In this work, we have simultaneously fabricated RF power LDMOSFETs on SOI and bulk-silicon following an identical process. This paper compares the large-signal RF performance of the devices to evaluate the merit of SOI LDMOSFETs in RF power applications.

DEVICE DESIGN

The LDMOSFETs that were fabricated were designed for single-chip wireless applications. The process was constrained to permit its integration into a minimally modified CMOS process flow [2]. A cross section of the SOI and bulk LDMOSFETs that were fabricated is shown in fig. 1.

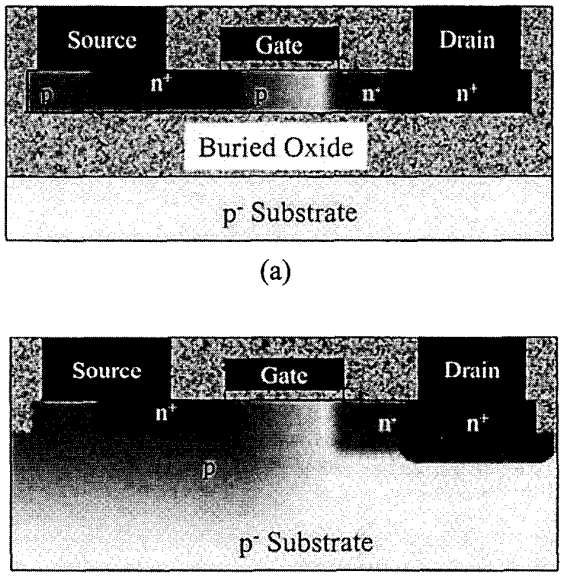

Figure 1 Cross-section of SOI (a) and bulk silicon (b) LDMOSFETs.

The SOI wafers that were used were full-dose SIMOX with a silicon thickness of 200 nm, and a buried oxide thickness of 400 nm. The wafers were all p-type with a resistivity of 10-20 Ohm-cm. The fabrication process is similar to a standard bulk-silicon LDMOSFET process [1]. A sinker implant is not useful on SOI and was not used. The body doping process and n^+ source implant were designed such that a body contact was created in the 200 nm silicon thickness under the source. LOCOS isolation was used. The n^+ polysilicon gate has a length of about 0.6 μm, and the gate oxide thickness is 30 nm.

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The bulk and SOI LDMOSFETs were processed simultaneously.

The results of the DC and S-parameter characterization were previously published in [2]. Only minor differences are found between the DC and small-signal RF characteristics of the SOI and bulk-silicon devices. All devices have an off-state breakdown voltage in excess of 20 V, a peak transconductance of 70 mS/mm, and an f_t of about 14 GHz.

RF POWER MEASUREMENTS

Load-pull measurements were performed at 1.9 GHz. A load-pull system from ATN Microwave Inc. was used. The devices that were measured had 20 fingers, each of which was 40 μm wide giving a total gate width of 800 μm. The source was conjugately matched while the load impedance was set for maximum power efficiency. A drain bias of 3.6 V was used, and the gate bias was set for Class A operation. Typical results are shown in fig. 2.

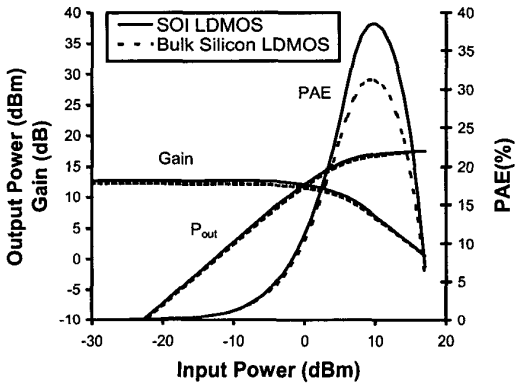

Figure 2 Large signal characteristics of the SOI and bulk silicon LDMOSFET at 1.9 GHZ. V_{dd} = 3.6 V.

As shown in fig. 2, the SOI device demonstrates a small signal gain of 12 dB, and a power added efficiency of up to 40%. The power density is about 80 mW/mm. The absolute performance of all of the devices is limited by the large resistance of the polysilicon gate. Hence, it is most useful to look at the comparison of the SOI and bulk-silicon devices rather than their absolute performance. The gain and power density of the SOI device is largely identical to that of the bulk-silicon LDMOSFET. The third-order intermodulation product of the devices was measured, and is displayed in fig. 3. The linearity of the SOI device is identical to the linearity of the bulk-silicon device. The power efficiency of the SOI device is significantly higher than the bulk device, by about 8 percentage points at the peak efficiency level.

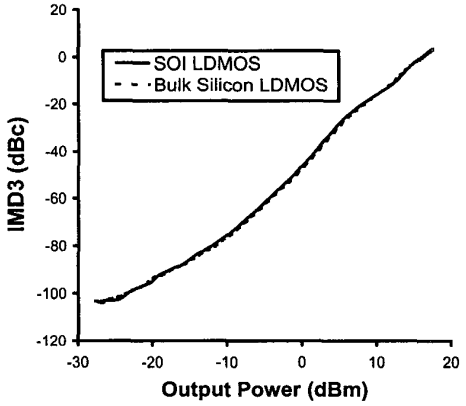

Figure 1 Intermodulation distortion of the SOI and bulk silicon LDMOSFETs at 1.9 GHz. V_{dd} = 3.6 V.

DISCUSSION

To understand the power efficiency advantage of SOI, we have studied the difference in the substrate parasitics between SOI and bulk-silicon devices. A picture of a device layout is shown in fig. 4 and the interconnect and pad metal are labeled. A simple model of the pads is also shown in fig. 4.

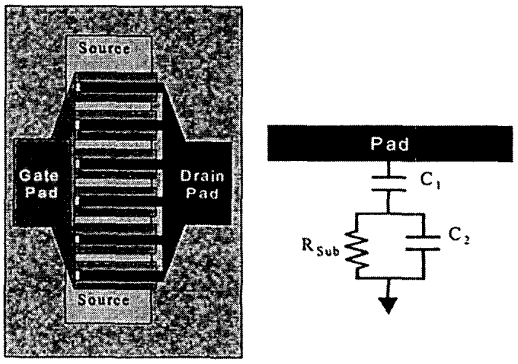

Figure 4 Device layout and a simple equivalent circuit model for the pad.

There is a significant difference in the layers that underlie the pad metal on SOI and bulk-silicon, as is depicted in fig 5. In the bulk-silicon device, LTO and LOCOS lie between the pad metalization and the substrate. At the surface of the substrate, the p-type field implant raises the doping level to prevent inversion of the field. In SOI, the buried oxide provides dielectric isolation and the implant is not required. The substrate doping level in the SOI devices remains low, and the substrate is partially depleted by the pad metalization. On SOI, the increased oxide thickness and the lack of a field implant significantly reduces the capacitance of the pads compared to bulk-silicon.

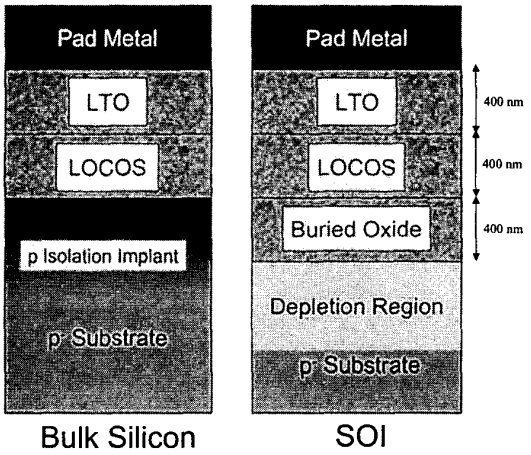

Figure 5 Cross-section beneath the pads of bulk and SOI LDMOSFETs.

The S-parameters of the bulk and SOI drain pads were measured, and are shown in fig. 6. The pads were modeled using lumped circuit as shown in fig. 4, and this model is also included in fig. 6. Values of the circuit elements for the pads on bulk and SOI are shown at the end of this paper in table 1. There are two primary differences between SOI and bulk. On SOI, the capacitor C1 and C2 are lower, and the substrate resistance R_{sub} is higher. These differences are directly related to the isolation implant, which increases capacitive coupling to the substrate and reduces the substrate spreading resistance. The lossiness of the pads is directly related to their overall conductance, which is plotted in fig. 7. At 1.9 GHz, the conductance of the pads is substantially higher on bulk-silicon than on SOI.

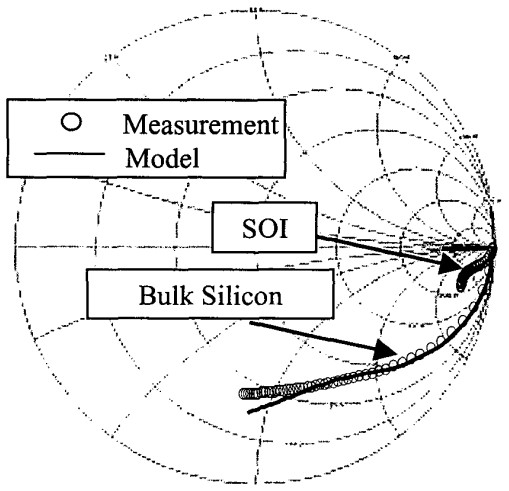

Figure 6 S-parameters of drain pads on SOI and bulk silicon. Freq. = 10 MHz to 6 GHz.

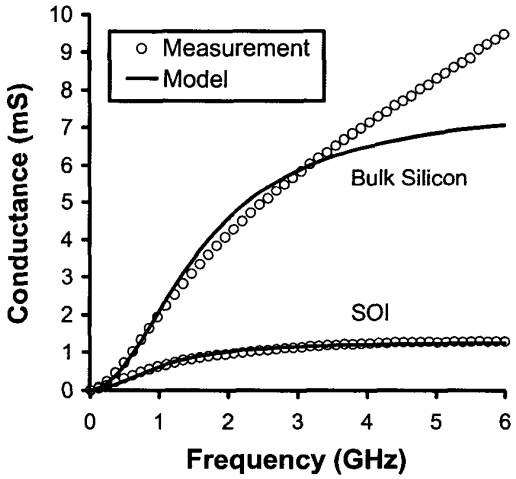

Figure 7 Conductance of pads on SOI and bulk silicon.

The increased conductance of the pads on bulk-silicon results in substantially increased power loss, and significantly reduced efficiency. Losses from the gate and drain metal were de-embedded from the load-pull measurements, and the results are shown in fig. 8. The intrinsic performance of a de-embedded SOI LDMOSFET is similar to the performance of

the bulk-silicon LDMOSFET. After de-embedding, the SOI device has 15 dB of small signal gain and peak efficiency of 52%, which nearly matches the bulk-silicon LDMOSFET. The pad parasitic losses on SOI are considerably reduced in comparison to bulk-silicon. The pads reduce the efficiency of the SOI and bulk devices by 12% points and 20%, respectively. Implementation of the LDMOSFET on SOI reduces parasitic loss and improves its efficiency.

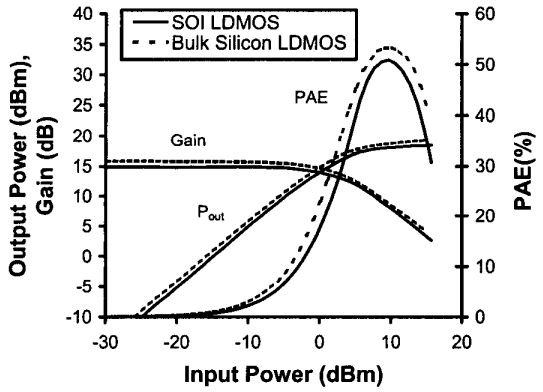

Figure 8 RF power measurements of LDMOSFETs at 1.9 GHz with the parasitics de-embedded. V_{dd}=3.6 V.

CONCLUSION

The RF power performance of an LDMOSFET fabricated on SOI was demonstrated and directly compared to the performance of an identically fabricated bulk-silicon device. This comparison shows that the intrinsic performance of SOI and bulk LDMOSFETs is very similar. It also shows that the substrate losses associated with the pad metalization and isolation implant are significantly reduced on SOI, and consequently the power efficiency of the SOI device is improved considerably. This work indicates that the RF power performance of an optimized SOI LDMOSFET can meet and may exceed the performance of a bulk-silicon LDMOSFET. SOI LDMOSFETs are promising devices for the highly-integrated RF PA applications of the future.

ACKNOWLEDGEMENTS

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	Bulk Silicon	*SOI*
C_1	1.2 pF	0.24 pF
R_{Sub}	50 Ω	516 Ω
C_2	0.750 pF	0.055 pF

Table 1 Pad model parameters on bulk-silicon and SOI.