A High Aspect-Ratio Silicon Substrate-Via Technology and Applications: Through-Wafer Interconnects for Power and Ground and Faraday Cages for SOC Isolation

Joyce H. Wu, Jesús A. del Alamo, and Keith A. Jenkins[1]

Massachusetts Institute of Technology, Cambridge, MA, U.S.A.
[1] IBM T. J. Watson Research Center, Yorktown Heights, NY, U.S.A.

Abstract

The reduction of ground inductance is crucial to the gain of RF and microwave circuits. To provide a low-inductance interconnect, we have developed a through-wafer via technology in silicon that incorporates a silicon nitride barrier liner and is filled with electroplated Cu. We have demonstrated vias with an aspect ratio as high as 14 and an inductance that approaches the theoretically expected value. Using the same technology, we have implemented a novel Faraday cage scheme for on-chip subsystem isolation that is successful in suppressing crosstalk by over 20 dB at 1 GHz at a distance of 100 μm.

Introduction

Substrate vias are widely used in GaAs microwave and millimeter-wave ICs to provide low-impedance ground connections [1, 2]. In many RF applications, silicon is starting to replace GaAs due to its lower costs and its logic integration capabilities. As silicon RFICs strive for high-performance, high-frequency operation, it becomes increasingly important to reduce all extrinsic parasitics. Of particular concern are the source impedance of MOSFETs and the emitter impedance of BJTs, which greatly affect the gain of RF amplifiers [3, 4]. To address this, we have developed a through-wafer via technology for silicon, which allows the implementation of high-aspect ratio, low-impedance ground connections. Since these vias incorporate an insulating liner, this through-wafer via technology could also be used to distribute power and ground in logic circuits and MEMS. This technology uses the same anisotropic plasma etch as previous Si via technologies, which have reached aspect ratios of 2.5 [5] and 17 [6], but their vias have only a thin coating of metal inside the via instead of being filled.

Our via technology can also be exploited to reduce crosstalk in RF circuits and improve subsystem isolation in RF System-on-a-Chip applications. High crosstalk immunity is critical to enable one-chip systems integrating noisy logic with sensitive low-noise amplifier and analog circuitry. Previous work has used buried oxide or doped silicon to isolate circuits [7-11]. In this paper we demonstrate a novel method of isolation that exploits our substrate-via technology. Our approach consists of surrounding noisy or sensitive circuits with a grounded Faraday cage of Cu vias.

Substrate-Via Technology

The substrate-via fabrication process was developed at the Microsystems Technology Laboratories at MIT. An illustration of our via concept is depicted in Fig. 1. Substrate thicknesses ranged from 100 to 170 μm. The process has three main steps: (1) via etch from the front of the wafer using an anisotropic deep reactive-ion etcher (DRIE) in a time-multiplexed inductively-coupled plasma, (2) deposition of conformal silicon nitride liner from the front and back of the wafer by PECVD, and (3) via filling with electroplated Cu.

For cross-section imaging of the technology, trenches were fabricated. Trench aspect ratios as high as 49 have been achieved in DRIE with nearly vertical sidewalls. There is a small aspect-ratio dependence on the etch rate [12]. For aspect ratios as high as 20, the decrease in etch rate was less than 15%.

The liner was made of silicon nitride because it electrically insulates the via from the substrate and is known to prevent Cu diffusion into silicon [13-15]. In our current approach, conformality of the nitride is limited to aspect ratios of 15 in trenches (Fig. 2).

Copper was electroplated using a pulse-reverse current source. A Ta-Ti-Cu electroplating seed layer was e-beam deposited on the backside of the wafer so that the via would fill from the bottom to the top. This method produced no

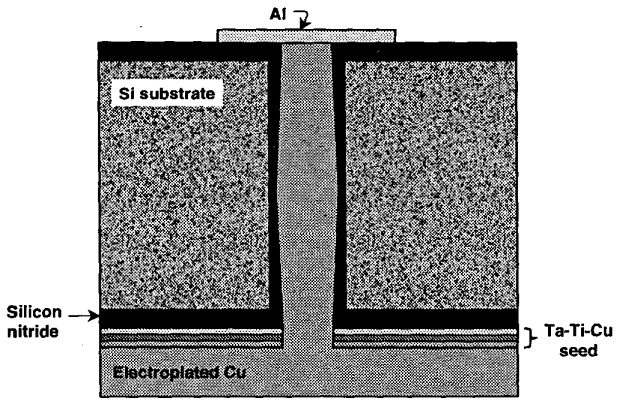

Fig. 1. Conceptual drawing of a substrate via conformally lined with silicon nitride and filled with Cu with an Al pad connected to the top of the via.

0-7803-6438-4/00/$10.00 ©2000 IEEE

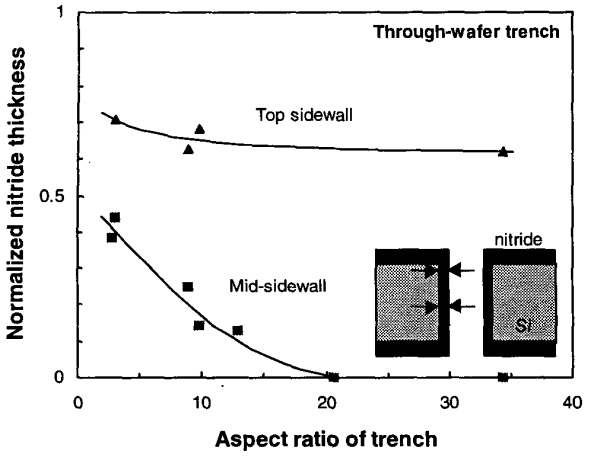

Fig. 2. Normalized PECVD Si_3N_4 liner thickness vs. aspect ratio of a trench. The liner thickness was normalized to the surface thickness. Mid-sidewall measurements were taken halfway down the trench and top sidewall measurements 1 μm down from the surface. The top sidewall thickness is relatively independent of aspect ratio. However, the mid-sidewall thickness decreases dramatically with aspect ratio. At an aspect ratio of about 15, the liner is non-conformal in the trench. Wafer thickness is 100 μm.

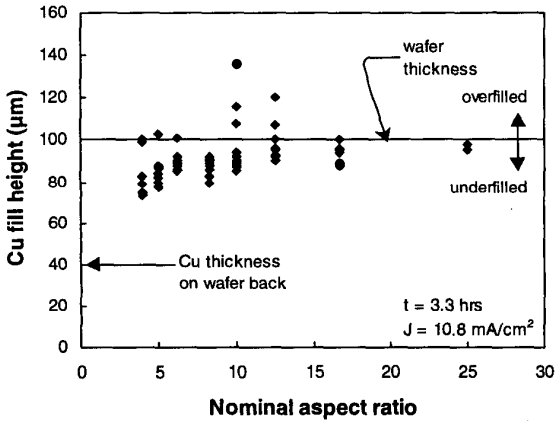

Fig. 3. Height of the Cu filled inside the via vs. nominal aspect ratio on a 100-μm thick wafer after 3.3 hours of electroplating at a current density of 10.8 mA/cm^2. Most vias on this wafer were underfilled, while a few were overfilled. The Cu thickness on the backside of the wafer was 40 μm, significantly less than inside the vias.

seams or voids in the via. However, the rate of filling has a slight inverse dependence on the opening width (Fig 3). We have succeeding in filling trenches with an aspect ratio of 49 and vias with an aspect ratio of 14.

An SEM cross-section of a finished via is shown in Fig. 4. Fig. 5 depicts detailed cross-sections of a trench and via to show the conformal silicon nitride liner between the Si substrate and the Cu via.

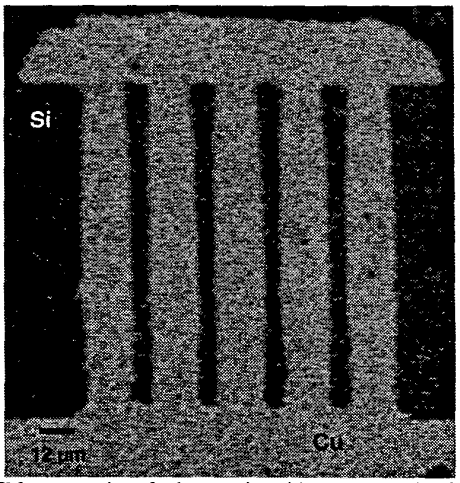

Fig. 4. SEM cross-section of substrate vias with an aspect ratio of 8. The substrate is 100-μm thick. Each via is 12-μm wide. These vias are overfilled.

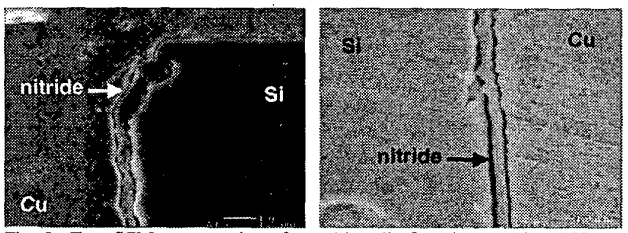

Fig. 5. Top: SEM cross-section of top-sidewall of a 14-μm wide x 103-μm deep via. The nitride liner is 550-nm thick at the surface and 500-nm thick 1 μm down from the surface. Bottom: cross-section of the mid-sidewall of a 38-μm wide x 106-μm deep trench. The nitride is 150-nm thick (260 nm at surface). Both are conformally lined with nitride and filled with Cu.

Via Impedance Measurements and Discussion

The microwave test structure for measuring the impedance of a single via is depicted in Fig. 6. This is a one-port test structure with a 50-Ω coplanar ground-signal-ground configuration. The via under test is on the signal line. The ground lines are shorted to the Cu ground plane through a large number of vias. Characterized vias ranged from 8 μm to 25 μm in nominal opening width. Wafer thickness is 170 μm. S_{11} was measured from 10 MHz to 6 GHz using a network analyzer and converted to Z_{11}. The series resistance and inductance of the test structure pads was not de-embedded, so the actual impedance of a via is lower than that measured.

For all vias, the real part of Z_{11} is largely independent of frequency, while the imaginary part is positive and increases linearly with frequency (Fig. 7). These results suggest a simple via model that consists of a resistor and an inductor in series. For vias with low-resistance, less than 1 Ω, the skin effect causes a noticeable dependence of via resistance and to a smaller extent of inductance on frequency (Fig. 8).

Fig. 9 shows the high-frequency (6 GHz) extracted inductance of several vias on a 170-μm thick substrate as a

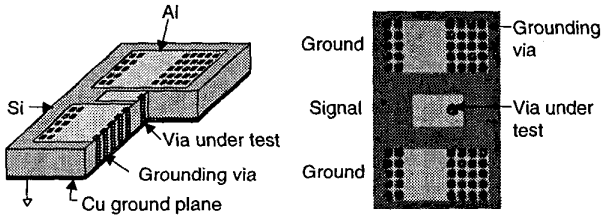

Fig. 6. *Left*: 3-D schematic of the test structure. The multiple grounding vias are introduced to reduce the impedance of the ground pads. *Right*: picture of the one-port test structure for measuring the impedance of a single via.

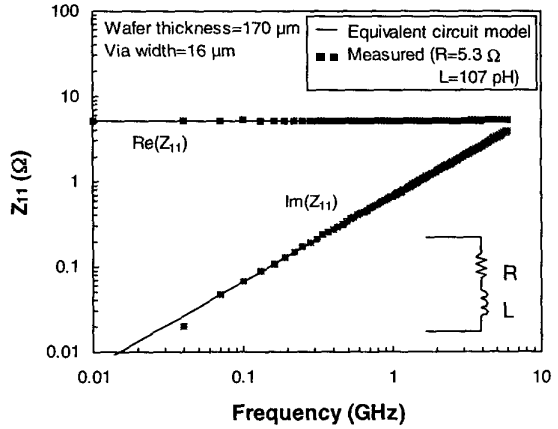

Fig. 7. Z_{11} vs. frequency of a one-port test structure with a via 16-μm wide and 170-μm deep. The real part of Z_{11} is independent of frequency, while the imaginary part has a linear dependence. This is the ideal behavior of a simple resistor and inductor in series.

function of the via aspect ratio. The scatter in the data is believed to result from slight underfilling or overfilling of some vias and the difficulty of the top pads in contacting them. Fig. 9 also includes a theoretical calculation of an inductance model by Golfarb and Pucel [16] for a substrate via. The lower lying experimental data points agree well with this theoretical model. This gives us confidence that without overfilling/underfilling, this technology can produce vias with theoretically minimum inductance.

Faraday Cage Characterization and Discussion

The high aspect ratio of our vias allows them to be packed in high density. We have exploited this to demonstrate a novel Faraday cage isolation scheme to suppress crosstalk in ICs. It consists of a simple ring of grounded vias that circle a noisy or sensitive subsystem in a chip. To test this concept, we have designed a two-port test structure with a Faraday cage surrounding a transmitter pad in a coplanar 50-Ω ground-signal-ground configuration. Isolation was measured by a receiver pad at varying distances (Fig. 10). An identical reference structure was fabricated without the Faraday cage. As the isolation figure of merit, the magnitude of S_{21} was measured up to 6 GHz. In the first implementation, the vias are 10-μm wide and are spaced 10 to 70 μm apart.

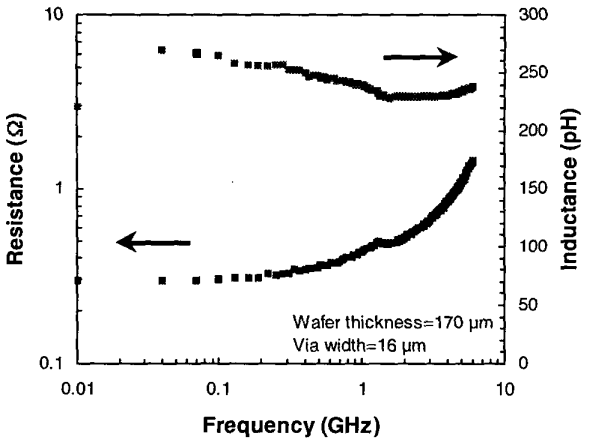

Fig. 8. Resistance and inductance vs. frequency for a via 16-μm wide and 170-μm deep. For vias with resistance less than 1 Ω, the skin effect is noticeable, producing a dependence of resistance and inductance on frequency.

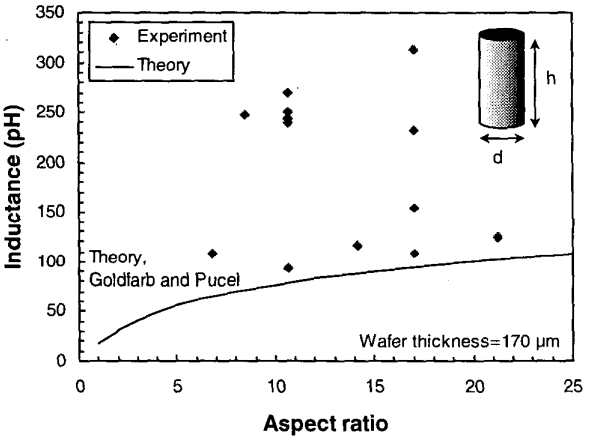

Fig. 9. Extracted inductance vs. nominal aspect ratio of vias on a substrate thickness of 170 μm. Plotted in a solid line is the theoretical inductance [16].

Compared to the reference structure, at a transmission distance of 100 μm, the Faraday cage with via separation of 10 μm improves isolation by 21 dB at 1 GHz and 15 dB at 6 GHz (Fig. 11). Over the entire frequency range, the signal measured with the probes in the air is similar to the caged-structure signal, indicating that the Faraday cage suppresses crosstalk down to the noise floor of our experimental technique. The crosstalk suppression improves as the distance from the transmission pad increases (Fig. 12). At 800 μm, cross-talk suppression reaches 25 dB at 1 GHz. In the range of via spacings that we have examined (10-70 μm), the via density of the cage does not affect the isolation effectiveness substantially (Fig. 13). These two results are consistent with an isolation effectiveness for the Faraday cage that exceeds the resolution of our experiments.

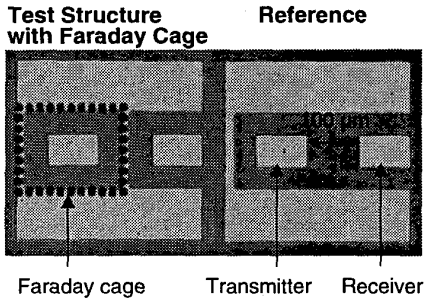

Fig. 10. Top view of the Faraday cage test structure at a transmitter-receiver separation or transmission distance of 100 µm. Each via of the cage is 10-µm wide and separated by 10 µm.

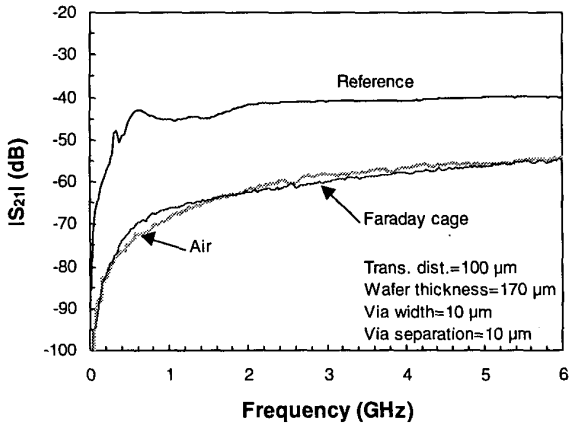

Fig. 11. Magnitude of S_{21} vs. frequency for a reference and caged structure at a transmission distance of 100 µm. The Faraday cage gives at least 15 dB of isolation improvement at 6 GHz and over 20 dB of improvement at 1 GHz. Measurement of the signal taken with the probes in air is similar to the caged-structure signal, indicating the Faraday cage suppresses substrate crosstalk down to the resolution limit of our experimental technique.

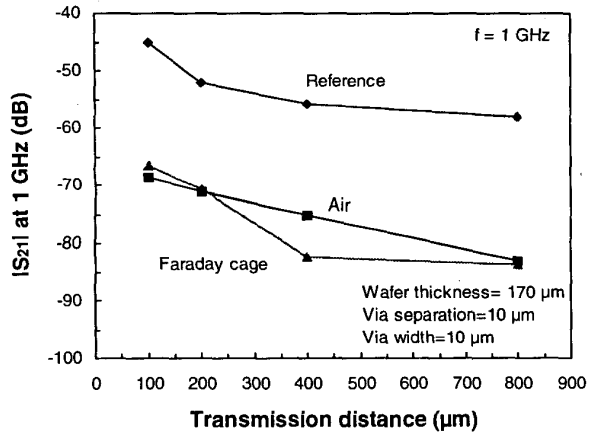

Fig. 12. Magnitude of S_{21} at 1 GHz vs. the transmission distance for a reference and caged structure. The effectiveness of the Faraday cage appears to increase with increasing transmission distance. Measurements with the probes in the air suggest that the Faraday cage effectiveness is higher than can be resolved.

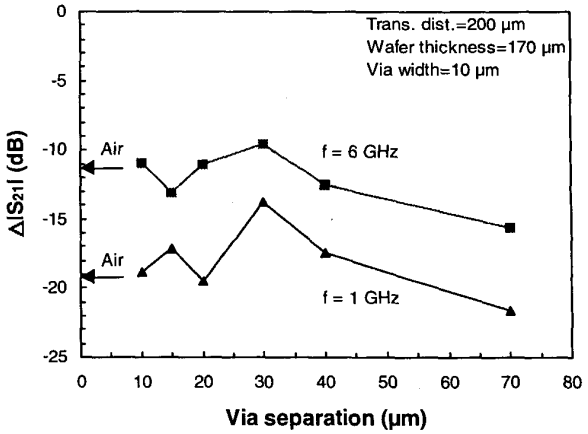

Fig. 13. Difference in the magnitude of S_{21} between the reference and caged structure vs. the separation between vias of the Faraday cage at 1 and 6 GHz. There is no apparent dependence on via separation for isolation effectiveness. This suggests that crosstalk suppression exceeds the air noise floor.

Conclusions

We have successfully developed a high-aspect ratio, insulated substrate-via technology for low-inductance power and ground distribution in ICs. Obtained inductance values approach theoretical expectations. We have also used this technology to demonstrate Faraday cages as a novel isolation scheme for SOC applications. The Faraday cage improves isolation by over 20 dB at 1 GHz at a distance of 100 µm.

Acknowledgements

We wish to thank J. G. Fiorenza, A. A. Ayón, J. Voldman, A. Fan, J. Scholvin, and the staff at the Microsystems Technology Laboratories at MIT for their stimulating discussions and fabrication expertise. We also thank D. A. Hitko for his assistance with the measurements. This work was funded by the Semiconductor Research Corporation.

References

[1] H. Furukawa et al., *IEEE GaAs Conf.*, 251, (1998).
[2] R. J. Shul et al., *Electrochem. Soc. Proc.*, 84, (1996).
[3] M. Fukuta et al., *IEEE Trans. Elect. Dev.*, **ED-23**, 388, (1976).
[4] L. A. D'Asaro et al., *IEEE Trans. Elect. Dev.*, **ED-25**, 1218, (1978).
[5] K. M. Strohm et al., *IEEE MTT-S Intl. Microwave Symp.*, 581, (1999).
[6] H. T. Soh et al., *Intl. Conf. on Sol. Stat. Dev. and Matls.*, 284, (1998).
[7] I. Rahim et al., *IEEE Intl. SOI Conf.*, 170, (1992).
[8] R. B. Merrill et al., *IEDM*, 433, (1994).
[9] A. Viviani et al., *IEDM*, 713, (1995).
[10] K. Joardar, *Electronics Lett.*, **31**, pp. 1230, (1995).
[11] J. Kodate et al., *Japan. J. of Appl. Phys. Part 1*, **39**, 2256, (2000).
[12] A. A. Ayón et al., *J. Electrochem. Soc.*, **146**, 339, (1999).
[13] G. M. Adema et al., *IEEE Trans. on Comp., Hybrids, and Manuf. Tech.*, **16**, 53, (1993).
[14] P.-L. Pai et al., *IEEE VLSI Multilevel Intercon. Conf.*, 258, (1989).
[15] J. Li et al., *IEEE VLSI Multilevel Intercon. Conf.*, 153, (1991).
[16] M. E. Goldfarb et al., *IEEE Micro. Guided Wave Lett.*, **1**, 135, (1991).