# On-State Breakdown in Power HEMT's: Measurements and Modeling

Mark H. Somerville, Roxann Blanchard, *Student Member, IEEE,*
Jesús A. del Alamo, *Senior Member, IEEE,* K. George Duh, and P. C. Chao

***Abstract*— We have carried out a systematic study of *on-state* breakdown in a sample set of InAlAs/InGaAs HEMT's using a new *gate current extraction* technique in conjunction with sidegate and temperature-dependent measurements. We find that as the device is turned on, the breakdown voltage limiting mechanism changes from a TFE-dominated process to a multiplication-dominated process. This physical understanding allows the creation of a phenomenological physical model for breakdown which agrees well with all our experimental results, and explains the relationship between $BV_{\rm on}$ and the sheet carrier concentration. Our results suggest that depending on device design, either on-state or off-state breakdown can limit maximum power.**

***Index Terms*— Breakdown, HEMT, impact ionization, MODFET.**

## I. Introduction

InAlAs/InGaAs and AlGaAs/InGaAs high electron mobility transistors (HEMT's) are enjoying significant success in microwave and millimeter-wave power applications [1]–[4]. Great strides have been made in improving off-state breakdown $(BV_{\rm off})$ in HEMT's through a variety of approaches, including the use of undoped or lightly-doped caps, high aluminum content insulators, composite channels, quantized channels, and novel gate recess schemes [5]–[8]. At the same time there has been significant work devoted to understanding the origins of $BV_{\rm off}$ [9]–[11], so that it is becoming feasible to engineer HEMT's with a given off-state breakdown voltage.

On the other hand, there has been relatively little work on the on-state breakdown voltage $(BV_{\rm on})$, even though $BV_{\rm on}$ is a parameter of primary importance for power devices [12]. This has been largely due to difficulties in measuring $BV_{\rm on}$ in a safe, reproducible manner. Typically on-state breakdown is thought of as a significant upturn in the drain current. Dickmann *et al.* have used this definition to explore $BV_{\rm on}$ in InAlAs/InGaAs HEMT's with different channel compositions [13]. While such a definition is intuitively attractive, it is difficult to implement in a reliable way, because observing the rise in $I_D$ requires biasing the device in a region of significant carrier multiplication. Furthermore, this definition is rather ambiguous due to the significant output conductance and kink effect [14] often present in short gate length HEMT's. An alternative approach is to use a burnout criterion, as suggested by Rohdin [12]. For this measurement, the device is biased at a given gate voltage, and the drain voltage is increased until the device is destroyed. While such a definition is precise, it is also undesirably destructive. Finally, Meneghesso has examined the dependence of on-state gate current on temperature and heterostructure design [8]. This work provides insight into the physics of $I_G$, but does not investigate or define $BV_{\rm on}$.

We have recently proposed a simple, unambiguous, and reproducible *gate current extraction* measurement for $BV_{\rm on}$ [15]. In this work, we use this method in conjunction with statistical burnout measurements as well as detailed temperature-dependent measurements and sidegate measurements to investigate the physics of both off-state and on-state breakdown. Our experiments illuminate the roles of impact ionization and tunneling plus thermionic field emission (TFE) in $BV_{\rm on}$, $BV_{\rm off}$, and device burnout. These insights allow us to develop a simple physical model for $BV_{\rm on}$ which explains our experimental results. We find that depending on device design, either $BV_{\rm off}$ or $BV_{\rm on}$ can limit the maximum power density of a HEMT.

## II. The Gate Current Extraction Technique

This new technique to measure $BV_{\rm on}$ is described in [15], [16] sketched in the inset of Fig. 1. In essence, $I_G$ is held constant at a desired value (a typical condition is $-1$ mA/mm), and $I_D$ is ramped from $|I_G|$ to some reasonable value (typically 20–40% of $I_{D\max}$). This measurement traces a locus of $V_{DS}$ versus $I_D$ for constant $I_G$; we define this locus as $BV_{\rm on}$. Fig. 1 illustrates the technique on a state-of-the-art 0.1-$\mu$m InAlAs/$In_{0.67}Ga_{0.33}As$ HEMT [9]. $BV_{\rm on}$ loci for several values of $I_G$ are superimposed on the device's output characteristics. In this case, as the device is turned on, $BV_{\rm on}$ at $|I_G| = 1$ mA/mm first drops from 4.2 V $(BV_{\rm off})$ to less than 2.5 V, and then saturates. Similar behavior is observed for other values of gate current.

Two advantages of the definition and technique are evident in Fig. 1. First, the definition is sensible and consistent in that $BV_{\rm on}$ converges to $BV_{\rm off}$ as the device is turned off. In addition, sampling the gate current is an excellent way to predict the region of rising output conductance (typically associated with device degradation and burnout) without actually operating the device in that regime [15].

Manuscript received June 25, 1998; revised January 20, 1999. The review of this paper was arranged by Editor A. S. Brown. This work was supported in part by Lockheed-Martin, MAFET, JSEP (DAAH04-95-1-0038), and a JSEP Fellowship.

M. H. Somerville, R. Blanchard, and J. A. del Alamo are with the Massachusetts Institute of Technology, Cambridge, MA 02139 USA.

K. G. Duh and P. C. Chao are with Sanders, Nashua, NH 03061-0868 USA.

Publisher Item Identifier S 0018-9383(99)04586-4.

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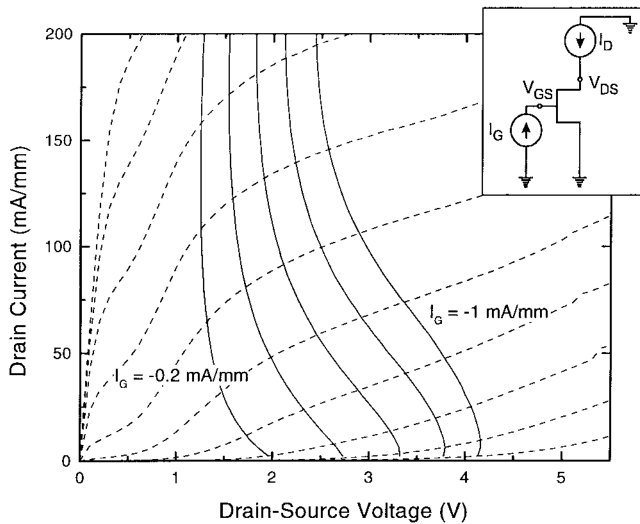



Fig. 1. $BV_{\rm on}$ versus $I_D$ for 0.1 $\mu$m InAlAs/InGaAs HEMT for different values of $I_G$. The data are superimposed on the output characteristics. The constant $I_G$ criteria additionally tracks the sudden rise of drain conductance often associated with $BV_{\rm on}$. The inset shows the *gate current extraction technique* used to measure $BV_{\rm on}$. A constant current (typically 1 mA/mm) is extracted from the gate while $I_D$ is swept from the off-state (1 mA/mm) to the on state.

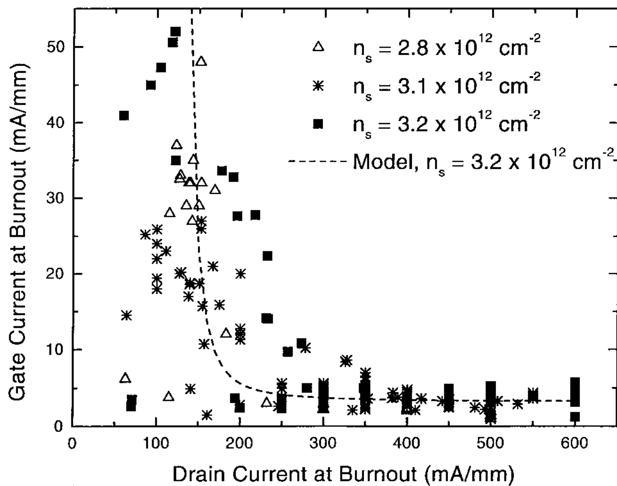



Fig. 2. Measured gate current at burnout as a function of drain current for several different 0.1-$\mu$m InAlAs/InGaAs HEMT's. For all three wafers, burnout in the on-state occurs at around $I_G = 2.5 \pm 1$ mA/mm regardless of $I_D$, so long as $I_D$ is above 200 mA/mm. At lower values of $I_D$, burnout occurs at much higher values of $I_G$. Also shown is the modeled gate current for one of the devices obtained by varying $I_D$ while holding the impact ionization component of $I_G$ constant.

Such an interpretation is supported by statistical burnout measurements on several wafers. In order to measure burnout we inject a given current into the drain, and gradually increase the gate current until the device fails. As confirmation we have also performed voltage-driven burnout measurements, where $V_{GS}$ is held constant, and $V_{DS}$ is increased until the device fails. Both approaches yield similar results, shown in Fig. 2. Here we plot the measured gate current at burnout versus drain current at burnout for three wafers with different sheet carrier concentrations. In the high current regime ($I_D > 200$ mA/mm), burnout occurs at an approximately constant gate current ($|I_G| = 3\pm1$ mA/mm) on all three wafers *regardless of* $I_D$. This suggests that in this regime, the burnout is associated with the total multiplication current, which should be mapped by $I_G$ once the device is turned on hard [8], [16], and not with the drain current. This is consistent with previously reported burnout results [12]. However, at lower values of $I_D$, burnout occurs at *significantly* higher values of $I_G$. Such a result suggest either that the burnout mechanism is changing, or that the origin of the gate current is changing, as we discuss below.

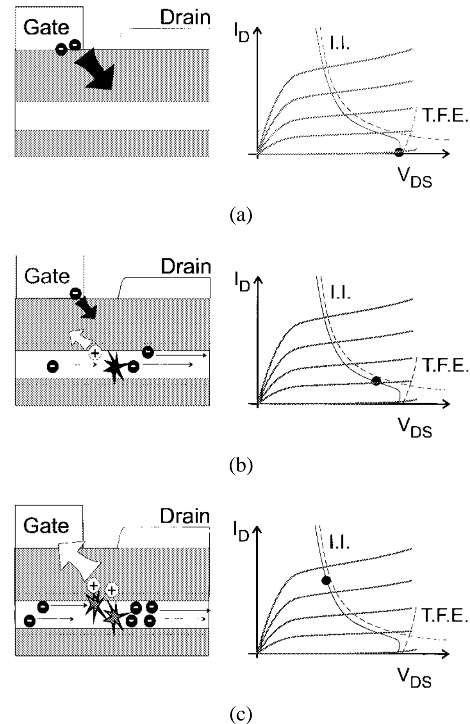



Fig. 3. Physical mechanisms for breakdown. (a) Close to threshold, $I_G$ is almost purely tunneling and thermionic field emission. (b) As the device is turned, impact ionization in the channel produces holes, which escape to the gate. (c) In order to support a constant $I_G$, $V_{DG}$, and $V_{DS}$ must drop.

## III. On-State Breakdown Physics

We have previously suggested that in the off-state, tunneling and TFE dominate the reverse gate current [9], [11]. Furthermore, it is widely agreed that in the on-state, reverse gate current arises as a result of impact ionization [8], [18]. Combining these two observations creates a simple picture of the physics of $BV_{\rm on}$ which is consistent with the measurements above and with previous results (Fig. 3). When the device is biased in the off-state at $BV_{\rm off}$, $I_G$ is almost purely TFE [Fig. 3(a)]. However, as the device is turned on, electrons flow through the high-field gate-drain region, where they undergo impact ionization. This produces holes, some of which escape to the gate. In order to maintain constant $I_G$, $V_{DG}$ must drop, and so must $V_{DS}$. Thus when the device is just above threshold, both impact ionization and TFE contribute to the gate current [Fig. 3(b)]. Finally, once the device is fully on, impact ionization dominates [Fig. 3(c)]. In this regime, $BV_{\rm on}$ becomes quite vertical, due to the exponential dependence of impact ionization on field. Such a picture should apply to most power HEMT structures, although the transition from

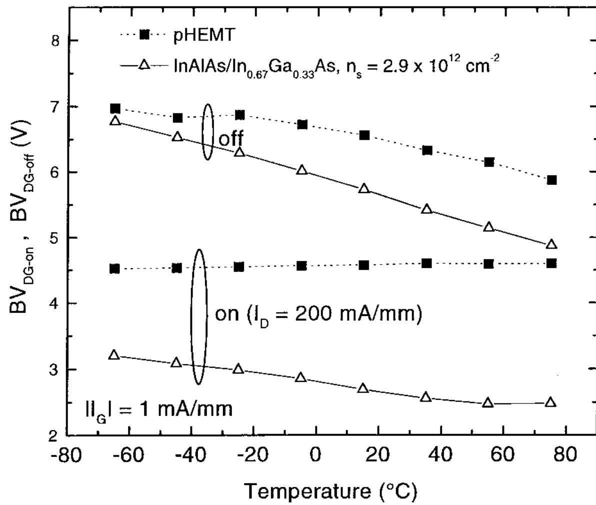



Fig. 4. Temperature dependence of $BV_{\rm off}$ ($|I_G| = I_D = 1$ mA/mm) and $BV_{\rm on}$ ($I_D = 200$ mA/mm, $|I_G| = 1$ mA/mm) in an AlGaAs/InGaAs PHEMT and a strained channel InAlAs/InGaAs HEMT.

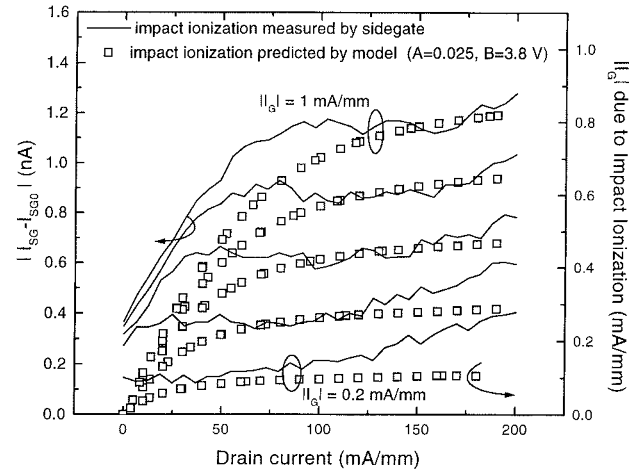



Fig. 5. Sidegate current measured during on-state breakdown measurement of 0.1-$\mu$um InAlAs/$In_{0.67}Ga_{0.33}As$ HEMT ($V_{SG} = -50$ V). The rise and saturation of $I_{SG}$ demonstrate the transition from the TFE dominated off-state to the impact ionization dominated on-state. Also plotted are the simple model's predictions for impact ionization current.

TFE dominated to multiplication dominated gate current will likely occur at different values of $I_D$.

In order to explore these physics, we have performed temperature dependent measurements of $BV_{\rm on}$ and $BV_{\rm off}$ for several different HEMT designs, including a high-performance 0.1-$\mu$m AlGaAs/$In_{0.22}Ga_{0.78}As$ PHEMT [17], a 0.1 $\mu$m InAlAs/$In_{0.67}Ga_{0.33}As$ HEMT's [9], and a lattice-matched 1-$\mu$m InAlAs/InGaAs HEMT fabricated at MIT [15]. Fig. 4 compares the results for the PHEMT and the InAlAs/$In_{0.67}Ga_{0.33}As$ HEMT. Here $BV_{\rm off}$ is defined at $|I_G| = I_D = 1$ mA/mm, and $BV_{\rm on}$ is tracked at $|I_G| = 1$ mA/mm, $I_D = 200$ mA/mm. Similar results are found for other choices of $I_D$ above 100 mA/mm.

Examining first the results on the PHEMT, we observe that $BV_{\rm off}$ exhibits a negative temperature coefficient, dropping from 7 V at $-65$ °C to less than 6 V at $+75$ °C. This negative temperature dependence is consistent with a tunneling/TFE mechanism. However, $BV_{\rm on}$ in the PHEMT exhibits a small but significant (50 mV) *rise* as temperature is increased. The transition from a negative to a positive temperature coefficient is a clear signature of a transition from TFE to impact ionization.

In contrast, the temperature dependences of both $BV_{\rm on}$ and $BV_{\rm off}$ for the InAlAs/$In_{0.67}Ga_{0.33}As$ HEMT are negative. Similar results are observed on the lattice matched device (not shown). These results are consistent with the recent demonstration of a negative temperature coefficient for impact ionization in InGaAs with higher indium concentrations [8]. Unfortunately, the identical signs of the TFE mechanism and the impact ionization mechanism make isolation of the physics more challenging.

In order to distinguish TFE from impact ionization in the InAlAs/InGaAs HEMT's, we have directly monitored hole generation through a negatively biased sidegate [18] or through a fourth probe on the substrate next to the active device [10]. The sidegate extracts a small portion of the generated holes without disrupting device behavior; thus by measuring sidegate current while the locus of $BV_{\rm on}$ is being traced, we can obtain a picture of the relative contribution of impact ionization to the gate current.

The results of this measurement on the InAlAs/$In_{0.67}Ga_{0.33}As$ HEMT are presented in Fig. 5 as a function of $I_G$ and $I_D$. These measurements were taken while the $BV_{\rm on}$ loci were being traced. When the device is off ($I_D$ small), the sidegate current is minimal and relatively independent of $I_G$, indicating that in the off-state TFE dominates breakdown. Note that there is some increase in $I_{SG}$ with increasing $I_G$; this has been observed in other devices, and is probably due to the combination TFE-impact ionization mechanism that has been previously suggested [10]. The fact that this increase in $I_{SG}$ is so small suggests that this mechanism plays a secondary role in $BV_{\rm off}$.

As the device is turned on, the sidegate current rises significantly. This is a signature of increasing impact ionization in the channel. However, since the gate current is held constant, impact ionization can only increase until $I_G$ is completely dominated by hole current. This occurs for $I_D \approx 80$ mA/mm, where we observe that the sidegate current saturates. Naturally, the saturated sidegate current scales with $I_G$. These observations indicate that 1) for high values of $I_D$, a constant $I_G$ criteria corresponds to constant impact ionization, and 2) the gate's hole collection efficiency does not depend much on $I_G$ or $I_D$. Indeed, the proportionality of $I_G$ and $|I_{SG} - I_{SG0}|$ strongly reinforces the link between gate current and impact ionization [8]. Measurements of the lattice-matched device yield similar results; however, saturation only begins to occur around $I_D = 200$ mA/mm, suggesting that due to the long gate length and less aggressive design of this device, impact ionization plays a less important role in $BV_{\rm on}$, and therefore TFE is important up to relatively higher values of $I_D$.

This picture of $BV_{\rm on}$ is also consistent with our observations of burnout and the hypothesis that burnout is strongly related to impact ionization [12]. When the device is fully on, $I_G$ is almost purely due to impact ionization, so a burnout

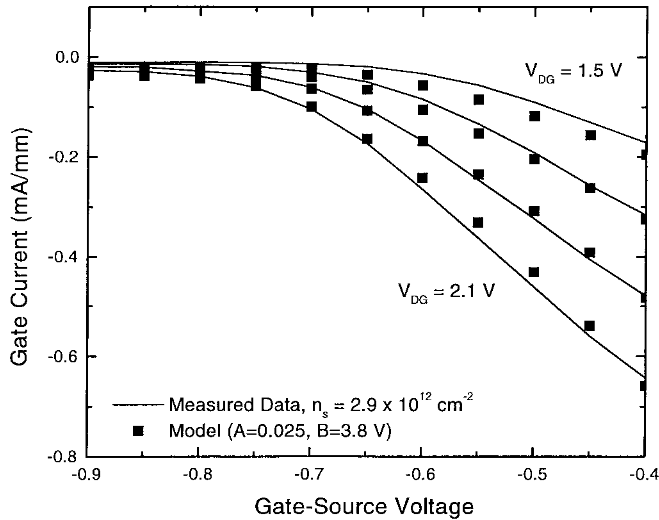



Fig. 6. Comparison of measured and modeled gate current characteristics for 0.1-$\mu$m InAlAs/InGaAs HEMT.

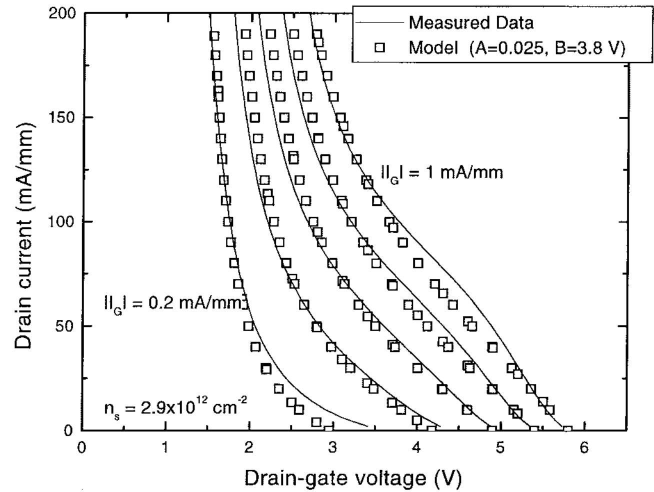



Fig. 7. Comparison of measured and modeled breakdown contours for 0.1-$\mu$m InAlAs/InGaAs HEMT for different $I_G$ criteria.

mechanism due to impact ionization should occur at a constant gate current. On the other hand, when the device is near threshold, $I_G$ consists primarily of thermionically emitted electrons. In this case, burnout will not occur until $I_G$ is increased to a much higher level, since the impact ionization component of $I_G$ is small. This is what is observed in the results of Fig. 2.

## IV. On-State BV Model

Our simple picture of $BV_{\rm on}$ leads to a phenomenological model that can assist device and circuit designers. For a given bias condition, $I_G$ is determined by the fraction of the holes generated by impact ionization that are extracted by the gate, and by the number of electrons which escape from the gate due to TFE and tunneling

$$I_G = I_{\rm TFE} + I_{ii}. \tag{1}$$

We have previously shown that TFE depends mainly on the extrinsic sheet carrier concentration, the gate Schottky barrier height, and $V_{DG}$ [9], [11]. Proper calculation of the impact ionization current requires precise knowledge of the fields in the channel and of the ionization rate. It is possible, however, to simplify the problem using the experimentally verified expression [18]

$$I_{ii} = AI_D \exp\left(\frac{-B}{V_{DG} - V_T}\right). \tag{2}$$

$B$ can be determined from sidegate measurements; $A$ is a scaling constant that depends on device design. While this expression is a phenomenological one, it does capture the key physics of impact ionization: carrier multiplication depends linearly on the electron flux (i.e., $I_D$), and has an exponential dependence on the field in the drain-gate gap.

Fig. 6 shows the modeled and measured gate current characteristics for several values of $V_{DG}$ for the 0.1-$\mu$m InAlAs/$In_{0.67}Ga_{0.33}As$ HEMT considered above. The agreement is very good. Note that the bell shape typically seen in gate current characteristics is not present because in this chart $V_{DG}$ is being held constant. Thus, as the device is turned on, the gate current is nominally linear in $I_D$. It is also clear that in this regime, TFE is not making a significant contribution to $I_G$, as $I_G$ is small in the off-state.

A comparison between the modeled and measured $BV_{\rm on}$ loci is plotted in Fig. 7. Using the same fitting parameters as used to model the gate current at lower values of $V_{DG}$, the model accurately captures both the initial drop in $BV_{\rm on}$ and the more vertical behavior of $BV_{\rm on}$ at higher values of $I_D$. The model works well for the full range of $I_G$ values considered.

The results in Fig. 7 are more impressive when considered in conjunction with the sidegate measurement of impact ionization and the model's predictions of impact ionization. Fig. 5 plots the amount of impact ionization current in $I_G$ predicted by the model for the simulated $BV_{\rm on}$ loci in Fig. 7. As can be seen, the model predicts exactly the same initial rise and subsequent saturation of impact ionization that is seen in the sidegate measurements. In other words, the model not only fits the actual $BV_{\rm on}$ loci, but also correctly models the relative proportion of impact ionization in $I_G$ for different values of $I_G$ and $I_D$.

Finally, the model helps us to understand the burnout results shown in Fig. 2. Here we have used the model to predict the total gate current for one of the devices as a function of $I_D$ under the condition that the impact ionization current is constant at 3 mA/mm, which should be a reasonable predictor for burnout [12]. Similar results are obtained for the other two devices. As can be seen, the model predicts that for $I_D > 200$ mA/mm, constant impact ionization corresponds to constant gate current. On the other hand, at low values of $I_D, V_{DG}$ must be made much higher to yield 3 mA/mm of impact ionization current; this in turn yields significantly more total gate current through the TFE component. The predicted gate current does rise much more quickly than the burnout current; this is due to the simplicity of our impact ionization expression (which becomes less valid at the high $V_{DS}$, low $I_D$ conditions required for low $I_D$ burnout). Nonetheless, the simple model does give physical insight into the burnout results.

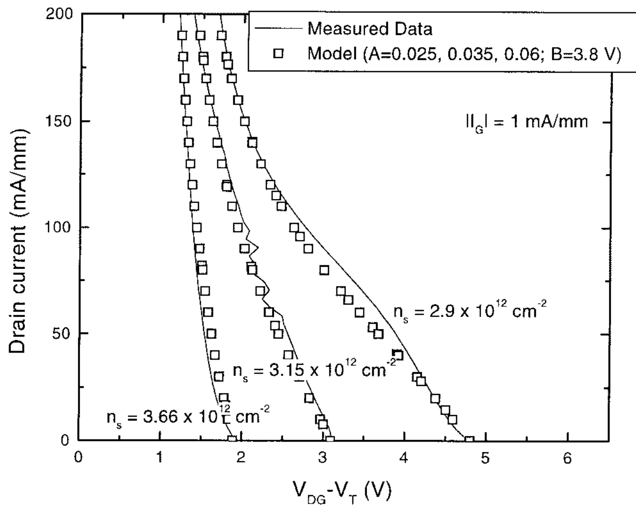



Fig. 8. Comparison of measured and modeled breakdown contours for 0.1-$\mu$m InAlAs/InGaAs HEMT's with three different sheet carrier concentrations at $|I_G| = 1$ mA/mm.

To explore the impact of design parameters on $BV_{\rm on}$, we have measured a sample set of 0.1 $\mu$m InAlAs/InGaAs HEMT's with varying values of extrinsic sheet carrier concentrations $(n_s)$ (Fig. 8) [9]. The model works well for all three devices with physically reasonable choices of fitting parameters; similar agreement is found for different $I_G$ criteria. Interestingly, increasing $n_s$ results in much more vertical $BV_{\rm on}$ contours. It is striking that three devices with such different $BV_{\rm off}$ values (1.9–4.7 V) approach similar $BV_{\rm on}$ values (1.2–1.7 V at 200 mA/mm). Our model explains this behavior: in the higher $n_s$ devices, $BV_{\rm off}$ is low; thus the field in the channel is lower, and the device moves more slowly from TFE into impact ionization. As a result, $BV_{\rm on}$ only degrades slightly. This view is supported by the model and by sidegate measurements on the higher $n_s$ devices [16], which show that these HEMT's move gradually into impact ionization. In contrast, we might expect devices with lower $n_s$ and higher $BV_{\rm off}$ to move more quickly into impact ionization. This may explain the discrepancy between our picture of $BV_{\rm off}$ and the previously suggested TFE-initiated impact ionization mechanism [10]—as $n_s$ is decreased and $BV_{\rm off}$ is enhanced, the contribution of impact ionization to $BV_{\rm off}$ is enhanced as well.

The devices' similarity in $BV_{\rm on}$ at higher currents seems to suggest that improvements in $BV_{\rm off}$ are not very meaningful from a power point of view. However, examination of allowable load lines on each device (Fig. 9) makes it clear that the *shape* of the $BV_{\rm on}$ locus is crucial to a device's power potential, as has been previously noted in MESFET's [19].

From a physical perspective, it is interesting to note which physical mechanism limits power for the different designs. As seen in Fig. 9, the load line for the high $n_s$ device intersects the $BV_{\rm on}$ locus close to the off-state; this device is thus limited almost exclusively by gate thermionic field emission. If one wished to improve the power performance of this device, approaches that suppress TFE would be most productive—e.g., improving the Schottky barrier height by increasing the aluminum content of the insulator or changing gate metals. On the other hand, the low $n_s$ device intersects the $BV_{\rm on}$ locus

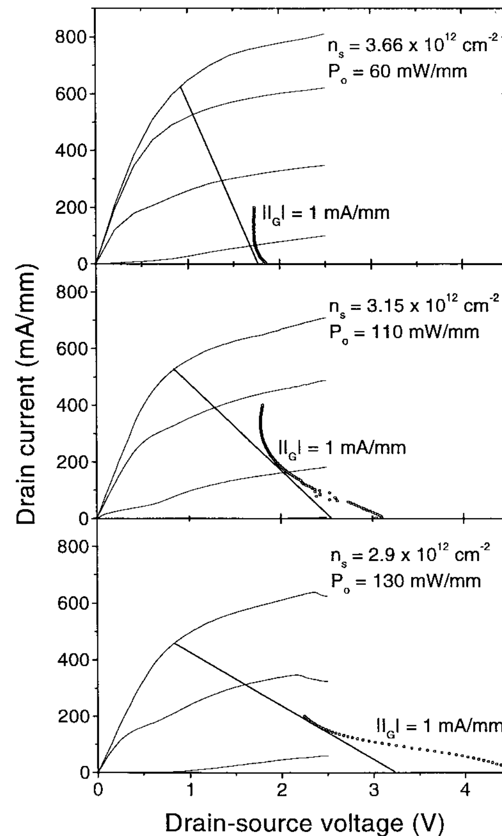



Fig. 9. Comparison of power load lines for InAlAs/InGaAs HEMT's with three different sheet carrier concentrations. Due to the shape of $BV_{\rm on}$, it is possible to bias the low $n_s$ device for greater power output.

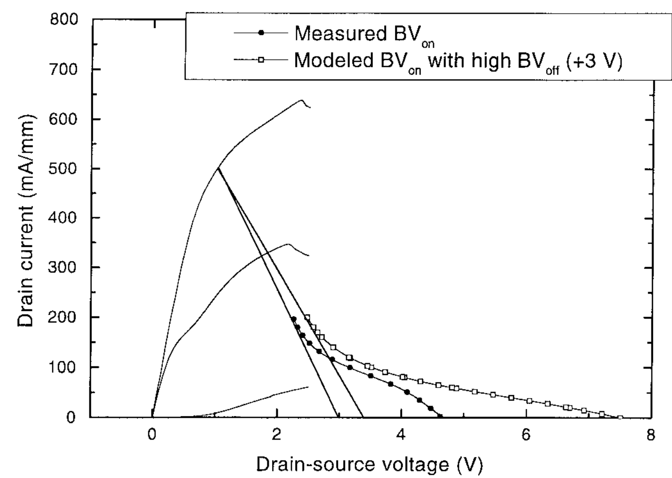



Fig. 10. Comparison of measured $BV_{\rm on}$ locus in low $n_s$ device and hypothetical $BV_{\rm on}$ locus of a device with identical impact ionization behavior but higher (+3 V) $BV_{\rm off}$ due to Schottky enhancement. Even though the hypothetical device has much higher $BV_{\rm off}$, the allowed load line provides only marginally more power output.

around $I_D = 160$ mA/mm. At this point impact ionization dominates $I_G$, so that increasing the Schottky barrier might not yield much improvement in the power performance.

To examine this question further, we have used our model to compare the $BV_{\rm on}$ locus of the low $n_s$ device with the $BV_{\rm on}$ locus of a hypothetical device with identical impact ionization behavior but an improved $BV_{\rm off}$ due to an enhanced Schottky barrier. Fig. 10 shows this comparison. As can be

seen, even though the hypothetical device has a significantly higher $BV_{\rm off}$, the maximum power output load line dictated by the $BV_{\rm on}$ locus is very similar to that of the lower $BV_{\rm off}$ device due to the dominance of impact ionization. Thus, improving the power performance of the low $n_s$ device might require alternative approaches, such as using a composite channel [8] or a channel with a lower indium content in order to suppress impact ionization.

## V. Conclusions

In summary, we have presented systematic study of on-state breakdown in HEMT's using the new *gate current extraction* technique. Careful sidegate and temperature-dependent measurements show that as the device is turned on, the breakdown mechanism changes from a TFE-dominated process to a carrier multiplication-dominated process. Based on this physical insight, we have created of a phenomenological physical model for breakdown which agrees well with all our experimental results, and explains the relationship between $BV_{\rm on}$ and the sheet carrier concentration. Our results suggest that the *shape* of $BV_{\rm on}$ must be considered in determining the power limits of a device. We further find that depending on device design, impact ionization, TFE, or a combination thereof can limit maximum power.

## References


[1] J. J. Brown, J. A. Pusl, M. Hu, A. E. Schmitz, D. P. Docter, J. B. Shealy, M. G. Case, M. A. Thompson, and L. D. Nguyen, "High-efficiency GaAs-based PHEMT C-band power amplifier," *IEEE Microwave Guided Wave Lett.*, vol. 6, pp. 91–93, Feb. 1996.

[2] M. Aust, H. Wang, M. Biedenbender, R. Lai, D. C. Streit, P. H. Liu, G. S. Dow, and B. R. Allen, "A 94-GHz monolithic power amplifier using 0.1 $\mu$m gate GaAs-based HEMT MMIC production process technology," *IEEE Microwave Guided Wave Lett.*, vol. 5, pp. 12–14, Jan. 1995.

[3] S. W. Chen, P. M. Smith, S. J. Liu, W. F. Kopp, and T. J. Rogers, "A 60-GHz high efficiency monolithic power amplifier using 0.1 $\mu$m PHEMT's," *IEEE Microwave Guided Wave Lett.*, vol. 5, pp. 201–203, June 1995.

[4] P. M. Smith, S. J. Liu, M. Y. Kao, P. Ho, S. C. Wang, K. H. Duh, S. T. Fu, and P. C. Chao, "W-band high efficiency InP-based power HEMT with 600 GHz $f_{\max}$," *IEEE Microwave Guided Wave Lett.*, vol. 5, pp. 230–232, July 1995.

[5] J. C. Huang, G. S. Jackson, S. Shanfield, A. Platzker, P. K. Saledas, and C. Weichert, "An AlGaAs/InGaAs PHEMT with improved breakdown voltage for X- and Ku-band power applications," *IEEE Trans. Microwave Theory Tech.*, vol. 41, pp. 752–758, May 1993.

[6] K. Y. Hur, R. A. McTaggart, B. W. LeBlanc, W. E. Hoke, A. B. Miller, T. E. Kazior, and L. M. Aucoin, "Double recessed AlInAs/GaInAs/InP HEMT's with high breakdown voltages," in *Proc. IEEE GaAs IC Symp.*, 1995, pp. 101–104.

[7] S. R. Bahl and J. A. del Alamo, "Breakdown voltage enhancement from channel quantization in InAlAs/n$^+$-InGaAs HFET's," *IEEE Electron Device Lett.*, vol. 13, pp. 123–125, Feb. 1992.

[8] G. Meneghesso, A. Mion, A. Neviani, M. Matloubian, J. Brown, M. Hafizi, T. Liu, C. Canali, M. Pavesi, M. Manfredi, and E. Zanoni, "Effects of channel quantization and temperature on off-state and on-state breakdown in composite channel and conventional InP-based HEMT's," in *IEDM Tech. Dig.*, 1996, pp. 43–46.

[9] C. S. Putnam, M. H. Somerville, J. A. del Alamo, P. C. Chao, and K. G. Duh, "Temperature dependence of breakdown voltage in InAlAs/InGaAs HEMTs: Theory and experiments," in *Proc. 7th Int. Conf. InP and Rel. Mat.*, 1997, pp. 197–200.

[10] S. R. Bahl, J. A. del Alamo, J. Dickmann, and S. Schildberg, "Off-state breakdown in InAlAs/InGaAs MODFET's," *IEEE Trans. Electron Devices*, vol. 42, pp. 15–22, Jan. 1995.

[11] M. H. Somerville and J. A. del Alamo, "A model for tunneling-limited breakdown in high-power HEMT's," in *IEDM Tech. Dig.*, 1996, pp. 35–38.

[12] H. Rohdin, C. Su, N. Moll, A. Wakita, A. Nagy, V. Robbons, and M. Kauffman, "Semi-analytical analysis for optimization of 0.1 $\mu$m InGaAs channel MODFET's with emphasis on on-state breakdown and reliability," in *Proc. 7th Int. Conf. InP and Rel. Mat.*, 1997, pp. 357–360.

[13] J. Dickmann, S. Schildberg, A. Geyer, B. E. Maile, A. Schurr, S. Heuthe, and P. Narozny, "Breakdown mechanisms in the on-state mode of operation of InAlAs/InGaAs PHEMT's," in *Proc. 6th Int. Conf. InP and Rel. Mat.*, 1994, pp. 335–338.

[14] M. H. Somerville, J. A. del Alamo, and W. Hoke, "A new physical model for the kink effect in InAlAs/InGaAs HEMT's," in *IEDM Tech. Dig.*, 1995, pp. 201–204.

[15] M. H. Somerville, R. Blanchard, J. A. del Alamo, P. C. Chao, and K. G. Duh, "A new gate current extraction technique for measurement of on-state breakdown in HEMT's," *IEEE Electron Device Lett.,* vol. 19, pp. 405–407, Nov. 1998.

[16] ——, "On-state breakdown in power HEMTs: Measurements and modeling," in *IEDM Tech. Dig.*, 1997, pp. 553–556.

[17] P. C. Chao, W. Hu, H. DeOrio, A. W. Swanson, W. Hoffman, and W. Taft,"Ti-gate metal induced PHEMT degradation in hydrogen," *IEEE Electron Device Lett.*, vol. 18, pp. 441–443, Sept. 1997.

[18] A. A. Moolji, S. R. Bahl, and J. A. del Alamo, "Impact ionization in InAlAs/InGaAs HFET's," *IEEE Electron Device Lett.*, vol. 15, pp. 313–315, Aug. 1994.

[19] T. A. Winslow and R. J. Trew, "Principles of large-signal MESFET operation," *IEEE Trans. Microwave Theory Tech.*, vol. 42, pp. 935–942, June 1994.



**Mark H. Somerville** received the B.S. degree in electrical engineering and the B.A. degree in liberal arts from the University of Texas, Austin, in 1990, the B.A. degree in physics from Oxford University, Oxford, U.K. in 1992, the M.S. and Ph.D. degrees in electrical engineering from the Massachusetts Institute of Technology (MIT), Cambridge, in 1993 and 1998, respectively. His doctoral research focused on fabrication, modeling and characterization of InAlAs/InGaAs HEMT's for power applications.

In September 1998, he joined the Department of Physics and Astronomy of Vassar College, Poughkeepsie, NY, as an Assistant Professor. From 1989 to 1990, he was a Systems Engineer at SEMATECH, Austin, where he worked on the development of modular automation approaches for semiconductor manufacturing. During this time, he also worked at the University of Texas on Monte Carlo simulation of InAlAs/InGaAs HBT's. At MIT, he conducted research on charge control and transport heavily-doped quantum wells from 1992 to 1993.

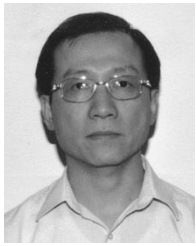
**Roxann R. Blanchard** (S'93) received the B.S.E.E. degree from the University of Vermont, Burlington, in 1989, and the M.S.E.E. degree from the Massachusetts Institute of Technology (MIT), Cambridge, in 1994. She is currently pursuing the Ph.D. degree in electrical engineering at MIT, where she has worked on the physics and technology of InP-channel InP HEMT's.

From 1989 to 1994, she was with the Raytheon Company, where she developed radiation-hardened CMOS and BiCMOS processes. More recently, she has been working to determine the effects of hydrogen on the reliability of InP HEMT's.

**Jesus A. del Alamo** (S'79–M'85–SM'92) received the degree of Telecommunications Engineer from the Polytechnic University of Madrid, Spain, in 1980, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1983 and 1985, respectively. His Ph.D. dissertation was on minority carrier transport in heavily doped silicon.

From 1977 to 1981 he was with the Institute of Solar Energy of the Polytechnic University of Madrid, working on silicon solar cells. From 1985 to 1988, he was Research Engineer with NTT LSI Laboratories, Atsugi, Japan, where he conducted research on heterostructure field-effect transistors based on InP, InAlAs, and InGaAs. Since 1988, he has been with the Department of Electrical Engineering and Computer Science, the Massachusetts Institute of Technology (MIT), Cambridge, where he is currently a Professor. His interests include high-power high-frequency high-electron mobility transistors based on compound semiconductors, Si bipolar transistors, and Si metal-oxide-semiconductor field-effect transistors.

Prof. del Alamo was an NSF Presidential Young Investigator from 1991 to 1996. In 1992, he was awarded the Baker Memorial Award for Excellence in Undergraduate Teaching at MIT. In 1993, he received the H. E. Edgerton Junior Faculty Achievement Award at MIT.



**K. George Duh** received the B.S.E.E. degree from National Taiwan University, Taipei, Taiwan, R.O.C., in 1977, the M.S.E.E. degree from Syracuse University, Syracuse, NY, in 1981, and the Ph.D. degree in electrical engineering from University of Minnesota, Minneapolis, in 1984.

From 1983 to August 1984, he was with Honeywell Corporate Technology Center, Minneapolis, where he worked on 30 GHz monolithic receive module designs. In 1984, he joined the General Electric (now Lockheed Martin) Electronics Laboratory, where he is currently Manager of Advanced Components in Microwave Electronics Division at Sanders, a Lockheed Martin Company, Nashua, MH. He has led a very successful program for NASA/JPL to develop cyrogenic HEMT receivers for the Voyager/Neptune encounter mission from 1984 to 1989. He is actively involved in the development of high-performance microwave semiconductor devices and assocaited (both hybrid and MMIC) circuits, particular emphasis on HEMT's based on GaAs and InP technologies. He has authored or coauthored more than 110 publications and presentations in the area of compound semiconductor devices and associated applications.

**P. C. Chao**, photograph and biography not available at the time of publication.