A RF Power LDMOS Device on SOI

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Abstract: We have fabricated a partially-depleted SOI Laterally Diffused MOSFET (LDMOSFET) that is designed for use in radio frequency (RF) power amplifiers (PA) for portable applications. The device is fabricated on thin film SIMOX wafers and is suitable for integration with SOI CMOS. A high breakdown voltage is attained using a simple body contact scheme and the RF performance is exceptional.

Introduction: There is considerable interest in the development of single-chip wireless systems in which digital, RF, and analog circuits are integrated onto a single die [1]. Due to its low parasitics and effective isolation, SOI technology has great potential for these applications, particularly as they migrate to higher frequencies and lower voltages [2]. In this research, we are investigating one of the functions that is most difficult to integrate into any single-chip RF technology: the RF power amplifier. In particular, we are studying process and device design issues for a power LDMOSFET on SOI that is suitable for integration with SOI-CMOS.

Fabrication: A cross section of the device is shown in fig. 1, a list of critical dimensions is given in fig. 2, and the process flow is shown in fig. 3. The devices were fabricated on p-type <100> SIMOX with a t_{si} of 200 nm, a t_{box} of 400 nm, and a resistivity of 10-20 Ohm-cm. A source-side boron implant of 1.3e13 cm^{-2} dose and 25KeV energy was diffused under the gate for 300 minutes at 1000 C to form the laterally diffused body doping profile. A phosphorous implant of 3e12 cm^{-2} dose and 55 KeV energy was used to create the 0.5 μm long LDD region, and an arsenic implant of 5e15 cm^{-2} dose and 25 KeV energy created the source and drain regions. After the implants, a region beneath the source remains p-type, creating a low resistance body contact which extends along the entire width of the device. The body contact is a result of the LDMOS fabrication process, and no additional implants or other fabrication steps are needed. The device is fully dielectrically isolated from other devices on the same die.

Results and Discussion: The output characteristics of a L_g=0.7 μm device are shown in fig. 4, and the transfer characteristics are shown in fig 5. The threshold voltage of the device is 1.5 V, and the peak transconductance is 65 μS/μm. The device transconductance rises sharply and then settles to a flat plateau. This is typical of LDMOS devices, and underlies the excellent linearity of this device. Microwave characterization of the devices was carried out. The short circuit current gain (h_{21}) and the maximum available power gain (G_{ma}) are plotted in fig. 6. By extrapolation, f_t is 13 GHz and f_{max} is 18 GHz for a device with a 20 μm gate width. This value of f_t compares well with modern discrete RF LDMOS devices with the same breakdown voltage [3].

A major concern of using thin film SOI technology for PA applications is that a low resistance body contact is essential to avoid problems associated with floating body effects. The body contact must prevent 'kink' related problems including poor on-state breakdown voltage and excessive output conductance. We have studied body contact design issues by fabricating devices with floating bodies, and with body contacts of different body resistance. By setting L_{body} to zero and L_{source} to 11 μm, a floating body device was created. The characteristics of this device are contrasted with a standard device in fig. 7. The body contact delays the turn-on of the body-source diode, preventing bipolar latch, and dramatically increases both the on-state and off-state breakdown voltage. The off-state breakdown voltage of the body-tied device is greater than 20 V, and the on-state breakdown voltage is greater than 10 V. Devices with an increased body contact resistance were fabricated by keeping L_{body} at its nominal value, and raising L_{source} to 50 μm. Fig 8 shows that even a moderately elevated resistance results in a kink in the I-V characteristics and significantly reduces the on-state breakdown voltage.

Conclusion: An RF SOI LDMOS device with a high breakdown voltage and a high cutoff frequency has been demonstrated. A simple body contact scheme effectively suppresses adverse floating body effects. This is a very promising technology for future integrated power amplifiers.

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.[1] Abidi, A. A., et al "The Future of CMOS Wireless Tranceivers", IEEE International Solid State Circuits Conference Digest of Technical Papers pp. 118-119, 1997

[2] W. M. Huang, et al. "TFSOI - Can it meet the challenge of single chip portable wireless systems?" IEEE International SOI Conference Proceedings. pp. 1-3, 1997

[3] I. Yoshida, "2 G-Hz Si Power MOSFET Technology", International Electron Device Meeting Technical Digest, pp. 51-54, 1997

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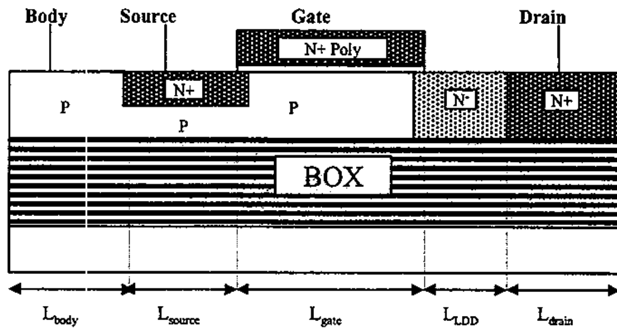

Fig 1. Sketch of RF SOI LDMOS device

L_{body}= 5.5 μm
L_{source}=5.5 μm
L_{gate}=0.7 μm
L_{LDD}=0.5 μm
L_{drain}=7.0 μm
t_{poly}=0.4 μm
t_{gox}=30 nm
t_{si}=0.2 μm
t_{box}=0.4 μm

Fig 2. Nominal device dimensions

- Isolation (LOCOS)
- Gate Oxidation
- Polysilicon deposition and doping
- Gate Patterning
- Body Doping Implant
- Body Doping Anneal
- LDD Implant
- S/D Implant
- R.T.A (1000 °C, 20s)
- Backend Processing

Fig 3. Fabrication Process

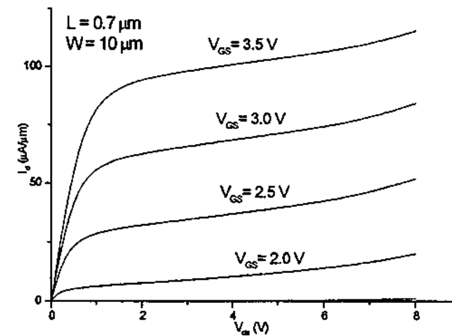

Fig 4. Output Characteristics

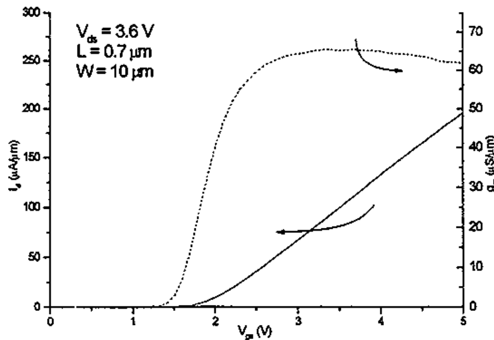

Fig 5. Transfer Characteristics

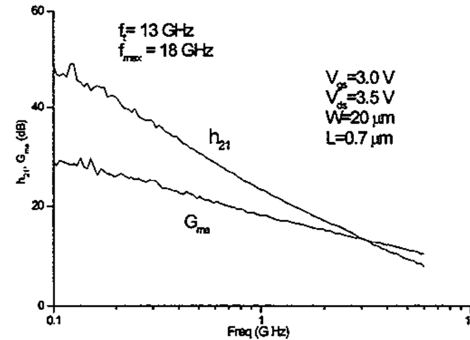

Fig 6. High frequency Characteristics

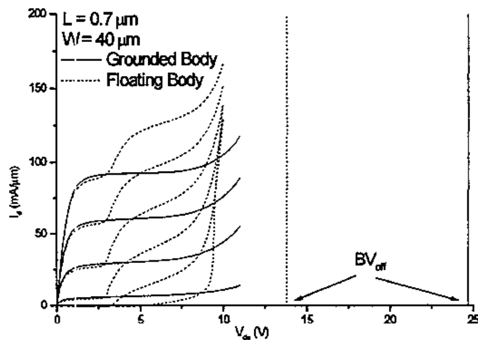

Fig 7. Output characteristics showing breakdown

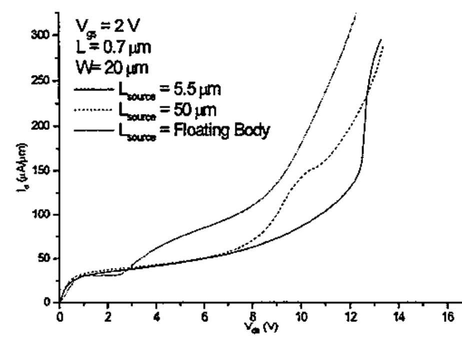

Fig 8. On-state breakdown