Off-State Breakdown in Power pHEMT's: The Impact of the Source

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***Abstract*— Conventional wisdom suggests that in pseudomorphic high electron mobility transistors (pHEMT's), the field between the drain and the gate determines off-state breakdown, and that the drain to gate voltage therefore sets the breakdown voltage of the device. Thus, the two terminal breakdown voltage is a widely used figure of merit, and most models for breakdown focus on the depletion region in the gate-drain gap, while altogether ignoring the source. We present extensive new measurements and simulations that demonstrate that for power pHEMT's, the electrostatic interaction of the source seriously degrades the device's gate-drain breakdown. We identify the key aspect ratio that controls the effect, $L_G : x_D$, where L_G is the gate length and x_D is the depletion region length on the drain. This work establishes that the design of the source must be taken into consideration in the engineering of high-power pHEMT's.**

***Index Terms*—Breakdown voltage, electric breakdown, electron tunneling, power HEMT's power MODFET's.**

I. Introduction

ALTHOUGH initially targeted at low-noise applications, the AlGaAs/InGaAs pseudomorphic high electron mobility transistor (pHEMT) is enjoying significant success in microwave and millimeter wave power applications [1]–[3]. This success has been accompanied by the recognition that off-state gate conduction plays a critical role in determining the large-signal performance, particularly the saturated power output, of these devices [4]. Further use of the pHEMT therefore hinges on a full understanding of the device's off-state breakdown behavior, both to facilitate improved device design and to allow accurate modeling of the pHEMT in circuit design.

There have been numerous theoretical and experimental studies of breakdown in GaAs and InP-based FET's. Experimentally, novel recess and channel designs [5]–[9] have led to significant breakdown voltage improvements. Theoretical explanations of breakdown behavior have appealed to impact ionization [10]–[13], tunneling and thermionic field emission [14]–[16], or combinations thereof [17]–[19]. Although such theories can account for the three-terminal bias-dependence of gate conduction in the on-state [14], [17], they generally consider off-state breakdown to be a two-terminal phenomenon. This approach reflects the conventional wisdom that, in the off-state, breakdown is purely determined by the field between gate and drain, and hence, by the drain-gate voltage (V_{DG}). Thus, a two-terminal measurement of the gate diode is usually considered sufficient for qualifying a device's off-state breakdown behavior.

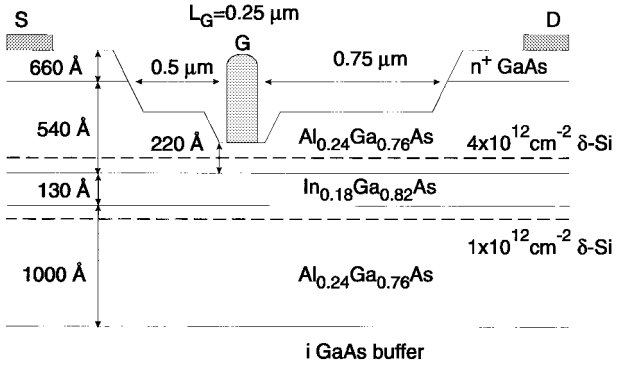

Fig. 1. Schematic cross section of AlGaAs/InGaAs double-heterostructure pHEMT used in this work.

In this paper we examine both two-terminal and three-terminal off-state breakdown behavior in state-of-the-art power pHEMT's. Our experiments and simulations demonstrate that the two-terminal description of breakdown in pHEMT's is inappropriate for modern devices. In particular, we find that in power pHEMT's the electrostatic interaction of the source seriously degrades the device's gate-drain breakdown voltage, and must be taken into consideration in device design.

II. Experimental

As a vehicle for this study we have used a state-of-the-art $L_G = 0.25$ μm double heterostructure pHEMT fabricated at Texas Instruments. The transistor exhibits excellent power performance [output power of 1 W, associated gain of 11 dB, and power added efficiency of 60% at 10 GHz for a gate width (W_G) of 1200 μm] and device characteristics (extrinsic transconductance of 400 mS/mm, maximum current density of 550 mA/mm). Fig. 1 presents a cross-section of the device. A number of design aspects contribute to the device's excellent power performance: the device features an asymmetric double recess, delta-doping, and a narrow channel with relatively low indium content, yielding a two-terminal off-state breakdown voltage between 20 and 25 V (Fig. 2). Devices with $W_G = 600$ μm and $W_G = 1200$ μm were characterized; no significant differences in behavior were observed in different width devices.

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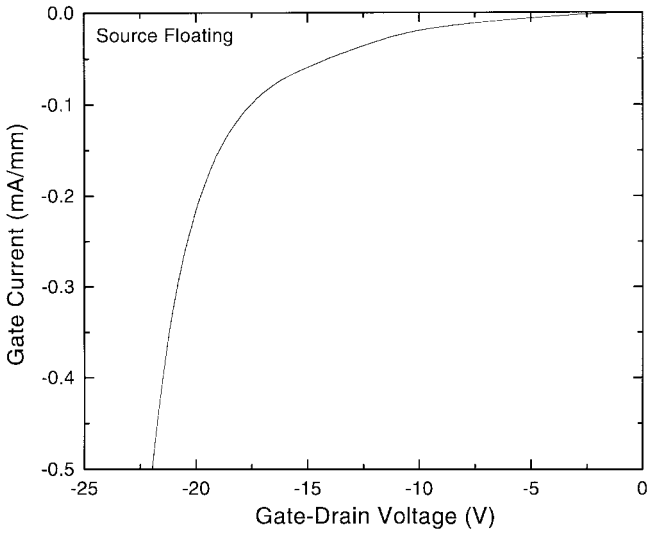

Fig. 2. Reverse gate-drain current–voltage characteristics measured with the source floating at room temperature.

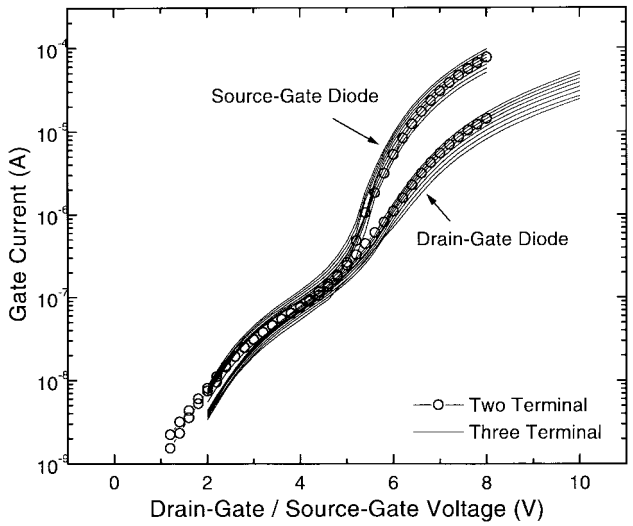

Fig. 3. Comparison of two- and three-terminal measurements of the drain-gate and source-gate diodes. The multiple three-terminal measurements were performed with the gate biased at different voltages slightly below threshold. The asymmetry of the device is apparent.

The asymmetry of the device is obvious in Fig. 3, which compares the behavior of the source-gate and drain-gate diodes in both two- and three-terminal configurations. At low voltages, the drain-gate and source-gate diodes behave identically, while at higher voltages ($V_{DG}, V_{SG} > 5$ V) the source-gate diode exhibits substantially higher leakage currents than the drain-gate diode, as the depletion region extends into the asymmetric wide recess. In addition, in both configurations the three-terminal behavior closely maps the two-terminal behavior. This appears to indicate that the physics of two-terminal breakdown are identical to those involved in three-terminal breakdown.

In order to understand the breakdown mechanism in this device, we have performed two- and three-terminal measurements as a function of temperature. Two-terminal measurements show the gate-drain diode is thermally activated only for low values of V_{DG} ($V_{DG} \approx 4$ V), and even in this range the activation energy is much smaller (0.05 eV) than the Schottky barrier height on AlGaAs (about 0.8 eV [22]). Three-terminal measurements as a function of temperature are consistent with the two-terminal findings. In Fig. 4 we plot the measured drain-gate and drain-source breakdown voltages (BV_{DG} and BV_{DS}) at several current criteria as proposed by Bahl *et al.* [20]. Two features are note-worthy: first, the drain-gate and drain-source breakdown voltages track each other, indicating that breakdown is limited by the drain-gate diode. In addition, the breakdown's temperature dependence is negative for low current criteria, and becomes zero for high current criteria. Such temperature dependence suggests that breakdown mechanism is dominated by a combination of thermionic emission and tunneling at low currents, and evolves to pure tunneling at higher currents. Were impact ionization dominant, a positive temperature dependence would be expected.

Thus far the picture presented of breakdown in these devices is a very conventional one, which would appear to support the belief that breakdown is purely determined by V_{DG}. However, careful examination of drain current injection measurements of breakdown show that the situation is not so simple.

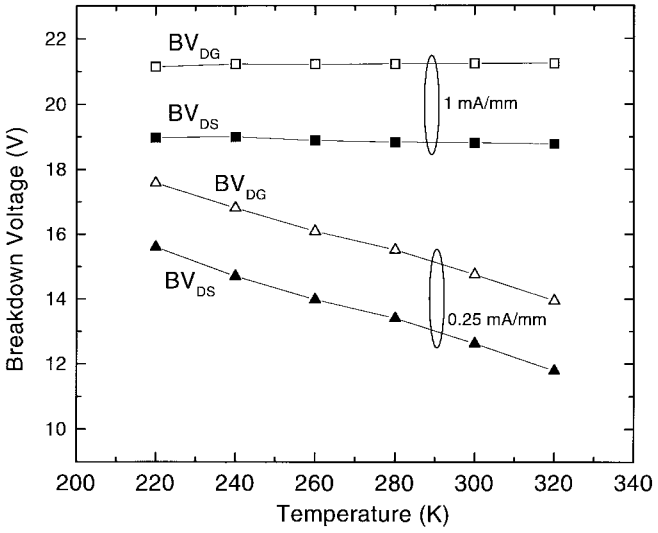

Fig. 4. Temperature dependence of breakdown at $I_D = 0.25$ mA/mm and $I_D = 1$ mA/mm. Note that BV_{DG} and BV_{DS} track each other, and that the temperature dependence of breakdown is negative at low current criteria, and approximately zero at higher current criteria.

The drain current injection technique consists of injecting a constant current (e.g., 1 mA/mm) through the drain while sweeping the gate voltage from on to off [20]. By measuring the gate current and the drain voltage, it is possible to track directly the breakdown behavior of the device as it is turned off. According to the conventional picture of drain-gate diode breakdown, once the device is turned off, V_{DG} should stay at a constant value such that the drain-gate diode can support the full 1 mA/mm of injected current. This is BV_{DG}. This behavior has been observed in a number of devices [20].

The drain-current injection technique reveals that the power pHEMT behaves in a strikingly different way. In Fig. 5 we plot typical room temperature drain current-injection results for the pHEMT under a variety of current criteria. Note that although the devices do in some cases exhibit oscillations in the on-state due to impedance matching difficulties in our temperature-

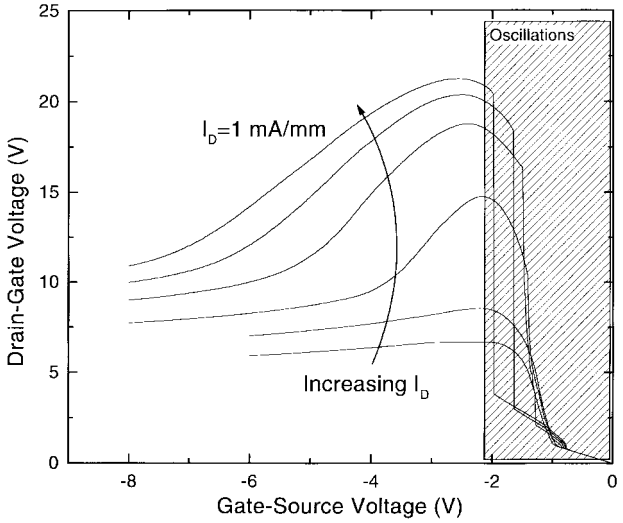

Fig. 5. Drain current injection results at room temperature for several current criteria (I_D = 0.02, 0.05, 0.25, 0.5, 0.75, and 1.0 mA/mm) for power pHEMT. The pHEMT exhibits classical drain-gate breakdown behavior at low current criteria ($I_D < 0.1$ mA/mm), but for higher current criteria, BV_{DG} drops significantly as V_{GS} is reduced.

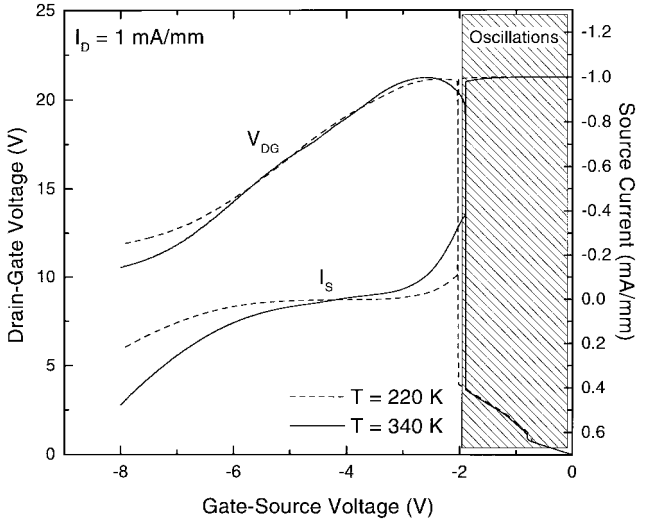

Fig. 6. Drain current injection results at high and low temperature for I_D = 1 mA/mm. The drop in BV_{DG} appears virtually independent of temperature.

controlled measurement apparatus, the oscillations disappear in the off-state, as the device's gain drops. Thus, we do not expect the on-state oscillations to affect measurements in the off-state. At low currents ($I_D = 0.02$, 0.05 mA/mm), we observe classical off-state drain-gate breakdown behavior with V_{DG} fairly independent of V_{GS} below threshold. At higher current criteria ($I_D = 0.25$, 0.5, 0.75, 1.0 mA/mm), though, we see a profound change in the behavior of BV_{DG}. For $I_D = 1$ mA/mm, for example, as the device is turned off, V_{DG} rises rapidly to reach a peak value of about 21 V at $V_{GS} = -3$ V, but then drops by more than 10 V as V_{GS} is swept, and finally saturates somewhat at the most negative values of V_{GS}. Notably the drop in V_{DG} increases both in magnitude and in breadth as I_D (or BV_{DG}) increases. Such behavior is clearly inconsistent with the simple two-terminal picture of drain-gate breakdown in which V_{DG} should remain at the constant voltage necessary to support the injected drain current. Furthermore, such a drop in V_{DG} is clearly undesirable, as it implies that the two-terminal breakdown measurement markedly over-estimates the actual breakdown voltage of the device in real-world large signal applications, in which the gate voltage might sweep substantially below threshold.

This peculiar drop in V_{DG} at high I_D criteria is observed throughout the temperature range we consider, as shown in Fig. 6. Indeed, there is virtually no change in the evolution of V_{DG} over the entire temperature range. This implies that tunneling remains the dominant mechanism, regardless of the value of V_{GS}. Fig. 6 also makes it clear that it is V_{GS}, not the leakage characteristics of the source-gate diode, that impact the device's drain-gate breakdown behavior: at 220 K, V_{DG} drops by 10 V, even though leakage on the source-gate diode is strongly suppressed.

Since it is clear that the source is having a major effect on the breakdown behavior of the device, we have also explored the influence of the drain on the breakdown behavior

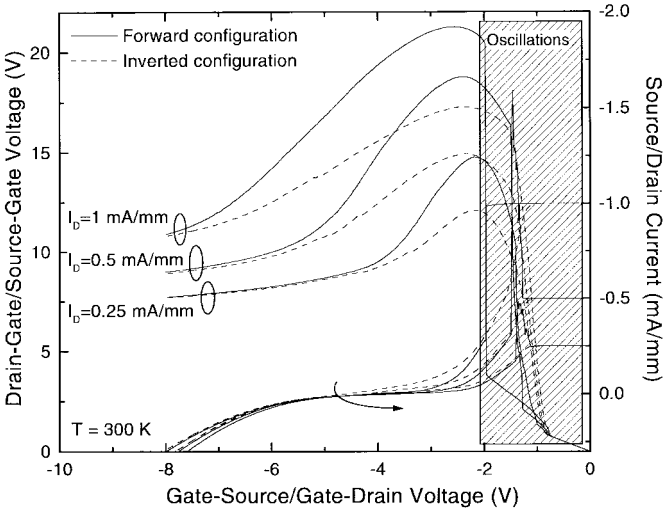

Fig. 7. Drain current injection results for pHEMT in normal and inverted configuration. The device's asymmetry is reflected by the fact that the source-gate voltage drops less than the drain-gate voltage for the same current criteria. Note that at sufficiently negative gate voltages, the asymmetry disappears.

of the source. Here we have simply reversed source and drain—in other words, the measurement consists of injecting a given current into the source, and sweeping the gate-drain voltage from above V_T to significantly below V_T. These results are plotted in Fig. 7 for several current criteria. As can be seen, the drain-gate voltage has a similar, albeit less significant impact on the behavior of the gate-source breakdown voltage. Interestingly, BV_{DG} and BV_{SG} approach approximately identical values as V_{GS} and V_{GD} are made more negative.

To summarize the results of our drain current injection measurements, we have found that 1) at 1 mA/mm, the drain-gate diode appears to breakdown due to tunneling regardless of the value of V_{GS}; 2) making V_{GS} more negative degrades the breakdown voltage of the drain-gate diode, particularly at high breakdown voltages; 3) the effect reflects the asymmetry

of the device; and loss of BV_{DG} is approximately temperature-independent. Because many circuit topologies rely on swinging the gate below threshold, understanding and correctly modeling this effect is essential.

III. Discussion and Model

Clearly a two-terminal picture of breakdown cannot explain the dependence of BV_{DG} on V_{GS}. Nonetheless, off-state breakdown in MESFET's and pHEMT's is typically determined in practice by a two-terminal measurement, and accordingly most models consider only the gate and the drain, while ignoring the source [10], [11].

It is worth noting that the three-terminal behavior we observe is, in certain respects, very simple. In particular, the fact that the drop in V_{DG} is temperature independent suggests that the effect is not related to the substrate or to impact ionization, and indeed that tunneling remains the dominant breakdown mechanism regardless of V_{GS}. Since tunneling current is exponentially dependent on electric field, the quantity that will determine breakdown is the field beneath the drain end of the gate. Possibly, changing V_{GS} modifies the field distribution at the drain end of the gate, and thus changes the drain-gate tunneling current. Such an effect would be similar to (but different from) short channel effects such as drain-induced barrier lowering [23]. Gauss' Law implies that the field directly beneath the gate is determined by the charge distribution on the gate. In other words, if electron tunneling from the gate is the relevant mechanism, we need only understand how the charge distribution on the gate changes with V_{DG} and with V_{GS}.

Predicting the charge distribution in the two-terminal case is relatively tractable—conformal transformations can provide a solution for the electrostatics either by assuming a semi-infinite gate [10] or by imposing a symmetry condition on the electrostatics beneath the gate [11]. While these models provide excellent insight into the two-terminal problem, they obviously cannot account for the three-terminal behavior of breakdown.

Understanding the charge distribution in the three-terminal case is more challenging, but a simple conformal transform (see Appendix) does provide some physical insight. The transform allows a solution for the potential distribution due to a line charge in the vicinity of a finite equipotential gate. Since in a delta-doped HEMT structure the dopants are tightly confined to one layer, the charge distribution on a finite gate due to a line charge is approximately analogous to the differential change in charge distribution that results from a small extension of the depletion region (see inset of Fig. 8). Thus, the conformal transformation of the line charge problem tells us where additional charge will be imaged as the depletion regions on the drain or source sides of the gate are extended.

In Fig. 8, we plot the calculated image charges on a 0.25 μm gate for single charges located 200 Å below the plane of the gate and at several positions to the left of the gate edge. This figure reveals that once the depletion region begins to extend beyond the gate edge, the additional image charge on the gate is not simply concentrated at the closest gate edge as some models suggest [13], but in fact is distributed across the entire gate length. Furthermore, the charge distribution shows a prominent peak at *the opposite* end of the gate, so that changing the extent of the depletion region on the source side of the gate can perceptibly change the charge distribution on the drain side of the gate.

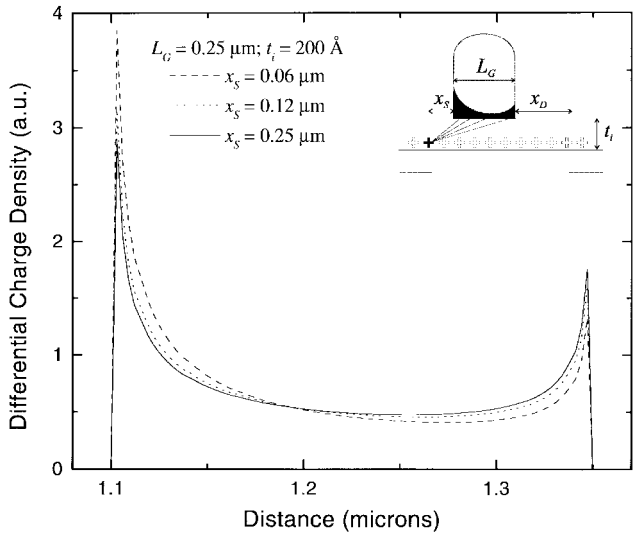

Fig. 8. Magnitude of calculated surface charge density on a finite gate due to a single line charge for three different charge positions, as indicated in the inset. Note that although the line charges are located in the gate-source gap, the conformal transform predicts that the corresponding image charges spread across the entire gate length, and are strongly peaked at *both* ends of the gate.

Fig. 9 shows how this can explain the dependence of BV_{DG} on V_{GS}. In Fig. 9(a), the device is biased such that the field at the drain end of the gate is sufficient to support a given current on the drain-gate diode. The charge on the gate consists of three components: the charge necessary to deplete the channel directly beneath the gate, the charge necessary to open the depletion region on the drain side of the gate, and the charge necessary to open the depletion region on the source side of the gate. When the gate to source voltage is made more negative [Fig. 9(b)], the depletion region on the source side of the gate is extended. A fraction of the newly exposed source depletion-region charge is imaged at the *drain end* of the gate; in this way, the total charge at that edge of the gate is increased. This raises the field there, and results in increased current on the drain-gate diode. In order to bring the current back down to the selected criteria, the drain to gate voltage must be decreased, so that the field at the drain end of the gate is reduced to its original value [Fig. 9(c)].

While such an explanation appears at first sight similar to other short channel effects, careful consideration of the geometry indicates that this problem is subtly different. In short channel effects like drain-induced barrier lowering, the relevant geometry is the ratio of gate length (L_G) to insulator thickness (t_i). The pHEMT's under consideration, though, have $L_G : t_i$ aspect ratios of about $10:1$. Although $L_G : t_i$ will come into play, the more relevant geometrical consideration for this problem is arguably the ratio of gate length to the extension x_D of the depletion region (see Fig. 10). In the case that $x_D \ll L_G$ [Fig. 10(a)], the edge of the drain depletion region is much closer to the drain edge of the gate than is

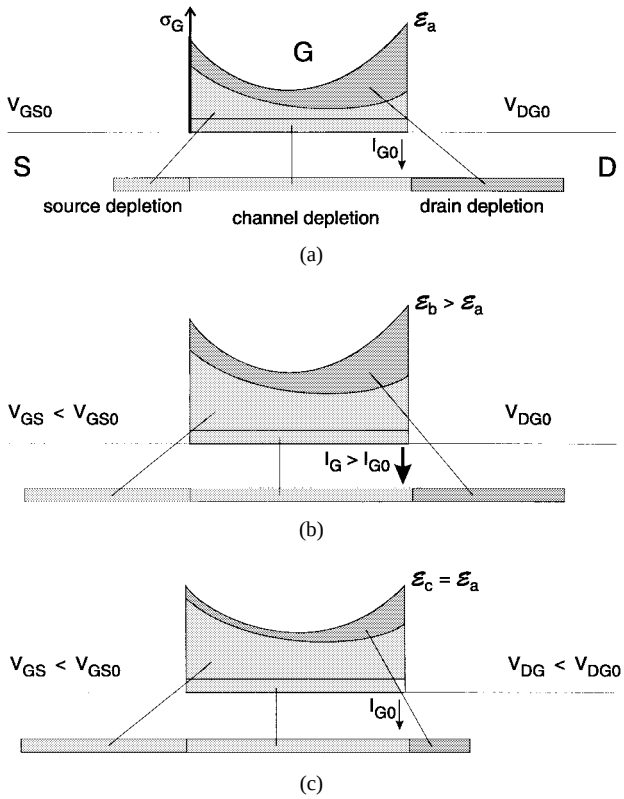

Fig. 9. Proposed mechanism for source-induced breakdown reduction. (a) Initially the device is biased such that the gate-drain diode supports a certain reverse leakage current. As V_{GS} is made more negative, the additional lateral depletion toward the source is partially imaged on the drain end of the gate. (b) This increases the field at the drain end of the gate, yielding a larger tunneling current. (c) In order to recover the original current level, V_{DG} must be reduced. Thus, the source significantly degrades drain-gate breakdown.

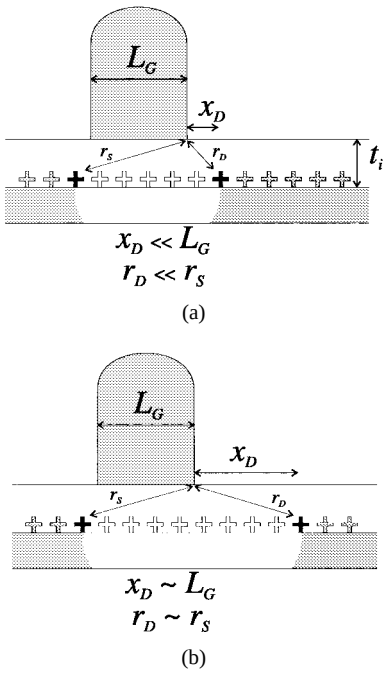

Fig. 10. Schematic showing relevant aspect ratio for determining impact of source on drain-gate breakdown voltage. (a) When $L_G : x_D$ is large, the source has little impact, because r_S, the distance from the edge of the source depletion region to the drain edge of the gate, is much greater than r_D, the distance from the edge of the drain depletion region to the drain edge of the gate. (b) As $L_G : x_D$ approaches 1, these distances become comparable, so that the source is expected to affect the drain-gate breakdown voltage significantly.

the edge of the source depletion region ($r_D \ll r_S$); thus, in this condition, V_{DG} will tightly control the electrostatics in the vicinity of the gate edge, and changes in V_{GS} should not have much impact on the tunneling current. On the other hand, when $L_G : x_D$ is larger [Fig. 10(b)], the edge of the source depletion region is no further from the drain edge of the gate than is the edge of the drain depletion region ($r_D \approx r_S$). In this case, increasing depletion on the source side of the gate should result in significant image charge on the drain edge of the gate.

Such a model explains all our experimental observations. For low current criteria, the impact of the source is expected to be minimal, as the extension of the depletion region on the drain side of the gate is small, so that $x_D \ll L_G$. At higher current criteria, the depletion region on the drain is extended, and the drain voltage is therefore much more sensitive to variations in the gate-source voltage. This is exactly what we observed in Fig. 5. The model also predicts that the saturating behavior observed in Fig. 5: as V_{DG} drops, its dependence on V_{GS} is reduced, both because x_D is dropping, and because the depletion length on the source side of the gate is increasing.

Furthermore, since the mechanism is purely a result of electrostatics and tunneling (at higher current criteria), we expect that the drop in V_{DG} should be relatively temperature-independent, as Fig. 6 shows. Finally, the asymmetry of the device layout (Fig. 1) is expected to yield an asymmetry in the effect, as seen in Fig. 7. Because of the proximity of the heavily-doped cap, the relevant aspect ratio ($L_G : x_D$) is larger when drain and source are reversed than when the transistor is in the normal configuration (assuming a constant current criteria); thus the effect is not so pronounced in the reverse configuration. Importantly, the model also predicts that as V_{GS} and V_{GD} increase further, the difference between drain-gate and source-gate breakdown voltages should disappear, as the relevant depletion length drops, bringing the device back into the symmetric regime. Fig. 7 demonstrates this effect beautifully.

In order to test the plausibility of this model, we have performed simple two-dimensional electrostatic simulations using MEDICI HD-AAM. Since we are simulating the off-state, transport models are not relevant, and we expect the results to be reasonably accurate. The structure is identical to the one in Fig. 1. Fig. 11 shows the field magnitude directly beneath the gate at three bias conditions. The shape of the field distribution at all three biases is strikingly similar to the predictions of the conformal transformation. In the first bias condition ($V_{DG} = 20$ V, $V_{GS} = -2$ V), the field is peaked at both the source and the drain end of the gate. When V_{GS} is changed to -4 V, the field at the source end of the gate increases, but the field at the drain end increases as well, *even though V_{DG} is held constant*. This increase in the field at the drain end will result in significantly higher leakage current on the drain-gate diode, due to the exponential dependence of tunneling current on electric field. In order to suppress this additional leakage, a reduction in V_{DG} is necessary. The

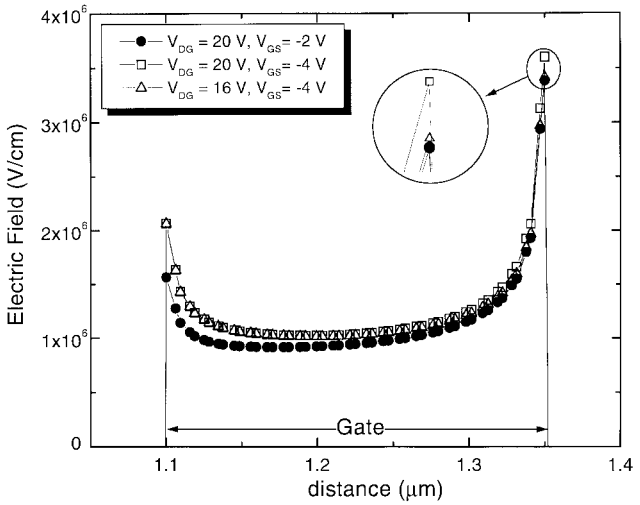

Fig. 11. MEDICI simulations of electric field beneath the gate for three bias conditions. Breakdown is associated with the peak field at the drain end of the gate; as V_{GS} is made more negative, V_{DG} must be reduced in order to keep the peak drain field constant.

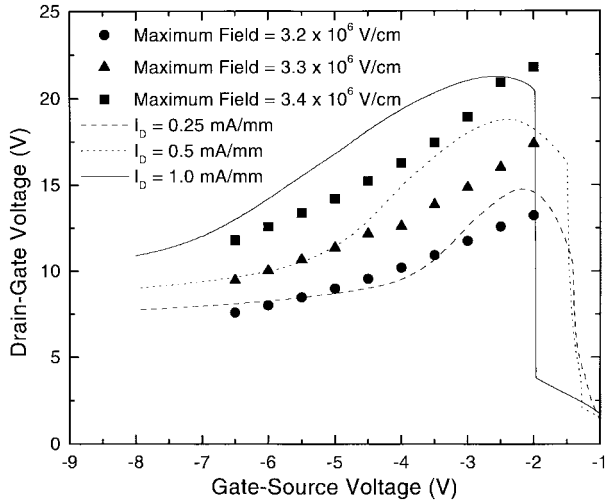

Fig. 12. Comparison of constant current criteria measurements with constant field criteria MEDICI simulations. The simulations effectively capture the qualitative behavior of BV_{DG}.

third bias condition ($V_{DG} = 16$ V, $V_{GS} = -4$ V) shows that because of the greater extent of the drain depletion region, the necessary drop in V_{DG} can be large—in this case, V_{DG} must be reduced by about 4 V in order to recover the original field, while V_{GS} only changed 2 V.

As we have argued above, it is reasonable to expect that the breakdown voltage is determined by the maximum field beneath the gate, given the exponential relationship between the tunneling current and the width of the tunneling barrier. In other words, *a constant drain current condition should be equivalent to a constant maximum field condition at the drain end of the gate*. With this in mind, it should be possible to map out the drop in BV_{DG} with V_{GS} by performing simulations to determine what value of V_{DG} is necessary to produce a given maximum electric field beneath the gate as a function of V_{GS}. Thus, Fig. 12 plots measured BV_{DG} for three current conditions, and calculated V_{DG} for three field conditions. As can be seen, the qualitative agreement is excellent.

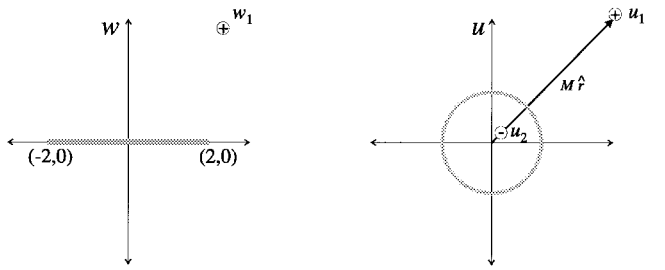

Fig. 13. Finite gate conformal transformation. The image charge necessary to create the equipotential surface is shown in the transformed coordinate system.

Clearly this effect is potentially significant both for power device design and for power circuit design. Since the impact of the source is greatest for large values of V_{DG} and small values (near V_T) of V_{GS}, it is clear that there is a tradeoff between source resistance and maximum BV_{DG} in high-power designs. In high-power HEMT's, the source must be engineered with complete understanding of its effect on the breakdown voltage. Furthermore, since many amplifier topologies require a gate voltage that swings significantly below threshold, the conventional two-terminal measurement of off-state breakdown may not be sufficient characterization for effective circuit design. Future device models should therefore reflect the impact of the source.

IV. Conclusion

We have carried out an experimental and theoretical study of the impact of the source on the breakdown behavior of high-power pHEMT's. Our findings demonstrate that contrary to the conventional two-terminal picture of off-state drain-gate breakdown, the electrostatic interaction of the source with the drain-end of the gate can have a major degrading impact on the off-state breakdown voltage of pHEMT's. We have identified a key aspect ratio, $L_G : x_D$, that explains all of our findings. The effect we report is relevant both for device modeling and for high-power device design.

Appendix
Finite Gate Conformal Transform

We wish to determine the charge distribution on a finite gate due to a single line charge. The finite gate is represented by an equipotential plane that is infinite in the z direction and that extends from $(-2, 0)$ to $(2, 0)$ in the complex plane. The transformation

$$u = \frac{w}{2} \pm \frac{\sqrt{w^2 - 4}}{2} \tag{1}$$

takes this equipotential plane in the complex plane w to a unit cylinder (i.e., a unit circle in the complex plane u—see Fig. 13). The sign of the root is determined by the sign of the imaginary part of w. The inverse transformation is

$$w = u + \frac{1}{u}. \tag{2}$$

Now, in the transformed coordinate system, the equipotential surface can be achieved by appropriate placement of equal

positive and negative line charges parallel to the z axis at

$$u_1 = M\hat{r} \tag{3}$$

and

$$u_2 = \frac{1}{M}\,\hat{r} \tag{4}$$

where $M > 1$.

The potential in the transformed coordinate system (u) corresponding to a charge located at w_1 in the w plane is thus

$$\phi[u(w), u_1(w_1)] = \frac{\lambda}{2\pi\varepsilon_0}\,\ln\left(\frac{|u-u_1|}{\left|u-\dfrac{u_1}{|u_1|^2}\right|}\right) \tag{5}$$

where λ is the magnitude of the line charge. Thus we may trivially determine the magnitude of the vertical field in the vicinity of the finite gate:

$$\mathcal{E}_y(w, w_1) = -\frac{\lambda}{2\pi\varepsilon_0}\,\mathrm{Im}\left[\frac{u_1 - \dfrac{u_1}{|u_1|^2}}{\left(u-\dfrac{u_1}{|u_1|^2}\right)(u_1-u)}\,\frac{du}{dw}\right]. \tag{6}$$

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