A New Z_{11} Impedance Technique to Extract Mobility and Sheet Carrier Concentration in HFET's and MESFET's

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***Abstract*—Conventional techniques to extract channel mobility, μ, and sheet carrier concentration, n_S, in heterostructure field-effect transistors (HFET's) do not account for the distributed nature of the device. This can result in substantial errors. To address this, we have developed a new technique that consists of measuring the gate-to-source impedance with the drain floating (Z_{11}) over a broad frequency range. A transmission line model (TL model) is fitted to $\mathrm{Re}[Z_{11}]$, thus obtaining the gate capacitance and channel resistance (and consequently $\mu(V_{\mathrm{GS}})$ and $n_S(V_{\mathrm{GS}})$) in a single measurement. We demonstrate this technique in InAlAs/InGaAs on InP HFET's. The TL model faithfully represents Z_{11} from 100 Hz to 15 MHz. Our technique can easily be automated and thus is a good tool for accurate charge control in an industrial environment.**

I. Introduction

THE design and characterization of high performance heterostructure field-effect transistors (HFET's) relies on accurate understanding of the charge control under the gate of the device. The dependence of the channel low-field electron mobility (μ) and sheet carrier concentration (n_S) on the gate-source voltage (V_{GS}) crucially shapes the operation of these transistors. Traditionally, the charge control of HFET's is determined from a combination of $I-V$ and $C-V$ measurements in specially-designed test structures [1]–[3]. In practice, this method of characterizing HFET's is inconvenient because it requires two independent measurements using different test equipment. In addition, the conventional measurement techniques ($C-V$ charge control and dc $I-V$ curves) do not consider transmission line effects (TLE) [1]–[6], which are potentially a serious source of errors, as it will be shown in this work.

In this paper, we propose a new simple technique that completely characterizes the charge control of an HFET using a single set of measurements. We denote our technique "the Z_{11} impedance measurement." For a given gate bias, the impedance seen from gate-to-source with the drain floating is measured over a broad frequency range. A transmission line model (TL model) that describes the generic distributed RC nature of the gate and the channel structure is fitted to the measurement of $\mathrm{Re}[Z_{11}]$, thus obtaining the gate capacitance and channel resistance [5], [6]. The technique relies on a single piece of equipment, a low-frequency impedance meter, and can be easily automated.

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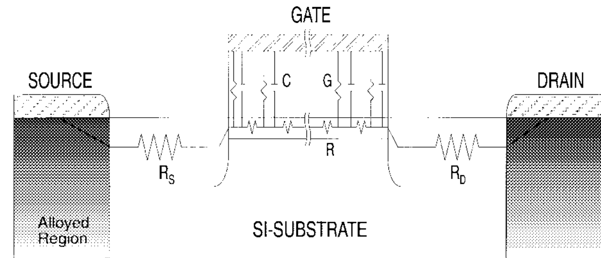

Fig. 1. Diagram of HFET showing the distributive RC network associated with the intrinsic device.

II. Theory

The theory that will be described in this section applies to field-effect transistors with "leaky" gates, such as HFET's and MESFET's. The geometry of the problem is shown in Fig. 1, which represents a generic FET biased in the linear mode of operation ($V_{\mathrm{ds}} \ll |V_{\mathrm{GS}} - V_T|$). In this regime, a very small electric field exists along the channel and the channel resistance is uniform throughout. The proper equivalent circuit representation of the intrinsic HFET is a network of series resistances and parallel conductances and capacitances, as shown in Fig. 1. The series resistance R (per unit length) characterizes the channel resistance, the parallel conductance G and capacitance C (per unit length) represent respectively the leakage and the capacitive effect between the metal gate and the conducting channel. The source and drain resistances R_S and R_D connect the intrinsic device to the outside world.

In order to extract $\mu(V_{\mathrm{GS}})$ and $n_S(V_{\mathrm{GS}})$, we need to determine the channel resistance R and the gate capacitance C as a function of V_{GS}. The proposed technique consists of applying a dc bias with a small ac signal between gate and source and measuring the resulting ac current. The drain is left floating so that there is no current through R_D nor the drain-side half of the channel, similarly to the $R_{\mathrm{gs}}(fd)$ measurement in [6]. Using a common-source two-port notation, the effective

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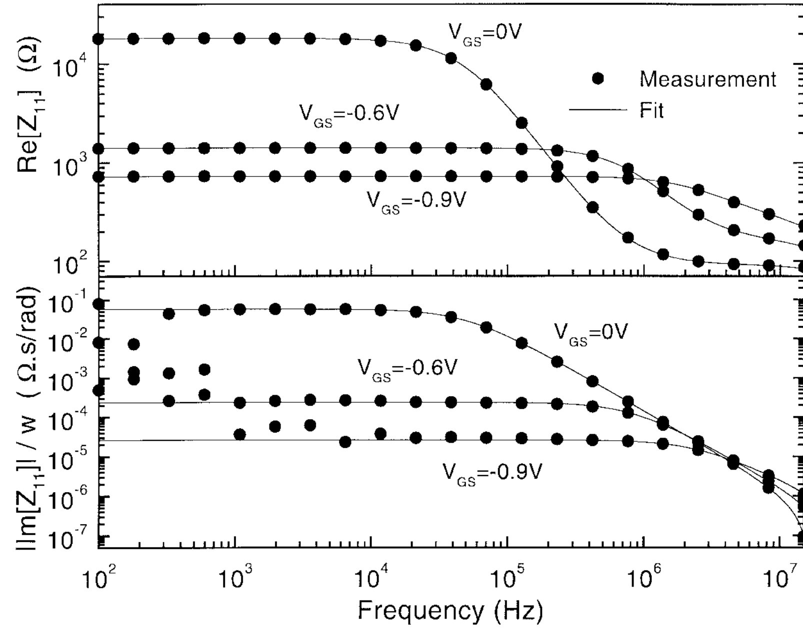

Fig. 2. Z_{11} measurement and fit as a function of frequency for three different $w_{\rm crit}$. The top graph is $\mathrm{Re}[Z_{11}]$; the bottom graph is $|\mathrm{Im}[Z_{11}]|/w$. For clarity, these graphs only plot five data points per decade of f. The fit was carried out using the full data set that consisted of 80 data points per decade of f.

measured impedance Z_{11} is

$$Z_{11} = \frac{Z_o}{\tanh(\gamma L_G)} + R_S \tag{1}$$

where Z_o is the characteristic impedance

$$Z_o = \sqrt{\frac{R}{G + jwC}} \tag{2}$$

γ the propagation constant

$$\gamma = \sqrt{R(G + jwC)} \tag{3}$$

w the angular frequency, and L_G the channel length [6].

The frequency dependence of Z_{11} in (1) can be exploited to extract the parameters of interest, R and C. In particular, a measurement of $\mathrm{Re}[Z_{11}]$ over a broad frequency range is sufficient for this purpose. There are two limits to (1). For short gate lengths, $\mathrm{Re}[Z_{11}]$ simplifies to

$$\mathrm{Re}[Z_{11}] \simeq \frac{G}{L_G(G^2 + w^2C^2)} + \frac{1}{2}RL_G + R_S \qquad L_G \ll \mathrm{Re}^{-1}[\gamma] \tag{4}$$

whereas for long gate lengths, $\mathrm{Re}[Z_{11}]$ is

$$\mathrm{Re}[Z_{11}] \simeq \frac{wC\sqrt{R}}{\sqrt{2(G^2 + w^2C^2)(\sqrt{G^2 + w^2C^2} - G)}} + R_S \qquad L_G \gg \mathrm{Re}^{-1}[\gamma]. \tag{5}$$

In the first case (4), the transistor can simply be modeled by a capacitor and a conductance in parallel with the channel resistance in series. This corresponds to a situation in which parallel conduction through the gate metal from the source to the drain is negligible. That is, TLE are small. On the other hand, (5) describes a situation in which TLE are dominant. That is, the gate barrier resistance is made negligibly small (or equivalently the channel resistance very large) and the gate metal effectively shorts the channel. TLE are not usually considered in the analysis of conventional C–V and I–V measurements.

For any given test structure at any gate bias, if we fit the real part of (1) to a $\mathrm{Re}[Z_{11}]$ measurement over a broad frequency range, the two parameters of interest R and C can be extracted in a single measurement. Repeating this procedure for different biases, we obtain R and C as a function of $V_{\rm GS}$, and consequently $n_S(V_{\rm GS})$ and $\mu(V_{\rm GS})$. The imaginary part of Z_{11}, $\mathrm{Im}[Z_{11}]$, does not provide any extra information, but can be used to reassure that the model fits well the data.

III. Experimental

As a vehicle for this study we used a InAlAs/InGaAs high electron mobility transistor (HEMT) fabricated at M.I.T. [7]. The test structure studied here is a 200 × 200 μm^2 HFET (FATFET). From TL measurements, the source resistance is estimated to be about 1 Ω.mm, which translates into R_S of about 5 Ω. The threshold voltage V_T is -1.6 V.

The Z_{11} impedance was measured with an HP-4194 Impedance-Analyzer as a function of frequency (100 Hz $\leq f \leq$ 15 MHz). The Impedance-Analyzer applies an ac signal superimposed to a dc bias and measures the corresponding small-signal impedance. It was found that probes and cables added a constant parasitic inductor term of value $L = 0.78\ \mu$H to all measurements.

At any gate bias, the real part of (1) was fitted to the $\mathrm{Re}[Z_{11}]$ measurement holding R_S and L constant. Fig. 2

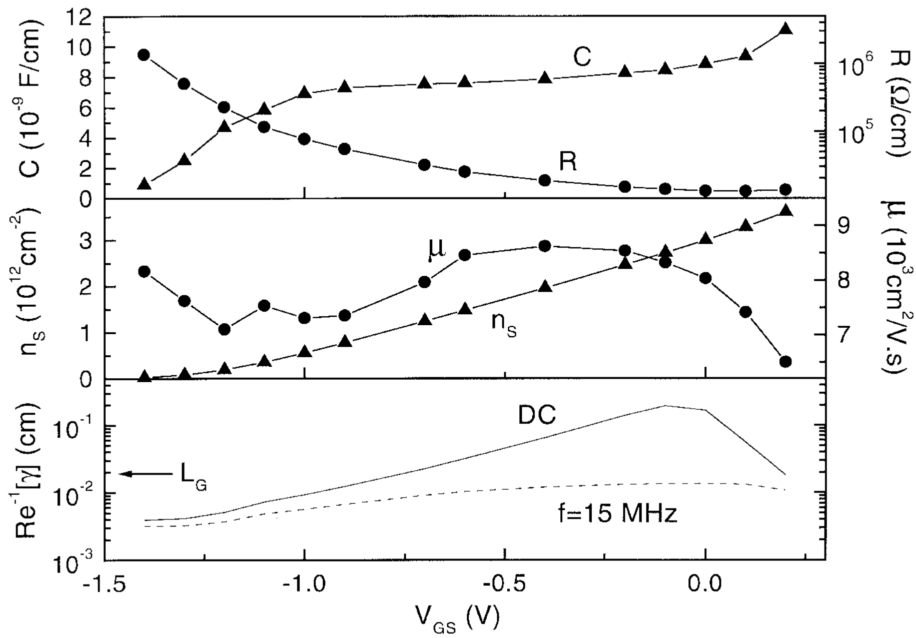

Fig. 3. Results extracted from the Z_{11} technique as a function of $V_{\rm GS}$: the top graph shows the fitted gate capacitance and channel resistance per unit length; the middle graph is a plot of the resulting sheet carrier concentration n_S and channel mobility micron; the bottom graph is a plot of $\mathrm{Re}^{-1}[\gamma]$ at dc and at $w_{\max}$.

shows the measurement and fit of Z_{11} versus frequency for three different $V_{\rm GS}$ (0, -0.6, and -0.9 V). The noise at low frequency in the bottom graph is due to the instrumentation phase shift resolution limit. As Fig. 2 shows, the model fits the measurement very well throughout the entire frequency range.

The three bias points selected in Fig. 2 correspond to different values of $\mathrm{Re}[\gamma L_G]$. In the case of $V_{\rm GS} = 0$ V, negligible TLE occur over most of the frequency range ($L_G \ll \mathrm{Re}^{-1}[\gamma]$) with a hint of TLE at the high frequency end. Note that for $w \gg G/C$, $\mathrm{Re}[Z_{11}]$ drops with a slope of -2, consistent with (4). On the other hand, for $V_{\rm GS} = -0.9$ V, $L_G \gg \mathrm{Re}^{-1}[\gamma]$ for all frequencies and thus TLE are dominant. In this case, for $w \gg G/C$, $\mathrm{Re}[Z_{11}]$ drops with a slope of $-1/2$ as depicted by (5). $V_{\rm GS} = -0.6$ V is a case in which L_G is comparable to $\mathrm{Re}^{-1}[\gamma]$. The graph shows that the Z_{11} technique can be used for any value of $\mathrm{Re}[\gamma L_G]$.

The measurement/fitting procedure was repeated for 14 different gate biases between V_T and 0.2 V. The upper limit of $V_{\rm GS}$ is set by gate leakage. For $-0.9 \leq V_{\rm GS} \leq 0.2$ V, the accuracy of the fits was within 3%. Below $V_{\rm GS} = -1$ V, the error increased: that is, for $V_{\rm GS} = -1.2$ V, the error was 20%, and for $V_{\rm GS} = -1.4$ V about 35%. The reason for this is that the pole at $w_o = G/C$ occurred at frequencies close to the maximum frequency of the instrument, $w_{\max} = 15$ MHz, and so, the high frequency behavior of $\mathrm{Re}[Z_{11}]$ was not well observed.

To overcome this inaccuracy, an additional impedance measurement was performed for $V_{\rm GS} \leq -1$ V. It consists of biasing the gate, and measuring the small signal impedance between drain and source. This corresponds to measuring $(Y_{12} + Y_{22})^{-1}$. The dc value of $(Y_{12} + Y_{22})^{-1}$ is solely given by R, G, and L_G [6]. Combining the dc value of this measurement and the one of $\mathrm{Re}[Z_{11}]$ at the same gate bias, R and G are determined within an error margin of 5%. The gate capacitance C was then extracted by fitting $\mathrm{Re}[Z_{11}]$. With this addition, the accuracy in the value of the fitted parameters is within 5% in the entire $V_{\rm GS}$ swing. This additional procedure is not needed if the instrumentation allows the frequency range to be extended to higher frequencies so that $w_{\max} \gg G/C$.

The fitted gate capacitance C and channel resistance R per unit length are plotted in the top graph of Fig. 3 as a function of $V_{\rm GS}$, and the resulting channel carrier concentration $n_S(V_{\rm GS})$ and mobility $\mu(V_{\rm GS})$ in the middle graph of Fig. 3. As it can be seen, channel mobility is roughly constant in the entire operating range of the device. The values of n_S and μ at zero gate bias are consistent with the heterostructure described previously and with Hall and charge control measurements: that is, for $V_{\rm GS} = 0$ V, the Z_{11} technique gives $\mu = 8072$ cm^2/V.s and $n_S = 2.98 \times 10^{12}$ cm^{-2}, and Hall measurements give $\mu = 8092$ cm^2/V.s and $n_S = 3.63 \times 10^{12}$ cm^{-2}. The n_S Hall value is made on a capped device. A Poisson simulation predicts that taking away the cap diminishes n_S down to $\sim 3.2 \times 10^{12}$ cm^{-2}, in which case the Z_{11} and Hall n_S values are within 7%. This simple comparison is appropriate since μ is rather independent of n_S. The inverse of the real part of the propagation constant, $\mathrm{Re}^{-1}[\gamma]$, is plotted in the bottom graph of Fig. 3. The full line is representative of TLE at dc and the dashed line at $w = w_{\max}$. As it can be seen, TLE are dominant at all frequencies for $V_{\rm GS} \leq -0.8$ V. At $w_{\max}$, we find that TLE are present at all $V_{\rm GS}$.

As a final check, we measured Z_{11} with the drain and source inverted for five bias points covering the $V_{\rm GS}$ swing. The value of the fitted parameters C, G, and R were within 6% of those obtained in the standard configuration.

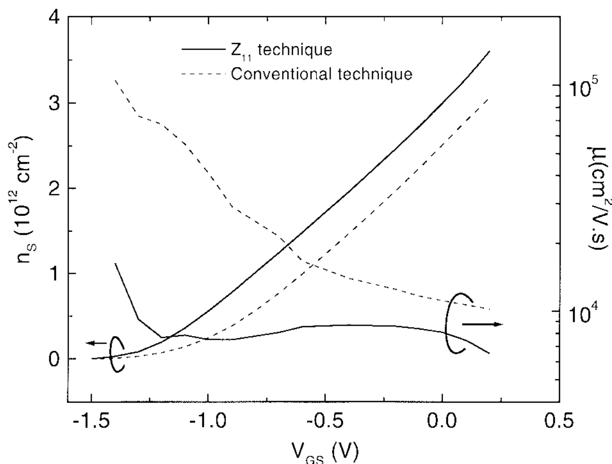

Fig. 4. Channel mobility μ and sheet carrier concentration n_S obtained for the Z_{11} technique (continuous line) and a conventional technique (dashed line) as a function of $V_{\rm GS}$. The conventional technique introduces very large errors due to transmission line effects.

IV. Discussion

We will now compare the results obtained from the Z_{11} and a widely used simple technique. We follow a procedure in which the total channel resistance, $R_{\rm chan}$, is derived from dc $I-V$ curves and the gate capacitance is obtained from $C-V$ measurements [4]. An HP-4145 parameter analyzer and an HP-4194 impedance analyzer have been used to perform the dc $I-V$ and ac $C-V$ measurements, respectively. We equated $R_{\rm chan}$ to the dc incremental output resistance, r_o, in the linear regime [1]–[3]. $C-V$ measurements were carried out with a 100 kHz ac small signal applied on top of a dc bias [3], [4]. We applied this technique to a 200 $\times$ 200 μm^2 diode lying on the same dice as the FATFET characterized as described above. We assumed a parallel model as commonly used [4].

The resulting n_S and μ obtained from each technique are plotted in Fig. 4 as a function of $V_{\rm GS}$. As it can be seen, the conventional characterization technique underestimates n_S and overestimates throughout the entire operating range of the device. Both errors arise from the fact that conventional techniques do not consider TLE. In the case of n_S, $C-V$ characterization techniques only measure a fraction of the total capacitance: for $V_{\rm GS}$ slightly above V_T, the channel resistance is large and so conduction occurs only at the periphery of the diode test structure. As a result, a lower n_S is obtained for all $V_{\rm GS}$. Similarly, when TLE are prominent, the channel resistance cannot be derived from simple $I-V$ measurements: conduction through the gate metal competes with the channel, and thus, the measured output resistance (Y_{22}^{-1}) is smaller than the channel resistance and becomes $\sqrt{\frac{R}{G}}$ which is independent of gate length [6]. As a result, μ is overestimated.

From the above discussion, conventional techniques should only be used when TLE are not prominent, that is when $L_G \ll {\rm Re}^{-1}[\gamma]$. On the other hand, the Z_{11} technique can be used as long as R, C, and G in the intrinsic device are independent of position so that the TL model is valid. Only very close to threshold, the Z_{11} technique is likely to fail. This is because of the channel debiasing that might occur due to the gate leakage current. This will have to be assessed for each individual technology.

V. Conclusion

A new simple technique to extract the channel resistance and gate capacitance in FET's, called the Z_{11} impedance measurement, has been developed. For a given gate bias, the impedance between gate and source with the drain floating is measured over a broad frequency range. A transmission line model is fitted to the measurements. The technique is applied to and the predictions of the theoretical model are confirmed in $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ HFET's. We also compared the Z_{11} technique to a conventional technique. We showed that the conventional technique leads to significant errors when the device operates under transmission line effects: channel mobility is overestimated and sheet carrier concentration underestimated for all values of $V_{\rm GS}$.

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