On-State Breakdown in Power HEMTs: Measurements and Modeling

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Abstract

A new definition of and measurement technique for on-state breakdown in high electron mobility transistors (HEMTs) is presented. The new *gate current extraction* technique is unambiguous, simple, and non-destructive. Using this technique in conjunction with sidegate and temperature-dependent measurements, we illuminate the different roles that thermionic field emission and impact ionization play in HEMT breakdown. This physical understanding allows the creation of a phenomenological model for breakdown, and demonstrates that depending on device design, either on-state or off-state breakdown can limit maximum power.

Introduction

Although great strides have been made in understanding and improving off-state breakdown (BV_{off}) in HEMTs [1-5], work on the on-state breakdown voltage (BV_{on}) has been limited due to difficulties in defining and measuring this figure of merit. Previous work has measured BV_{on} using a burnout criterion [6], which while precise, is undesirable destructive. Other workers have defined BV_{on} as a significant upturn in the drain current [7]. This definition is also frequently destructive, and also ambiguous due to the significant output conductance typically present in short gate length HEMTs. Clearly a simpler, less destructive approach is desirable.

In this work we propose a simple, unambiguous, and reproducible *gate current extraction* measurement for BV_{on}. This method, in conjunction with detailed temperature-dependent measurements and sidegate measurements, reveals the roles of impact ionization and tunneling plus thermionic field emission (TFE) in BV_{on} and BV_{off}. This allows us to develop a simple physical model for BV_{on}. We find that depending on device design, either BV_{off} or BV_{on} can limit the maximum power density of a HEMT.

A New Measurement Technique

Fig. 1 depicts the measurement technique for BV_{on}. I_G is held constant at a desired value (a typical condition is 1 mA/mm), and I_D is ramped from I_G to some reasonable value (typically 20% to 40% of I_{Dmax}). This measurement traces a locus of V_{DS} versus I_D for constant I_G (Fig. 1); we define this locus as BV_{on}. This definition is sensible in several respects: (1) it ramps from BV_{off} which is usually defined as $I_G = I_D = 1$ mA/mm; (2) it defines a locus of significant gate conductance; (3) as seen below, it measures a locus of constant impact ionization, which has been associated with burnout [6].

The technique is illustrated on a state-of-the-art 0.1 μm InAlAs/InGaAs HEMT [1] in Fig. 2, where BV_{on} loci for several values of I_G are superimposed on the output characteristics. As the device is turned on, BV_{on} first drops from 4.2 V (BV_{off}) to less than 2.5 V, and then saturates.

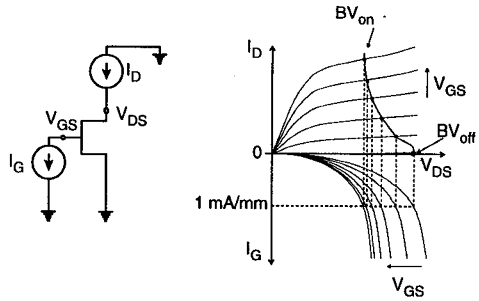

Figure 1: Gate current extraction technique for measuring BV_{on}. A constant current (typically 1 mA/mm) is extracted from the gate while I_D is swept from the off-state (1 mA/mm) to the on state. The technique traces a breakdown locus of V_{DS} versus I_D.

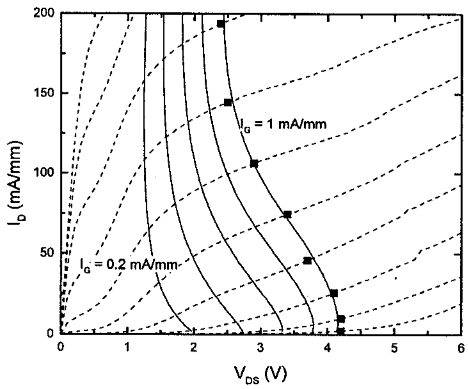

Figure 2: BV_{on} versus I_D for 0.1 μm InAlAs/InGaAs HEMT for different values of I_G. The data are superimposed on the output characteristics. As an independent verification of the technique, the points on the output characteristics at which $I_G = 1$ mA/mm are plotted as well. The constant I_G criteria additionally tracks the sudden rise of drain conductance often associated with BV_{on}.

Examining the output characteristics, we see that for $V_{DS} > BV_{on}$, the drain conductance begins to rise, indicating that the device is approaching a dangerous region. Such an interpretation is strongly supported by statistical burnout measurements. In Fig. 3, we present the results of such measurements on one wafer. As can be seen, the locus of burnout is fairly well predicted by the BV_{on} locus. Furthermore, our results strengthen Rohdin's suggestion that the burnout mechanism is not a constant power mechanism, but a constant impact ionization mechanism [6]. This is confirmed by measurements on several wafers that suggest that in the on state, burnout occurs at an approximately constant gate current *regardless of*

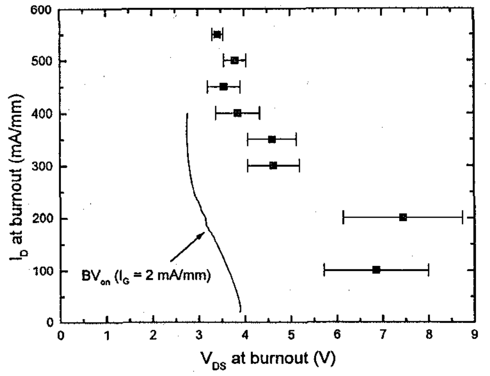

Figure 3: Comparison of BV_{on} and burnout voltages for an InAlAs/InGaAs HEMT ($L_G = 1\ \mu m$). The gate current extraction technique predicts the unsafe bias region fairly well.

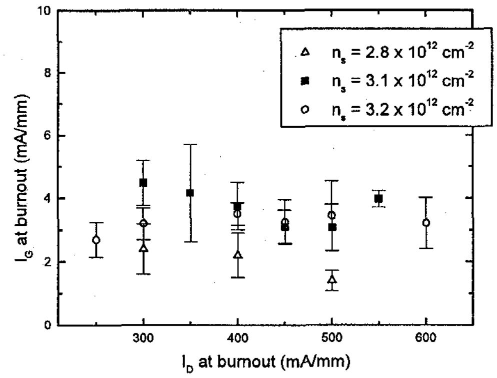

Figure 4: Measured gate current at burnout as a function of drain current for several different InAlAs/InGaAs HEMTs. For all three wafers, burnout in the on-state occurs at around $I_G = 2.5 \pm 1$ mA/mm regardless of I_D.

I_D (Fig. 4). Thus, a constant gate current criteria is reasonable for predicting the burnout locus.

On-state Breakdown Physics

Fig. 5 presents a simple picture of the physics of BV_{on} which is consistent with these measurements and previous results. In the off-state, I_G is almost purely TFE [1,5]. However, as I_D rises, impact ionization starts to generate holes which escape to the gate [10]. To maintain constant I_G, V_{DG} must drop, and so does V_{DS} . Once the device is fully on, BV_{on} becomes more vertical, due to the exponential dependence of impact ionization on field and the diminished role of TFE. Such a picture should apply to most power HEMT structures.

In order to explore these physics, we have compared BV_{on} in a high- performance AlGaAs/InGaAs pHEMT ($L_G = 0.1\ \mu m$) [8] with BV_{on} in the InAlAs/InGaAs HEMT (Fig. 6). Both devices show similar characteristics, suggesting that similar mechanisms are at play: BV_{on} drops as the device is turned on, and then becomes fairly constant at higher values of I_D.

We have performed temperature-dependent measurements of BV_{on} and BV_{off} to help identify the dominant physical mechanisms (Fig. 7). BV_{off} in both types of

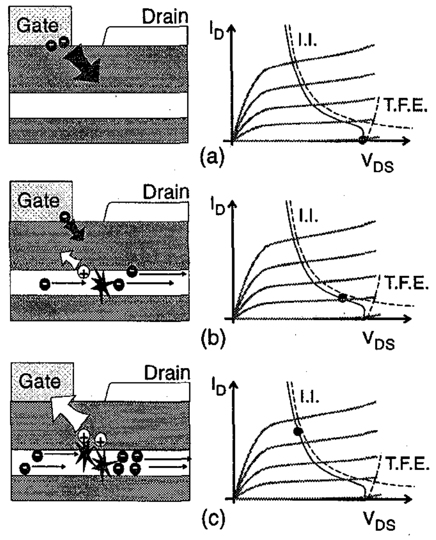

Figure 5: Physical mechanisms for breakdown. (a) Close to threshold, I_G is almost purely tunneling and thermionic field emission. (b) and (c) As the device is turned, impact ionization in the channel produces holes, which escape to the gate. In order to support a constant I_G, V_{DG} and V_{DS} must drop.

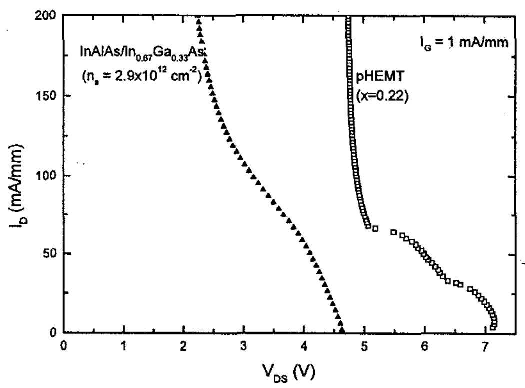

Figure 6: BV_{on} for an InAlAs/$In_{0.67}Ga_{0.33}As$ HEMT and an AlGaAs/InGaAs pHEMT at $I_G = 1$ mA/mm. Both devices show a significant drop in breakdown as I_D is increased.

HEMTs exhibits a negative temperature coefficient, consistent with TFE. However, BV_{on} in the pHEMT exhibits a small but significant (50 mV) rise as temperature is increased. The transition from a negative to a positive temperature coefficient is a clear signature of a transition from TFE to impact ionization.

In contrast, the temperature dependence of BV_{on} for the InAlAs/InGaAs HEMT is negative. This is consistent with the recent demonstration of a negative temperature coefficient for impact ionization in this material system [9]; however, it makes identification of the physical mechanism more challenging.

In order to distinguish TFE from impact ionization in the InAlAs/InGaAs HEMT, we have directly monitored hole generation through a sidegate [10] while the locus of BV_{on} is traced (Fig. 8). When the device is off, the sidegate current is minimal and independent of I_G, indicating that in the off-state TFE dominates breakdown. However, as I_D is increased, the sidegate current first rises

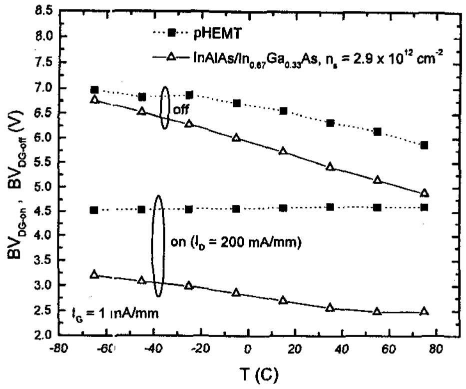

Figure 7: Temperature dependence of BV_{off} ($I_G = I_D =$ 1mA/mm) and BV_{on} (I_D = 200 mA/mm, I_G = 1mA/mm) in an AlGaAs/InGaAs pHEMT and a strained channel InAlAs/InGaAs HEMT.

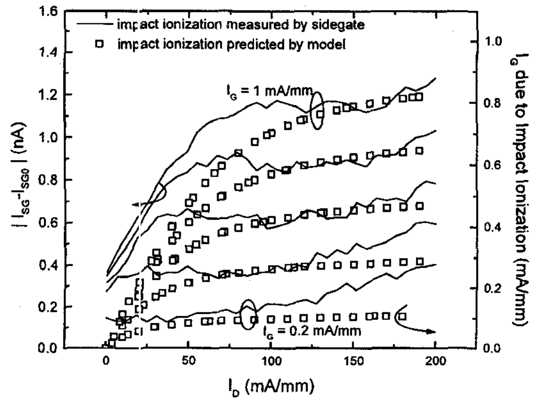

Figure 8: Sidegate current measured during on-state breakdown measurement (V_{SG} = -50 V). The rise and saturation of I_{SG} demonstrate the transition from the TFE dominated off-state to the II-dominated on-state. Also plotted are the simple model's predictions for impact ionization current.

as impact ionization turns on, and then saturates for I_D > 80 mA/mm. Furthermore, the saturated sidegate current scales with I_G. This indicates that the gate's hole collection efficiency does not depend much on I_G or I_D, and that for sufficiently high values of I_D, a constant I_G criteria corresponds to constant impact ionization.

On-state BV Model

Our simple picture of BV_{on} leads to a phenomenological model that can assist device and circuit designers. For a given bias condition, I_G is determined by the fraction of the holes generated by impact ionization that are extracted by the gate, and by the number of electrons which escape from the gate due to TFE and tunneling:

$$I_G = I_{TFE} + I_{ii} \tag{1}$$

We have previously shown that TFE depends mainly on the extrinsic sheet carrier concentration, the gate Schottky barrier height, and V_{DG} [1,5]. Proper calculation of the impact ionization current requires precise knowledge of the fields in the channel and of the ionization rate. It is possible, however, to simplify the problem using the

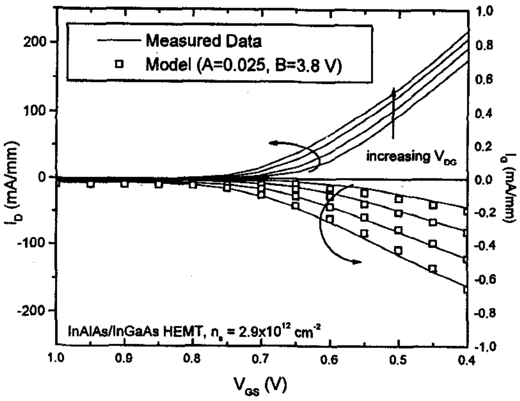

Figure 9: Comparison of measured and modeled gate current characteristics for InAlAs/InGaAs HEMT.

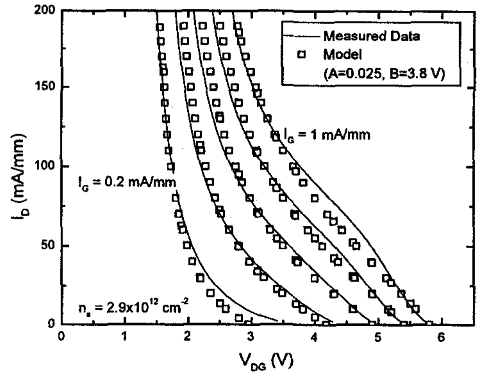

Figure 10: Comparison of measured and modeled breakdown contours of an InAlAs/InGaAs HEMT for different I_G criteria.

experimentally verified expression [10]:

$$I_{ii} = AI_D \exp(\frac{-B}{V_{DS} - V_{DS(sat)}}) \tag{2}$$

B can be determined from sidegate measurements; A is a scaling constant that depends on device design.

Using this model, it is possible to predict accurately the I_G characteristics (Fig. 9) and the evolution of the BV_{on} loci (Fig. 10). Impressively, the model also does a good job of predicting the amount of impact ionization measured by the sidegate (Fig. 8). This is an excellent indication that the model is effectively capturing the physics of on-state breakdown.

To explore the impact of design parameters on BV_{on}, we have measured a sample set of 0.1 μm InAlAs/InGaAs HEMTs with varying values of extrinsic sheet carrier concentrations (n_s) (Fig. 11) [1]. The model works well for all three devices. Interestingly, increasing n_s results in much more vertical BV_{on} contours. It is striking that three devices with such different BV_{off} values (1.9 V to 4.7 V) approach similar BV_{on} values (1.2 V to 1.7 V at 200 mA/mm). Our model explains this behavior: in the higher n_s devices, BV_{off} is low; thus the field in the channel is lower, and the device moves more slowly into impact ionization. As a result, BV_{on} only degrades slightly. This view is supported by the model and by sidegate measurements on the higher n_s devices (Fig. 12), which show that these HEMTs move gradually into impact ionization.

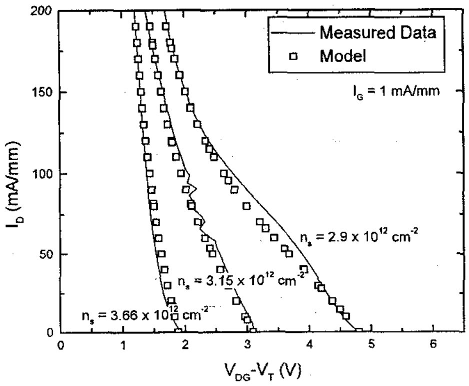

Figure 11: Comparison of measured and modeled breakdown contours for three different InAlAs/InGaAs HEMTs at I_G = 1 mA/mm.

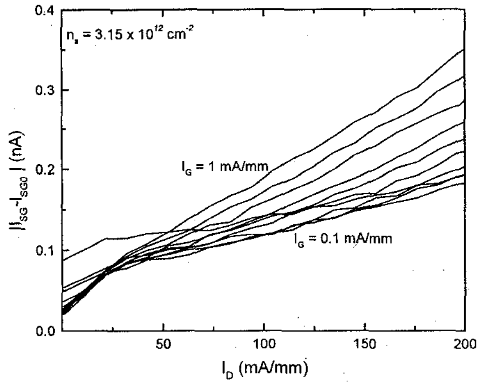

Figure 12: Sidegate current for InAlAs/InGaAs HEMT with higher n_s. The fact that the sidegate current does not saturate indicates the relative importance of TFE up to high values of I_D.

The devices' similarity in BV_{on} seems to suggest that improvements in BV_{off} are not very meaningful from a power point of view. However, examination of allowable load lines on each device (Fig. 13) makes it clear that the *shape* of the BV_{on} locus, which depends strongly on BV_{off}, is crucial to a device's power potential, as has been previously noted in MESFETs [11].

Conclusions

In summary, we have presented an unambiguous definition and a simple, non-destructive measurement for BV_{on} in HEMTs. This has allowed us to achieve physical understanding of BV_{on}. Both BV_{off} and BV_{on} must be considered when designing a power device.

Acknowledgments

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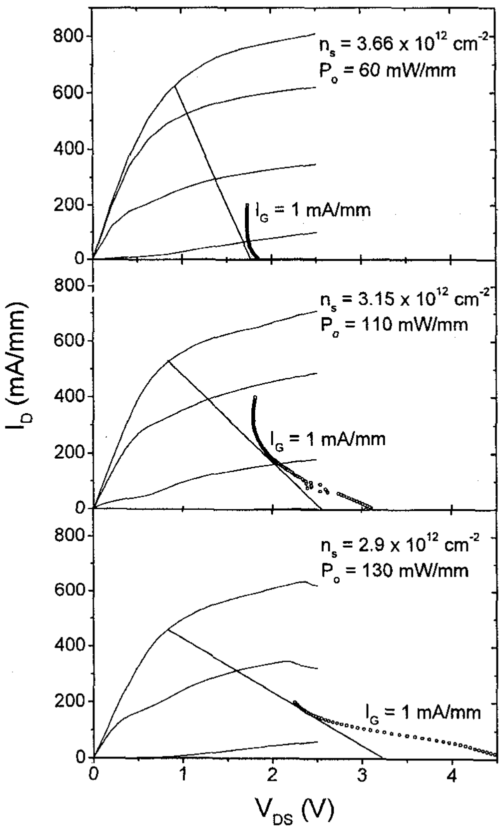

Figure 13: Comparison of power load lines for three 0.1 μm InAlAs/InGaAs HEMTs. Due to the shape of BV_{on}, it is possible to bias the low n_s device for greater power output.

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