# Impact Ionization and Transport in the InAlAs/n$^+$-InP HFET

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*Abstract*—**We have carried out an experimental study exploring both impact ionization and electron transport in InAlAs/n$^+$-InP HFET's. Our devices show no signature of impact ionization in the gate current, which remains below 17 $\mu$A/mm under typical bias conditions for $L_g = 0.8\,\mu$m devices (60 times lower than for InAlAs/InGaAs HEMT's). The lack of impact ionization results in a drain-source breakdown voltage ($BV_{DS}$) that *increases* as the device is turned on, displaying an off-state value of 10 V. Additionally, we find that the channel electron velocity approaches the InP saturation velocity of about $10^7$ cm/s (in devices with $L_g < 1.6\,\mu$m) rather than reaching the material's peak velocity. We attribute this to the impact of channel doping both on the steady-state peak velocity and on the conditions necessary for velocity overshoot to take place. Our findings suggest that the InP-channel HFET benefits from channel electrons which remain cold even at large $V_{GS}$ and $V_{DS}$ making the device well-suited to power applications demanding small $I_G$, low $g_d$, and high $BV_{DS}$.**

## I. Introduction

THERE is a rapidly growing interest in an electronics family based on InP, fueled both by the possibility of integration with long-wavelength optical devices and by the excellent performance potential of InAlAs/InGaAs Heterostructure Field-Effect Transistors (HFET's) at millimeter-wave frequencies. Many specific applications for an InP-based integrated circuit technology, including laser drivers and photodiode receivers for optical communications systems and microwave amplifiers for wireless systems, demand high-speed devices capable of handling large currents and voltages. Photodiode receivers additionally require very low gate current ($I_G$) to avoid degrading sensitivity through the introduction of $I_G$-related input noise [1].

Despite the high-frequency merits of the InAlAs/InGaAs HFET [2], the devices are quite vulnerable to impact ionization in the narrow-bandgap channel, even under normal biasing conditions [3]. In addition to lowering the drain-source breakdown voltage ($BV_{DS}$), this phenomenon degrades voltage gain ($a_v$) through increased output conductance ($g_d$), and generates excess $I_G$ from escaping holes [3]–[6]. Several studies have explored techniques for reducing impact ionization in these devices, including engineering the cap layer over the drain-gate gap to lower the peak drain electric field [7] and employing a pseudomorphic gate barrier layer to reduce thermionic field emission of gate electrons into the channel which can produce impact ionization [4]. Others have focused on methods for reducing the consequences of impact ionization, including inserting an additional pseudomorphic layer between gate and channel to block multiplication holes and thus lower excess $I_G$ [8], [9]. The success of these methods and their associated performance tradeoffs are still unclear, however.

The InAlAs/InP system offers a promising alternate approach for HFET's targeted at high-power and low input-noise telecommunications applications. In an InAlAs/InP HFET, InP is employed as an *active* layer, rather than merely as a *mechanical* substrate, offering several distinct advantages compared with InGaAs. Electronically, the wide bandgap material enjoys an exceptional breakdown field, making it potentially resistant to impact ionization. In addition, although InP has a smaller mobility at low electric fields, it shows a higher peak electron velocity ($v_e$) which persists over the electric field range (5–50 kV/cm) most relevant to modern, submicrometer devices [10]. Some of the benefits of these material properties have been observed in both doped-channel [11] and modulation-doped [12] InP-channel HFET's which have recently demonstrated an excellent combination of high transconductance ($g_m$), current density, power density, and breakdown voltage. Additionally, highly selective chemical etchants exist for InGaAs and InAlAs over InP. This property makes InP an ideal *etch-stop* layer, for example, enabling a device to achieve the benefits of a recessed-n$^+$-InGaAs-cap design while maintaining a very tight threshold voltage ($V_T$) distribution [11].

To date, however, there has been little work assessing the InAlAs/InP HFET so as to allow a judicious comparison with competing HFET designs on InP. Such a comparison must address two distinct areas, corresponding to the two key electronic properties of InP. First, it must look at impact ionization, focusing on its effects on $I_G$, $g_d$, and $BV_{DS}$. This is an area in which InP-channel HFET's should hold an advantage over InGaAs-based devices. Second, it must explore the behavior of the device's electron transport char-

Manuscript received July 6, 1994; revised February 22, 1995. The review of this paper was arranged by Associate Editor P. K. Bhattacharya. This work was supported under Grants DL-H-441694 and DL-H-441638 from C.S. Draper Laboratory, grant DAAL03-92C0001 from the Joint Services Electronics Program, as well as through equipment grants from Bellcore and Hewlett Packard. In addition, DRG received personal fellowship support from the Fannie and John Hertz Foundation and from the Intel Foundation.

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IEEE Log Number 9413276.

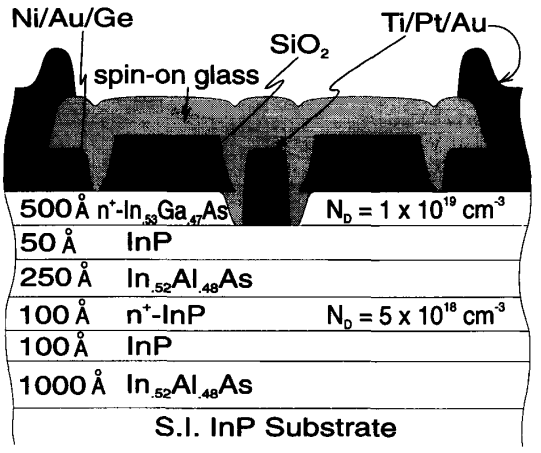


Fig. 1. Schematic cross section of the InAlAs/n$^+$-InP HFET.

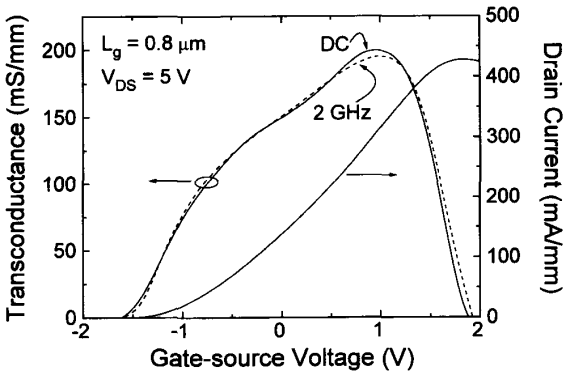


Fig. 2. $g_m$ versus $V_{GS}$ (at both dc and 2 GHz) and $I_D$ versus $V_{GS}$ for an $L_g = 0.8\,\mu$m device ($V_{DS}$ =5 V).

acteristics and frequency response as gate length is scaled down, an area in which InGaAs-channel devices should enjoy an advantage. Understanding these issues will allow device designers to choose the optimal heterostructure for a given application.

This experimental work studies in detail both of these issues and their effects on performance in submicron InP-channel HFET's, first considering impact ionization and subsequently examining the physics of transport, using the InAlAs/n$^+$-InP Metal-Insulator-Doped-Channel FET (MIDFET) as a vehicle. Featuring an undoped InAlAs insulator and thin, heavily-doped InP channel, the MIDFET has been shown to achieve high drain-current ($I_D$) linearity over a broad gate-source voltage ($V_{GS}$) swing, broad plateaus in $f_T$ and $f_{\max}$, large breakdown voltage, and low-frequency dispersion in transconductance ($g_m$) [13]–[16]. These features are well-suited to a variety of modern telecommunications applications. Our study finds that the wide-bandgap InP channel eliminates discernible impact ionization at any bias point (including at breakdown), resulting in low $I_G$ combined with high $BV_{DS}$ and low $g_d$. On the other hand, we find that the effective electron velocity ($v_e^{eff}$) in the n$^+$-InP channel approaches the material's saturation velocity ($v_{sat} \simeq 1 \times 10^7$ cm/s) rather than the larger peak velocity. This is attributed to the impact of doping. In context with the reported performance of other HFET designs on InP, our findings suggest that the InAlAs/n$^+$-InP HFET is well-suited to power applications demanding small $I_G$, low $g_d$, and high $BV_{DS}$ and accepting the tradeoff of moderate frequency response.

## II. Experiment

The devices used in this study were fabricated using the MOCVD-grown heterostructure shown in Fig. 1. The heterostructure consists, from top to bottom, of a 500 Å $In_{0.53}Ga_{0.47}As$ cap ($N_D = 1 \times 10^{19}\,cm^{-3}$), a 50 Å undoped InP etch-stop layer, a 250 Å undoped $In_{0.52}Al_{0.48}As$ gate barrier, a 100 Å n$^+$-InP channel ($N_D = 5 \times 10^{18}\,cm^{-3}$), a 100 Å undoped InP subchannel, and a 1000 Å undoped $In_{0.52}Al_{0.48}As$ buffer/electron-confinement layer grown on a (100) semi-insulating InP substrate.

Fabrication begins with a mesa wet etch, followed by PECVD deposition of a 3000 Å $SiO_2$ layer. This layer is later wet-etched in buffered oxide etch after both the ohmic contact and gate level photolithography steps to leave a photoresist overhang for reliable, high-yield lift-off. Next, Ni/Au/Ge ohmic contacts are deposited, patterned, and RTA annealed at 375°C for 10 s. Following gate photolithography, the n$^+$-InGaAs cap is selectively etched down to the InP etch-stop layer with 1:10:220 $H_2SO_4$:$H_2O_2$:$H_2O$ etchant just prior to the deposition and lift-off of Ti/Pt/Au gates. Precise timing of the etch or iterative monitoring of $I_D$ is obviated by the better than 300:1 selectivity of this etchant for InGaAs on InP. The resulting increased reliability and $V_T$ control are essential for circuit fabrication. Finally, we conclude fabrication with spin-on glass intermetal dielectric coating (cured at 200°C, 30 m) and via-hole etching followed by Ti/Pt/Au pad/second-level metal formation.

Our mask set includes an array of $\pi$-gate devices for on-wafer microwave probing with $W_g = 200\,\mu$m and $L_g$ ranging from 0.8–2 $\mu$m. The gate-source and gate-drain spacings ($L_{gs}$ and $L_{gd}$) are each equal to 2 $\mu$m for all devices. A dummy microwave device without mesa is included adjacent to the working HFET's for measuring the parasitic probe pad capacitances. To supplement our scaling study, we have also looked in detail at longer $L_g$ devices (1.7 $\mu$m to 5.7 $\mu$m) from results reported in [11].

## III. Results and Discussion

### A. General Results

Fig. 2 shows $g_m$ versus $V_{GS}$ (at both dc and 2 GHz) and $I_D$ versus $V_{GS}$ at $V_{DS} = 5$ V for an $L_g = 0.8\,\mu$m device. We note that $g_m$ rises linearly as $V_{GS}$ is increased from threshold, peaking at about 200 mS/mm and then falling off rapidly due to the onset of strong gate leakage at about $V_{GS} = 1$ V. The thin, heavily doped channel and undoped gate barrier contribute to little frequency dispersion in $g_m$ between dc and 2 GHz and to a typical maximum drain current ($I_{D,MAX}$)

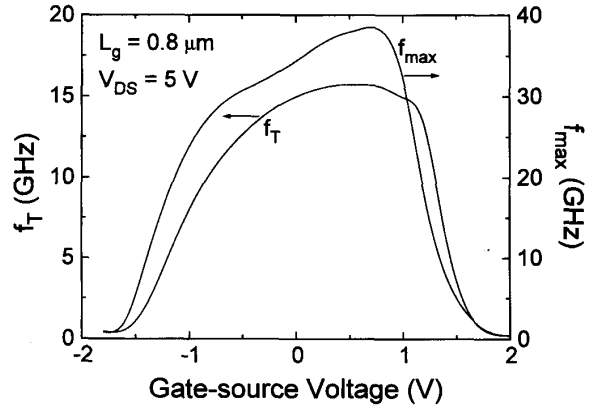


Fig. 3. $f_T$ and $f_{\max}$ versus $V_{GS}$ for an $L_g = 0.8\,\mu$m device ($V_{DS} = 5$ V).

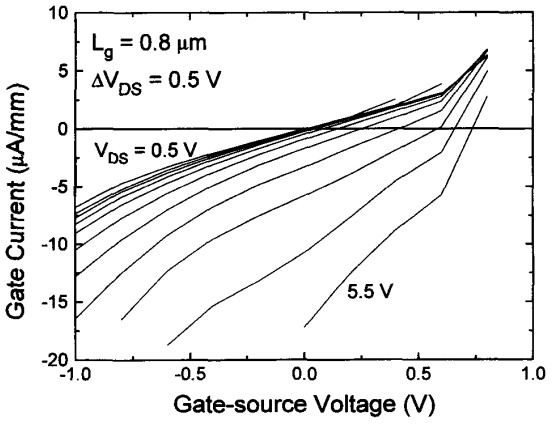


Fig. 4. $I_G$ versus $V_{GS}$ for an $L_g = 0.8\,\mu$m device ($V_{DS} = 0.5$–5.5 V).

of 430 mA/mm. We also observe a kink or slope change (at $V_{GS} = -0.8$ V in this device), corresponding to about $I_D = 100$ mA/mm in devices of all gate lengths. We shall later find that this kink directly relates to the nonlinearity of the small-signal source resistance ($r_s$) in these devices, making it necessary to correct for $r_s$ prior to drawing any physical understanding of electron transport from this data.

Fig. 3 shows the behavior of $f_T$ and $f_{max}$ versus $V_{GS}$ for the same device. Peak values are 15 GHz and 38 GHz, respectively. As with $g_m$, $f_T$ rises linearly with $V_{GS}$ just above threshold, but then flattens into a broad plateau before eventually falling off. We will later examine the scaling of the channel electron velocity with gate length and find that the $f_T$ plateau stems from a velocity saturation condition in the channel.

### *B. Impact Ionization Study*

The wide-bandgap InP channel is expected to reduce impact ionization in the InAlAs/InP HFET, resulting in lower $I_G$, improved $BV_{DS}$, and reduced $g_d$. Examining the behavior of $I_G$ versus $V_{GS}$ is key to assessing the role of impact ionization in an HFET [17], [18]. As $V_{GS}$ is increased from threshold in an HFET employing a narrow-bandgap channel such as InGaAs, electrons exiting the drain end of the channel may eventually possess sufficient energy to generate an electron-hole pair. A significant quantity of holes may be created in this way as the generated carriers are themselves accelerated by the high electric field near the drain and continue the impact ionization process. These ionized holes travel through the channel toward the source, with most easily escaping over the gate barrier and creating a large signature "hump" in $I_G$ versus $V_{GS}$ [8], [9], [19], [20].

To look for this signature in our devices, we plot $I_G$ versus $V_{GS}$ for several values of $V_{DS}$ for a typical $L_g = 0.8\,\mu$m device in Fig. 4. Significantly, the curves are completely free of the characteristic impact ionization hump at all measured $V_{DS}$ despite the type II band alignment of the InAlAs/InP system (i.e., negative channel-to-barrier $\Delta E_v$), strongly indicating that the devices are completely free of this deleterious effect.

A major benefit of this absence of ionized hole current is a low $I_G$ compared with values in InGaAs-channel devices. We find that $|I_G|$ remains less than 17 $\mu A$/mm over the $V_{GS}$ range of useful $g_m$ between $-1$ V and 1 V, at a typical $V_{DS}$ of 4 V. This value is up to 60 times lower than for reported lattice-matched InGaAs HEMT's operated at a lower $V_{DS}$ of 2 V (including devices with channel edge isolation) [8], [9], [19]. A low $I_G$ is essential for high-sensitivity optoelectronic receiver applications.

As a further result of negligible impact ionization combined with the excellent electron confinement of the thin MIDFET channel, our devices display very low $g_d$ and thus good values for $a_v$ despite only modest values for $g_m$. At 2 GHz and $V_{DS} = 5$ V, for example, $g_d$ remains below 5 mS/mm over a $V_{GS}$ swing of 2 V. We find that $g_d$ rises with $V_{GS}$ at a rate similar to $g_m$, leading to a broad plateau in $a_v$ centered around a value of 33.

The lack of impact ionization in our devices also leads to excellent breakdown voltage characteristics. Since impact ionization in an HFET is initiated by high-energy electrons moving through the drain end of the channel, the phenomenon becomes more pronounced with increasing $I_D$. Consequently, $BV_{DS}$ in such a device degrades from its off-state value as the device is turned on, the behavior observed in InAlAs/InGaAs HFET's [21]. This is quite different from what happens in our devices, as illustrated in Fig. 5 showing $I_D$ versus $V_{DS}$ for an $L_g = 0.8\,\mu$m device with $V_{GS}$ varied from just below to moderately above threshold. Rather than degrading with increasing $I_D$, we find that $BV_{DS}$ in our devices actually *increases* as the device is turned on, confirming that breakdown is not limited by impact ionization in the channel. The number of traces presented in this figure is limited by the high probability of device destruction each time the device is stressed beyond breakdown.

To explore the breakdown mechanism further, we plot $V_{DS}$, $V_{DG}$, and $I_G$ versus $V_{GS}$ for the same device in Fig. 6, using the Drain-Current Injection technique described in [22] with $I_D = 1$ mA/mm. We measure an excellent off-state $BV_{DS}$ and $BV_{DG}$ values of 10 V and 12 V, respectively. We also

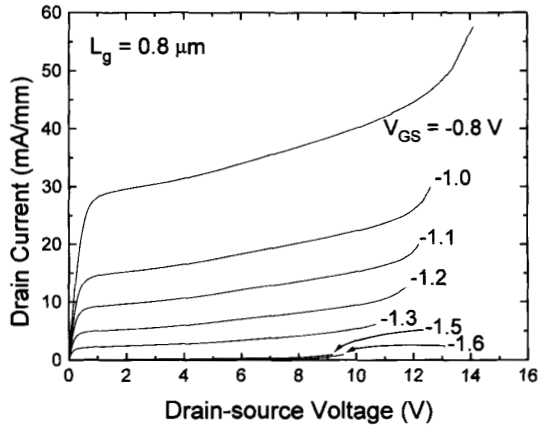


Fig. 5. $I_D$ versus $V_{DS}$ for an $L_g = 0.8\,\mu$m device showing $I_D$-dependence of drain-source breakdown above threshold.

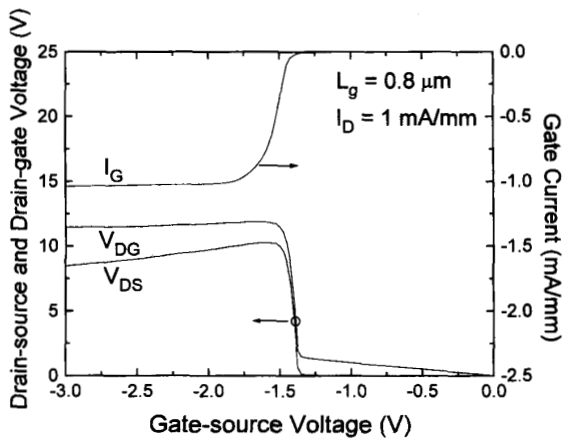


Fig. 6. $V_{DS}$, $V_{DG}$, and $I_G$ versus $V_{GS}$ at $I_D = 1$ mA/mm for an $L_g = 0.8\,\mu$m device.

note that breakdown in our device occurs at constant $V_{DG}$ regardless of $V_{GS}$, with all injected drain current emerging from the gate. This behavior, which does not depend on $L_g$ in the examined range, confirms that breakdown occurs through a *gate-drain* mechanism, such as the tunneling of electrons between the $n^+$-$In_{0.53}Ga_{0.47}As$ cap and gate metal through the gate barrier.

Our results indicate that the InP-channel HFET holds an advantage over InGaAs-channel designs for applications emphasizing small $I_G$, low $g_d$, and high $BV_{DS}$. Indeed, our findings point to considerable room to improve these figures of merit still further, through well-known methods such as the use of a pseudomorphic, AlAs-rich gate barrier layer [16] as well as the use of a double-recessed cap structure [23].

### C. Channel Transport

Although InP has a lower mobility compared with InGaAs, the effective electron velocity ($v_e^{eff}$) in the InAlAs/InP HFET channel may benefit from the material's potentially greater

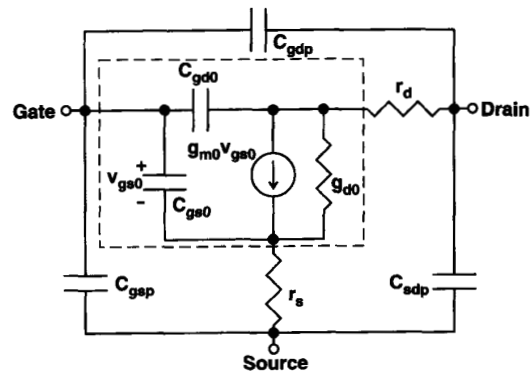


Fig. 7. Small-signal equivalent circuit model for an HFET, including parasitic source and drain resistances and pad capacitances.

$v_e$ at medium to high electric fields. Any comparison of the InAlAs/InP HFET against InGaAs-channel designs should therefore explore the transition from the mobility-limited to the velocity-saturation-limited transport regimes by examining the scaling of $v_e^{eff}$ over devices with various $L_g$ [15].

Our approach to extracting $v_e^{eff}$ in this study is based on the small-signal equivalent circuit for an HFET shown in Fig. 7, which models the device up through and including the probe pads. The portion of the circuit enclosed by the dashed line represents the intrinsic device beneath the gate metal and is thus directly related to the transport physics of the HFET. In the velocity-saturation regime of operation, for example, one can define the effective electron velocity $v_e^{eff}$ in the channel from the intrinsic transconductance $g_{m0}$ through

$$v_e^{eff} \equiv \frac{L_g}{\tau_t} = \frac{g_{m0}L_g}{C_{gs0}} \tag{1}$$

where $C_{gs0}$ is the gate-source capacitance defined in Fig. 7 and $\tau_t$ is the electron transit time from source to drain. The values of $g_{m0}$ and $C_{gs0}$ may themselves be easily extracted from the y-parameters of the intrinsic equivalent circuit, according to

$$g_{m0} = \Re e[y_{21}] \tag{2}$$

$$C_{gs0} = \frac{\Im m[y_{11} + y_{12}]}{\omega}. \tag{3}$$

We have characterized our devices over the frequency range from 0.5–40 GHz, finding that the model in Fig. 7 holds quite well up to about 10 GHz (before smaller, unaccounted circuit elements become important). We have thus performed all our extractions at 2 GHz. This procedure is more accurate than methods which estimate $v_e^{eff}$ through $f_T$, since $f_T$ is degraded through $C_{gd0}$, $g_{d0}$, $r_s$, and $r_d$, yielding a value somewhat lower than the true channel velocity [24].

The $y$-parameters for the intrinsic device are de-embedded from the measured $s$-parameters in two stages. First, we convert the $s$-parameters to $y$-parameters and subtract out the impact of the probe pads, modeled by parasitic capacitances

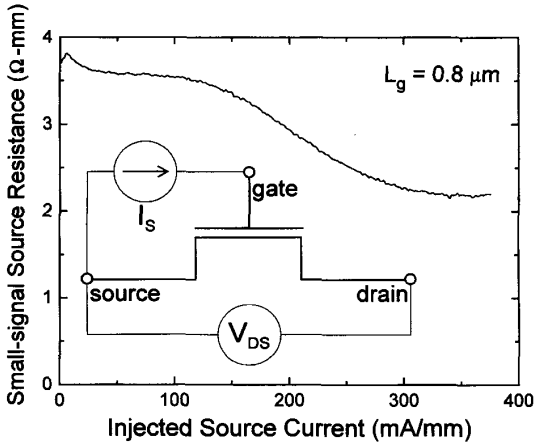


Fig. 8. $r_s$ versus $I_S$ for an $L_g = 0.8\,\mu$m HFET ($L_{gs} = 2\,\mu$m), measured using the current-injection technique illustrated in the inset.

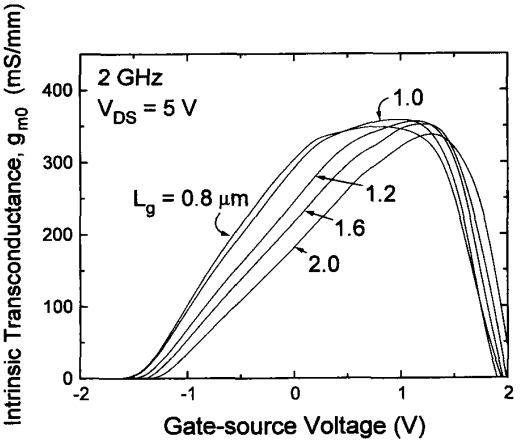


Fig. 9. Extracted $g_{m0}$ versus $V_{GS}$ for various $L_g$ ($V_{DS} = 5$ V).

$C_{gsp}$, $C_{gdp}$, and $C_{sdp}$. Minor pad inductances are not included in our model, since they may be ignored in the measured frequency range. The second stage corrects for the parasitic source and drain resistances, which are subtracted out after converting to the $z$-parameter domain. Converting back to $y$-parameters yields the desired intrinsic model.

We extract the parasitic pad capacitance needed in this correction process using a dedicated test structure located near the devices of interest. This test structure has an almost identical layout to that of a working HFET, but lacks the mesa containing the active heterostructure layers.

Determining $r_s$ and $r_d$ is somewhat more involved because these values may vary from device to device and are, in our device structure, dependent on $I_S$ and $I_D$, respectively [11]. While Dambrine *et al.*, have illustrated a technique by which these resistances may be extracted directly from the $y$-parameters with the device biased at $V_{DS} = 0$ V [25], the method has a drawback in that it extracts $r_s$ and $r_d$ only at one bias point with no current flowing.

We therefore use a current-injection technique to directly profile $r_s$ versus $I_S$ and $r_d$ versus $I_D$ on each device (see inset in Fig. 8) [15]. For $r_s$, we measure $V_{DS}$ as current $I_S$ is injected from gate to source with the drain floating. This measured $V_{DS}$ consists of two potential drops: the one of interest resulting from the parasitic source resistance, and the drop across a portion of the channel near the source through which $I_S$ passes before exiting out the gate. Except at very small currents, however, $I_S$ crowds quite close to the source end of the gate metal and falls off exponentially toward the drain, so that the desired parasitic-source ohmic drop dominates over almost the entire $V_{DS}$ versus $I_S$ sweep. Finally, the derivative $dV_{DS}/dI_S$ yields $r_s$. We extract $r_d$ in the same manner.

Fig. 8 shows $r_s$ versus $I_S$ for a typical $L_g = 0.8\,\mu$m device ($L_{gs} = 2\,\mu$m). We indeed find that $r_s$ is dependent on $I_S$. For $I_S$ below 100 mA/mm, $r_s$ is constant at about 3.5 $\Omega \cdot$ mm . Through a detailed study using several test structures [32], we find that this value consists of 2.3 $\Omega \cdot$ mm due to the contact resistance to the channel layer and 1.2 $\Omega \cdot$ mm due to the 600 $\Omega/\square$ channel sheet resistance. At higher currents, however the potential drop in the source-gate gap is sufficient to turn on the cap/barrier/channel SIS junction in that region, which has a low effective barrier height (less than 0.1 eV) due to the high doping level in the cap layer. At this point, the cap, with a sheet resistance of 50 $\Omega/\square$ and a contact resistance of 0.15 $\Omega \cdot$ mm, begins to conduct current in parallel with the channel and $r_s$ declines. This drop in $r_s$ at 100 mA/mm is the source of the observed kink in the slope of $g_m$ versus $V_{GS}$ seen at $V_{GS} = 0.8$ V in Fig. 2.

Fig. 9 shows extracted $g_{m0}$ versus $V_{GS}$ at $V_{DS} = 5$ V and for $L_g$ between 0.8–2 $\mu$m. We note that the kinks that were apparent in $g_m$ versus $V_{GS}$ have disappeared. The initial rise in $g_{m0}$ as $V_{GS}$ increases from threshold is consistent with mobility-limited electron transport. As $V_{GS}$ is increased further, however, $g_{m0}$ flattens out into a plateau which widens with decreasing $L_g$. The value of $g_{m0}$ in the plateau, about 350 mS/mm, is the same regardless of $L_g$. This behavior indicates that $v_e^{eff}$ in the channel is approaching a saturation velocity, $v_{sat}$ [15].

At sufficiently high $V_{GS}$ (about 1.2 V in our devices), $g_{m0}$ falls off rapidly. This fall-off is due to the gate/barrier/channel diode turning on, with a resulting rise in the gate conductance. Since correcting for such a large effect is inherently unreliable and the device is largely useless in this region, we have chosen not to include the gate conductance in parallel with $C_{gs0}$ in our circuit model. Thus, we treat this model and all extracted circuit element values as being valid only up through the onset of gate leakage.

We look next at the behavior of $C_{gs0}$ versus $V_{GS}$, shown in Fig. 10. As a general trend, we note that $C_{gs0}$ indeed scales up with $L_g$, and thus with gate area, as expected. We gain a more rigorous understanding of $C_{gs0}$ versus $V_{GS}$, however, by comparing our measured results with those of a model. Such a model must account for the nonuniform charge distribution in the channel of a device under drain-source bias.

In particular, we employ the gradual-channel approximation and combine the measured one-dimensional gate-channel

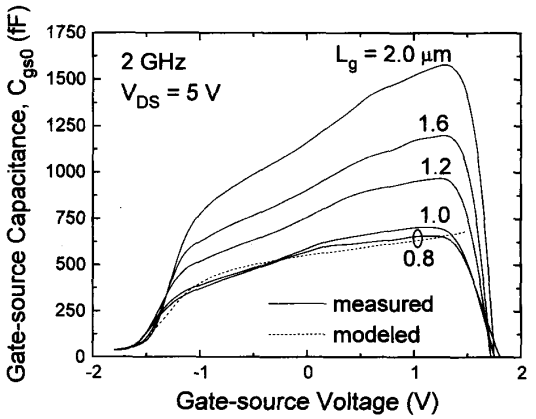


Fig. 10. Extracted $C_{gs0}$ versus $V_{GS}$ for various $L_g$ ($V_{DS}$ = 5 V) together with modeled $C_{gs0}$ versus $V_{GS}$ for an $L_g = 0.8\,\mu$m HFET.

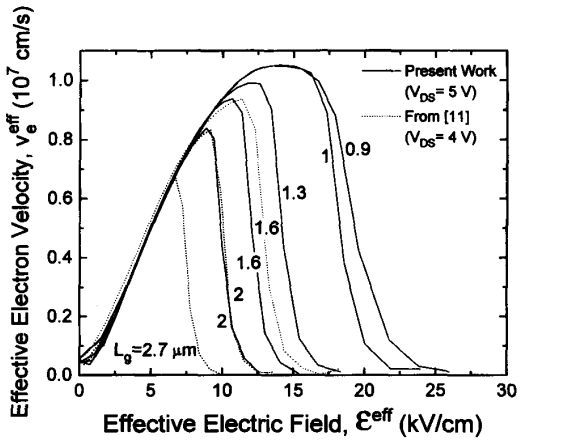


Fig. 11. $v_e^{eff}$ versus $V_{GS}$ for various $L_g$ (present work: $V_{DS}$ = 5 V, [11]: $V_{DS}$ = 4 V). Indicated $L_g$ values are after correction according to procedure described in text.

capacitance of our device (source and drain shorted) with a description of the channel electron velocity-field characteristics. To describe channel transport, we use a simple two-segment piecewise linear characteristic in which $v_e$ is given by $\mu_e\mathcal{E}$ at low fields and saturates to $v_{sat}$ when this velocity is reached. A consequence of our transport model is that the drain end of the channel does not remain pinched off as $V_{GS}$ is increased from threshold, but experiences significant charge modulation once electrons near the drain reach velocity saturation. The result is larger values for $C_{gs0}$ and for the slope of $C_{gs0}$ with $V_{GS}$ compared with the predictions of models which ignore velocity saturation.

The dashed line included in Fig. 10 shows the resulting modeled $C_{gs0}$ versus $V_{GS}$ for a $L_g = 0.8\,\mu$m device, using $\mu_e = 1100$ cm$^2$/V · s and $v_{sat} = 1 \times 10^7$ cm/s. Both of these transport parameters are consistent with values extracted in the discussion below. We note that the excellent agreement between model prediction and measured data, which we achieve only if we account for velocity saturation in our transport model, further supports our preliminary conclusion based on $g_{m0}$ and $f_T$ versus $V_{GS}$ that this phenomenon is occurring in our devices.

Having extracted both $g_{m0}$ and $C_{gs0}$ and established confidence in their proper behavior, we estimate $v_e^{eff}$ in the n$^+$-InP channel using (1). In order to gain as fundamental a view of channel transport as possible, we examine $v_e^{eff}$ versus $\mathcal{E}^{eff}$, where $\mathcal{E}^{eff}$ is an effective channel electric field, defined through

$$\mathcal{E}^{eff} = \frac{V_{GS0} - V_T}{L_g} \tag{4}$$

Here, $V_{GS0}$ is the intrinsic gate-source voltage obtained by subtracting the parasitic source resistance potential drop from $V_{GS}$, and threshold voltage $V_T$ is defined as the $V_{GS}$ value required to yield $I_D = 1$ mA/mm.

Since $L_g$ appears in both (1) and (4), we are careful to ensure that we use accurate values for this quantity, which can differ from the $L_g$ drawn on the mask due to variations in photolithography. To account for this variation, we employ a correction method based on two principles. First, since all devices are fabricated on the same heterostructure, we expect the slope of $v_e^{eff}$ versus $\mathcal{E}^{eff}$, proportional to channel mobility, to be the same for all devices at low fields ($V_{GS}$ just above threshold). Second, our experience with photolithography shows that $L_g$ variation generally effects only the smallest $L_g$ values, with gates longer than about 1.5 $\mu$m tending to reproduce quite accurately. Thus, we take our longest, $L_g = 2\,\mu$m device to be of the proper length and correct all shorter gates relative to this so as to achieve the same low-field $v_e^{eff}$ versus $\mathcal{E}^{eff}$ slope. We obtain the largest correction with the nominally $L_g = 0.8\,\mu$m device, which becomes 0.9 $\mu$m. In the remainder of this work, we indicate only these corrected values for $L_g$.

Fig. 11 shows the result, plotting $v_e^{eff}$ versus $\mathcal{E}^{eff}$ for devices with various $L_g$. For completeness, we supplement the plot with data from a second set of devices made from a piece of the same heterostructure, but using an earlier-generation mask containing longer gate lengths [11]. Remarkably, although our correction procedure simply aligns $v_e^{eff}$ versus $\mathcal{E}^{eff}$ at low-fields, we find that both the $L_g = 0.9\,\mu$m and 1.0 $\mu$m devices track each other precisely *even at high fields as the curves plateau.* Thus, by adjust $L_g$ to fit the curves at one point, they proceed to match everywhere as well. We also note that devices of comparable adjusted gate length from the two separate samples display $v_e^{eff}$ versus $\mathcal{E}^{eff}$ profiles that fall virtually on top of one another as well, with the same peak $v_e^{eff}$ values. These two results each support the validity of the correction procedure.

Considering Fig. 11, we note that $v_e^{eff}$ does indeed rise linearly with $\mathcal{E}^{eff}$ at low fields, indicating mobility-limited transport with $\mu_e = 1100$ cm$^2$/V · s. In the shortest-gate devices, however, we clearly observe $v_e^{eff}$ to flatten into a plateau at high fields, with a plateau value of $1.05 \times 10^7$ cm/s. The presence of this plateau indicates the onset of velocity saturation. As $L_g$ increases, devices continue to follow the same curve, but achieve increasingly lower peak fields and

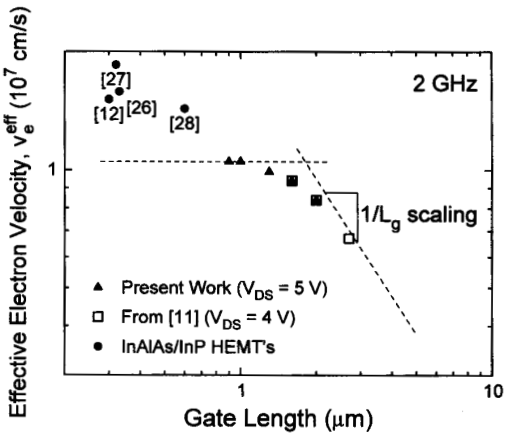


Fig. 12. Maximum $v_e^{eff}$ versus $L_g$ (present work: $V_{DS} = 5$ V, [11]: $V_{DS} = 4$ V). Values for several InAlAs/InP HEMT's (estimated from reported $f_T L_g$) included for comparison [12], [26]–[28].

therefore lower peak electron velocities before the onset of gate leakage.

To examine this scaling behavior further, we plot in Fig. 12 the maximum $v_e^{eff}$ attained over $V_{GS}$ at each $L_g$. We find that $v_e^{eff}$ scales up as approximately $1/L_g$ with decreasing $L_g$ for $L_g > 1.6\,\mu$m, as expected for devices that remain mobility-limited at all bias. For $L_g$ below 1.6 $\mu$m, $v_e^{eff}$ saturates to about $1.05 \times 10^7$ cm/s.

In the moderate electric field range between 5–50 kV/cm, bulk undoped InP shows a broad velocity peak that reaches up to $2.6 \times 10^7$ cm/s [10]. We do not observe any influence of this peak in our devices, however. Instead, our extracted velocity agrees well with the saturation velocity expected for InP at very high electric fields (above 50 kV/cm) [10].

Our inability to observe the velocity peak is most likely due to the presence of doping in the channel, as suggested by a comparison with estimated electron velocities achieved in reported InAlAs/InP HEMT devices [12], [26]–[28]. Since we cannot perform the careful $v_e^{eff}$ extraction used in this study, we take the reported $f_T \cdot L_g$ product as a lower-bound $v_e^{eff}$ estimate and superimpose several such values on the $v_e^{eff}$ versus $L_g$ data for our doped-channel devices in Fig. 12. We note that undoped InP-channel devices achieve values for $v_e^{eff}$ of about $1.6 \times 10^7$ cm/s, much closer to the expected peak velocity for InP.

Doping is known to degrade the steady-state velocity-field characteristics of the common III–V semiconductors [29]. In addition to reducing low-field mobility, doping is found to decrease the peak electron velocity and to increase the electric field ($\mathcal{E}_{peak}$) at which electrons attain this peak velocity [29]. At sufficiently high doping levels, the velocity peak can become indiscernible, leading to a curve that simply rises monotonically from zero toward $v_{sat}$ with increasing field.

Since this behavior, which we observe in the InAlAs/n$^+$-InP MIDFET, seems to eliminate the possibility of observing values for $v_e^{eff}$ in excess of $v_{sat}$ in the MIDFET design, it might seem initially unrealistic to pursue such a device design for high-frequency applications. Yet, both n$^+$-InGaAs-and n$^+$-GaAs-channel devices of comparable or longer gate lengths to those presented here are, in fact, observed to display values for $v_e^{eff}$ significantly beyond $v_{sat}$, and thus, presumably, beyond the peak velocity of the doping-degraded steady-state velocity-field curve [13]–[16], [30]. This picture strongly suggests that a proper correlation of channel material and doping level with observed $v_e^{eff}$ hinges on understanding not only steady-state transport but also nonstationary or transient transport in the channel, which Monte Carlo simulations have shown to be important in III–V devices with heavily doped channels at submicrometer gate lengths [13].

Although achieving nonstationary values for channel $v_e^{eff}$ beyond $v_{sat}$, known as velocity-overshoot, is distinct from observing a peak velocity above $v_{sat}$ in steady-state, the two phenomena are, in fact, related. Overshoot in the common III–V materials is due to Γ-valley electrons temporarily achieving energies above the L-valley minima prior to relaxing into these satellite valleys. Thus, a necessary condition for observing overshoot in a III–V device is achieving values for $\mathcal{E}^{eff}$ corresponding to a significant steady-state L-valley population, or, equivalently, to achieving $\mathcal{E}^{eff} > \mathcal{E}_{peak}$ [31]. Evaluating this minimum criterion for observing overshoot in devices of a given gate length but with differing doping levels or channel materials therefore reduces to estimating $\mathcal{E}_{peak}$ and comparing this value with the maximum $\mathcal{E}^{eff}$ achieved in the device channel.

Using a simple Boltzmann transport equation model described elsewhere [29], [32], we can estimate a value for $\mathcal{E}_{peak}$ in the channel of our devices of about 20 kV/cm. We note from Fig. 11, however, that $\mathcal{E}^{eff}$ never exceeds this value in our devices, explaining why we observe $v_e^{eff} \leq v_{sat}$ without any indication of nonstationary transport. In contrast, an n$^+$-InGaAs channel of similar doping level shows a much lower $\mathcal{E}_{peak}$ value of about 8000 kV/cm. This minimum criterion for observing velocity overshoot is easily exceeded by devices of comparable gate lengths to the devices reported here. These results suggest the strong possibility for improving the frequency response of our InP-channel device design in future processing runs by scaling down $L_g$ to raise the achievable channel field beyond $\mathcal{E}_{peak}$.

As a conclusion to our work, we assess the InAlAs/n$^+$-InP HFET in regard to application suitability, compared against other HFET designs on InP. Our study suggests that the merits of the InAlAs/n$^+$-InP HFET stem from its wide bandgap channel combined with the fact that the channel electrons remain cold even at large $V_{GS}$ and $V_{DS}$ (with no evidence of real-space transfer in $I_D$ or $I_G$ observed over the full bias range, despite the relatively low $\Delta E_c$ of the InAlAs/InP system). The InAlAs/n$^+$-InP is thus the most attractive design for applications demanding small $I_G$, low $g_d$, and high $BV_{DS}$ and where moderate frequency response is an acceptable tradeoff in gaining these merits. For applications stressing the highest frequency response over power handling ability, the InGaAs-channel HFET is perhaps the best choice, but also suffers from a variety of hot-electron related effects

[4], [9], [33]. The InAlAs/InP HEMT is a third alternative falling between these other two options, with values for $v_e^{eff}$ about 70% greater compared with the InAlAs/n$^+$-InP MIDFET, but, in devices of comparable $L_g$ to those reported here, with somewhat reduced $I_{D,MAX}$ or $BV_{DS}$ [34], [35].

## IV. Conclusions

InP offers promise as an active channel material for HFET's stemming from its high breakdown field and high peak electron velocity. In this study, we have explored the specific influence of these properties on device performance, using InAlAs/n$^+$-InP HFET's as a vehicle. We find the wide bandgap of InP eliminates impact ionization, resulting in very low $I_G$ (and thus potentially low input noise in optoelectronic receiver applications), low $g_d$, and high breakdown voltage that increases with increasing $I_D$. In addition, examining the scaling of the effective channel electron velocity versus $L_g$ reveals that $v_e^{eff}$ in devices with $L_g < 1.6\,\mu$m saturates at about $1.05 \times 10^7$ cm/s, the high-field saturation velocity for the material. The higher peak velocity is not observed, which we attribute to the impact of channel doping both on this peak velocity and on the conditions necessary for observing velocity overshoot. These findings suggest that channel electrons in the InAlAs/n$^+$-InP HFET remain cold over the full bias range, making the device well-suited to power applications demanding small $I_G$, low $g_d$, and high $BV_{DS}$, and where moderate frequency response is an acceptable tradeoff.

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