Off-State Breakdown in InAlAs/InGaAs MODFET's

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***Abstract*— Recent efforts are being focussed on improving the breakdown voltage (BV) of InAlAs/InGaAs MODFET's on InP towards high-power applications. A detailed understanding of the physics of breakdown in these devices is still lacking. In this work, we carry out a study of off-state breakdown on state-of-the-art MODFET's in this material system. Through a combination of a *surface-depleted* cap and *mesa-sidewall isolation* the devices have BV's of around 10 V. We find that BV shows a negative temperature coefficient and also decreases with a higher InAs mole fraction in the channel. As we have recently found in InAlAs/n^+–InGaAs HFET's, off-state breakdown appears to be a two-step process. First, electrons are emitted by thermionic-field emission from the gate to the insulator. Second, as a consequence of the large electric field in the insulator and the substantial ΔE_C between insulator and channel, they enter the channel hot, into the high-field drain-gate region, and relax their energy through impact-ionization. This combined hypothesis is able to explain why the MODFET breakdown voltage depends on both channel and insulator design parameters.**

I. Introduction

Research on the InAlAs/InGaAs Modulation-Doped Field-Effect Transistor (MODFET) on InP has been strongly motivated by the excellent transport properties of InGaAs, a material lattice-matched to InP at an InAs mole-fraction, x, of 0.53. $In_{0.53}Ga_{0.47}As$ has a number of advantages over GaAs [1], which make it a superior material for ultra-high frequency and low-noise applications. These features have enabled the InAlAs/InGaAs MODFET to achieve record high-frequency and low-noise performance [2].

InAlAs/InGaAs FET's, however, have one fundamental weakness when compared to GaAs-based FET's and that is their low breakdown voltage, BV. This is basically due to two fundamental facts. First, $In_{0.53}Ga_{0.47}As$ has a bandgap (E_G) of 0.73 eV [3], about half the bandgap of GaAs ($E_G =$ 1.42 eV) [4]. Second, $In_{0.52}Al_{0.48}As$ has a lower Schottky barrier height (0.66 eV [5]) than AlGaAs ($\approx$1 eV [6]). These two facts [7] limit the breakdown voltage of FET's based on the InAlAs/InGaAs system. For example, until recently InAlAs/InGaAs MODFET's have rarely exhibited BV over 5 V [8].

Lately, there has been considerable experimental work towards improving the breakdown voltage of InAlAs/InGaAs MODFET's on InP. One can classify this effort into four categories. First, enhancement of the effective gate-Schottky barrier has been carried out by using an undoped InAlAs layer directly beneath the gate [9], by increasing the Al-mole fraction in the insulator [10]–[13], and by moving a portion of the dopants from the top InAlAs layer to the buffer layer (reverse MODFET) [14]. Second, efforts to reduce the peak electric-field in the drain-gate gap have focussed on double gate-recessing [15], surface-undoped caps [16], and surface-depleted caps [17], [18]. Third, channel bandgap enhancement was carried out by using an InGaAsP layer [19], or a composite InGaAs/InP channel [20]. Also, channel bandgap grading has been performed with good results [21]. Fourth, mesa-sidewall isolation was performed [18], [22], [23], [24] to eliminate a parasitic gate-leakage path [25]. As a result of these efforts, state-of-the-art MODFET's currently achieve drain-gate breakdown voltages (defined at 1 mA/mm of gate width) of 10 to 13 V [15], [18], [20], [23].

There has also been some work directed to understanding the mechanism of breakdown in the on-state (channel conducting). On-state breakdown is believed to occur by impact-ionization in the high-field region of the InGaAs channel [26, 27, 28, 29, 30, 31], although a systematic study has yet to be carried out. An understanding of off-state breakdown (channel off) is also important for many applications. For instance, the off-state drain-source breakdown voltage, BV_{DS}, limits the power density of class-A amplifiers [2]. Although there has been a large empirical effort to increase BV_{DS}, there has not been much work directed to produce fundamental understanding of the physics of off-state breakdown in InAlAs/InGaAs MODFET's.

In this paper, we present the first comprehensive experimental study of off-state breakdown in InAlAs/InGaAs MODFET's. This work draws upon a previous study carried out by two of the authors into the physics of breakdown in InAlAs/n^+–InGaAs HFET's [32], which has allowed us to formulate a convincing hypothesis for the physics of off-state breakdown in InAlAs/InGaAs MODFET's. The hypothesis is consistent with previous findings on breakdown reported in the literature for InAlAs/InGaAs MODFET's [9], [12], [13], [14], [15], [16], [18], [19], [20], [27], [28]. In this work, we used the *Drain-Current Injection Technique* [33] to characterize three-terminal off-state breakdown.

II. Experimental

This work is based on devices fabricated by Daimler-Benz [18]. The heterostructure was grown by MBE on a semi-insulating InP substrate. A schematic of the cross-section is shown in Fig. 1. The layer sequence (bottom to top) is

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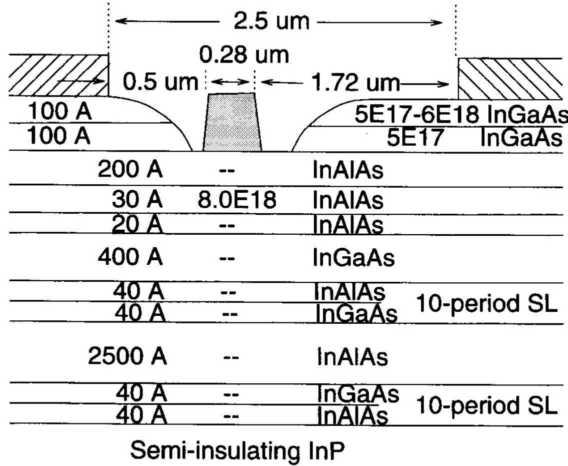

Fig. 1. Schematic cross-section of heterostructure. Three structures were grown with InAs-mole fraction, x =0.53, 0.62, and 0.70 in the channel. For the $x = 0.70$ sample, the lower 250 Å of the channel was grown with $x = 0.53$. All other layers are lattice-matched to the substrate. The Si-doping is expressed in units of cm^{-3}.

TABLE I
KEY FIGURES OF MERIT AND ELECTRICAL PARAMETERS OF MODFET's ($L_G = 0.28$ μm, $W_G = 80$ μm) USED IN THIS STUDY. THE LOW-FIELD MOBILITY AND CARRIER CONCENTRATION WERE OBTAINED FROM SHUBNIKOV-DE HAAS OSCILLATIONS AT 2 K.

x	V_T (V)	$I_{D(MAX)}$ (mA/mm)	$g_{m(PEAK)}$ (mS/mm)	f_t (GHz)	f_{max} (GHz)	μ @ 2K ($cm^2/V \cdot s$)	n_S @ 2K (cm^{-2})
0.53	-0.6	275	400	83	140	40,000	2.0×10^{12}
0.62	-0.6	290	450	87	150	49,000	2.2×10^{12}
0.70	-0.6	350	550	93	180	54,000	2.5×10^{12}

as follows: a buffer comprising a 2500 Å InAlAs layer sandwiched between 10-period (40 Å InGaAs, 40 Å InAlAs) superlattices; a 400 Å InGaAs channel; an InAlAs insulator comprising a 20 Å spacer, 30 Å heavily Si-doped ($N_D = 8 \times 10^{18}$ cm^{-3}) layer, and a 200 Å barrier enhancement layer. The structure was capped with an exponentially-doped (5×10^{17} to 6×10^{18} cm^{-3}) 200 Å thick InGaAs layer. All layers are undoped and lattice matched to the substrate unless specified. The cap was designed to be *surface-depleted* [17] for higher breakdown voltage. Three different heterostructures were characterized in this study, with different InAs mole-fractions of $x = 0.53$ (lattice-matched), $x = 0.62$, and $x = 0.70$ in the channel. For the device with $x = 0.70$, the lower 250 Å of the channel was grown with a lattice-matching composition of $x = 0.53$ to avoid excessive strain. Processing was carried out according to the sequence described in Ref. [18]. The cap was etched selectively, and mesa-sidewall isolation was used in all heterostructures. This prevents the gate contact to the InGaAs channel at the mesa-sidewall [24]. The devices used in this study were unpassivated.

MODFETs with $L_G = 0.28$ μm and $W_G = 80$ μm were characterized. Some important figures of merit of the resulting devices are tabulated in Table I. The lattice-matched device had $I_{D(\text{MAX})} = 275$ mA/mm, $g_{m(\text{PEAK})} = 400$ mS/mm, $f_t = 83$ GHz, and $f_{\max} = 140$ GHz. Further device characterization is presented in [18]. In this study, both drain-source breakdown voltage, BV_{DS}, and drain-gate breakdown voltage, BV_{DG}, were measured. As described below, BV_{DS} and BV_{DG} were 8.9 V and 9.9 V respectively for the lattice-matched device. The terminology, "drain-source breakdown voltage" refers to the breakdown of the drain with respect to the grounded source, i.e. the sharp rise of I_D on the output I-V characteristics [2]. It does not necessarily imply that breakdown occurs in the drain-source path. We have defined BV_{DG} at $I_D = 1$ mA/mm with source floating, and BV_{DS} as the maximum drain-source voltage the device can attain with $I_D = 1$ mA/mm regardless of V_{GS} [32], [33].

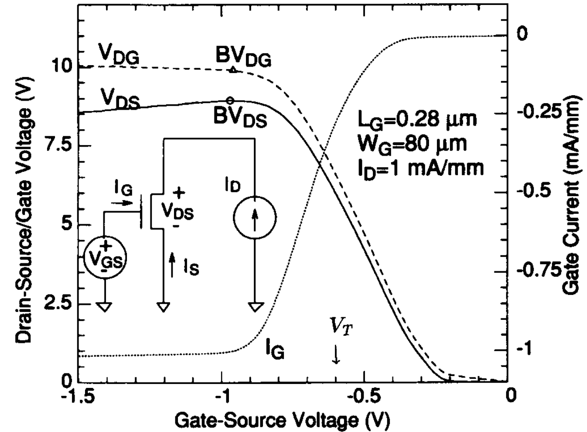

Fig. 2. A Drain-Current Injection scan ($I_D = 1$ mA/mm) showing V_{DS}, V_{DG}, and I_G vs. V_{GS} for the lattice-matched device. The inset shows the schematic circuit diagram.

We used the Drain-Current Injection technique to measure BV_{DS} and BV_{DG} [32, 33]. This is a relatively safe technique for the characterization of three-terminal FET off-state breakdown. In a single sweep, both BV_{DS} and BV_{DG} are obtained. The schematic is shown in the inset of Fig. 2. We have implemented it using the HP-4145B semiconductor parameter analyzer.

Temperature dependent measurements were performed using a low-temperature probe station from MMR Technologies, Inc. In a temperature-breakdown scan, the temperature was scanned from high to low temperatures. This was done to avoid the presence of moisture from the melting of the slight condensate on the sample if the temperature were raised through the freezing point of water. The initial instability due to device degradation was minimized by repeatedly scanning the device (typically 2–4 times) at the starting temperature till a steady-state characteristic was obtained.

III. RESULTS

A typical Drain-Current Injection scan [33] ($I_D = 1$ mA/mm) for the lattice-matched device is shown in Fig. 2 at 300 K. The figure shows a plot of V_{DG}, V_{DS} and I_G vs. V_{GS}. Starting at $V_{GS} = 0$ V, the device is on, the channel resistance is low, and therefore $V_{DS} \approx 0$ V. Since V_{DG} is small, I_G is also very low. The gate-source voltage is then ramped down to below threshold ($V_T = -0.6$ V). As the channel is shut off, both V_{DS} and V_{GS} rise sharply in order to accomodate the

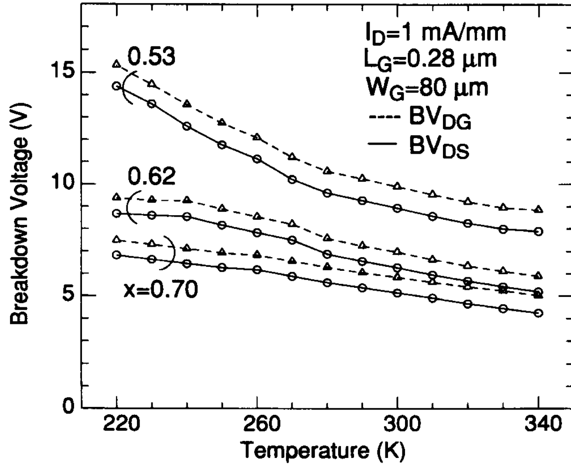

Fig. 3. Drain-source and drain-gate breakdown voltages, BV_{DS} and BV_{DG}, vs. temperature as a function of InAs molefraction, x, in the channel.

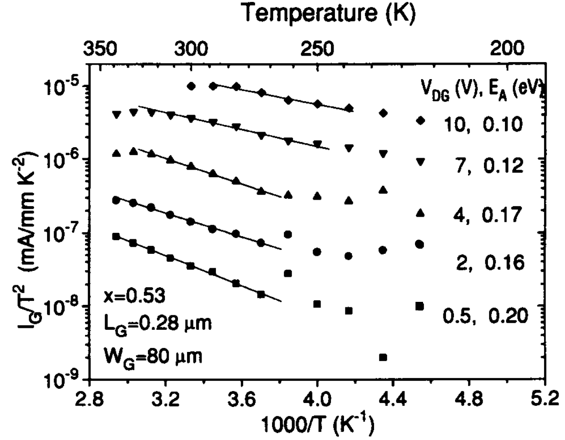

Fig. 4. An Arrhenius plot of log (I_G/T^2) vs. $1000/T$ for the $x = 0.53$ device.

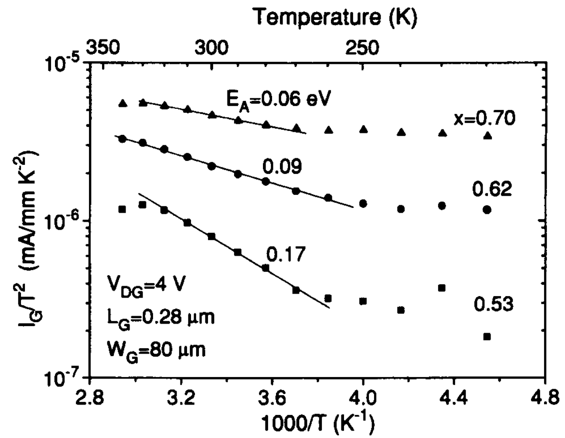

Fig. 5. An Arrhenius plot of log(I_G/T^2) vs. $1000/T$ for $V_{DG} = 4$ V as a function of x.

constant 1 mA/mm of current being injected into the drain. This can initially be done through short-channel effects, but eventually the device is driven into breakdown. Breakdown occurs in the drain-gate path, causing a larger negative I_G. At $V_{GS} = -0.97$ V, V_{DS} peaks at $BV_{DS} \equiv 8.9$ V. For $V_{GS} = -0.96$ V, I_G becomes -1 mA/mm. This defines BV_{DG} since at this bias point, $I_S = 0$, and the configuration is equivalent to a two-terminal drain-gate measurement with source floating (there is negligible leakage current from the reverse-biased gate-source junction). Upon decreasing V_{GS} further, V_{DS} decreases linearly with V_{GS}, showing a slope of ≈ 1, while V_{DG} remains constant at about 10 V.

The data shows that when the channel is turned off, all the injected drain-current comes out of the gate, and V_{DG} becomes independent of V_{GS}. This behavior is a clear signature of gate breakdown, rather than channel breakdown, and shows that gate breakdown limits the maximum drain-source voltage of the device. The same conclusions were reached for devices with $x = 0.62$ and 0.70 in the channel.

Temperature dependent measurements were carried out on the MODFET's between 340 K and 220 K. A plot of BV_{DS} and BV_{DG} vs. T is presented in Fig. 3. At 300 K, BV_{DS} was 8.9 V, 6.3 V, and 5.1 V for $x = 0.53$, 0.60, and 0.70 respectively. These are very high values for InAlAs/InGaAs MODFET's. In all devices, BV_{DS} and BV_{DG} show a *negative* temperature coefficient. V_{DS} was limited by gate breakdown for the entire range of temperatures in all devices (the Drain-Current Injection scan showed the same features as Fig. 2). BV_{DS} and BV_{DG} track each other with a difference of about V_T, consistent with the above finding. BV_{DS} increases from 7.9 V at 340 K to 14.4 V at 220 K for $x = 0.53$. Since the breakdown voltage due to impact-ionization has a positive temperature coefficient [7], it follows that breakdown cannot be a simple impact-ionization phenomena, as might be expected for a narrow bandgap channel with long mean-free path [34]. This is also confirmed in a separate temperature-dependent study of the conventional output characteristics of these devices [30].

As in our work on InAlAs/n^+-InGaAs HFET's [32], we investigated the temperature dependence of the gate current approaching breakdown. Here, we present a similar study on MODFET's. Data from the locus of the Drain-Current Injection technique ($I_D = 1$ mA/mm) was used. I_G was found to be thermally activated in the range of temperatures around room-temperature (340 K to 260 K). An Arrhenius plot of I_G/T^2 was generated for several values of V_{DG} from above threshold to breakdown. Fig. 4 is a plot of the data for $x = 0.53$. The activation energy of the gate current, E_A, was found to decrease slowly from 0.2 eV at $V_{DG} = 0.4$ V to 0.1 eV at $V_{DG} = 10$ V. As x was increased in the channel, a given V_{DG} resulted in larger I_G and lower E_A. The data is plotted for the three channel compositions in Fig. 5 for $V_{DG} = 4$ V. E_A is 0.17 eV, 0.09 eV, and 0.06 eV for $x = 0.53$, 0.62, and 0.70 respectively. Note also that as the temperature is lowered towards 220 K, I_G tends to saturate, suggesting a transition to tunneling [7]. The above findings are consistent with additional results presented in [30].

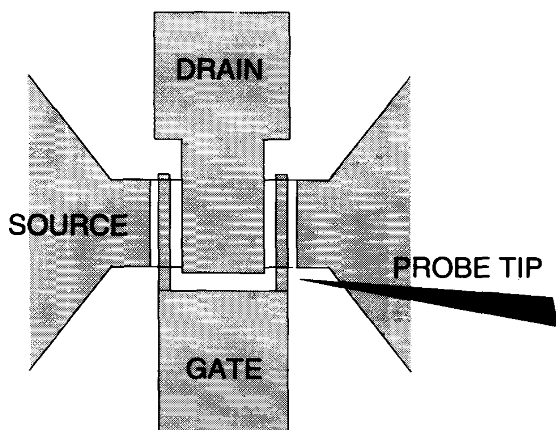

Fig. 6. A schematic diagram of the HFET layout, showing location of probe tip in sidegating measurements.

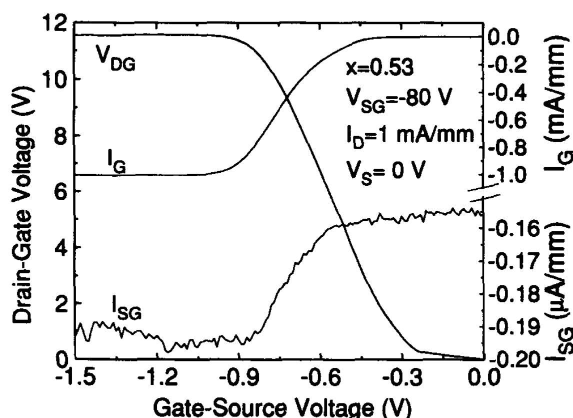

Fig. 7. A Drain-Current Injection scan at $I_D = 1$ mA/mm, including sidegate current. The correlation between I_G and I_{SG} indicates that holes are generated during breakdown.

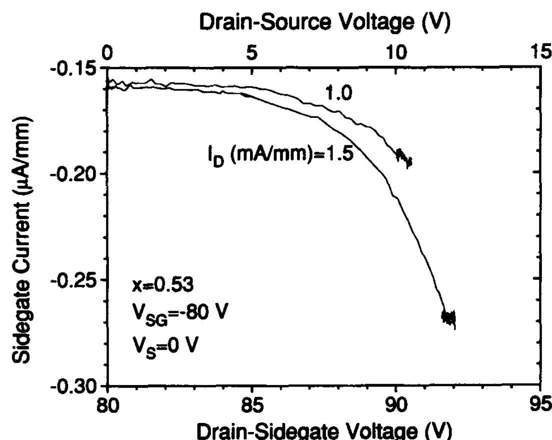

Fig. 8. A plot of the sidegate current vs. drain-sidegate voltage. The data was measured by Drain-Current Injection scans at I_D =1 mA/mm and 1.5 mA/mm.

We have also used the *sidegating* technique [32, 35] to investigate whether electron-hole pairs are generated in the channel during breakdown. Specially designed sidegate structures such as those in Ref. [32] were not available, but we found that a probe tip biased at -80 V and positioned close to the intrinsic device (see Fig. 6) was able to capture a few holes. The probe tip was placed away from the drain contact pad to minimize parasitic contribution from the drain-sidegate path, since V_{D-SG} also increases during the breakdown process. A Drain-Current Injection scan at $I_D = 1$ mA/mm was carried out on the FET and the sidegate current monitored. The plot is shown in Fig. 7. As the device is turned-off, V_{DG} increases, accompanied by a simultaneous rise in both I_G and I_{SG}. We have confirmed that the larger I_{SG} is not due to a parasitic drain-sidegate path by carrying out Drain-Current Injection scans with different values of I_D. This is shown in Fig. 8, which is a plot of I_{SG} vs. V_{D-SG}, from Drain Current Injection scans with $I_D = 1$ mA/mm and 1.5 mA/mm. The data shows that for a given V_{D-SG}, larger I_D gives rise to larger I_{SG}. Since in this experiment, the sidegate voltage is very negative, a larger I_{SG} can only arise from holes, thereby showing that an electron-hole pair generation process is in action at breakdown.

IV. Discussion

Before putting forth a hypothesis of off-state breakdown at room temperature, we will summarize the key findings from our work and those that are relevant from the InAlAs/InGaAs MODFET literature:

1. BV improves with methods that enhance the effective gate-Schottky barrier height [9], [12], [13], [14].
2. BV increases with techniques that reduce the peak electric-field at the drain edge of the gate [15], [16], [18].
3. BV improves for channel materials with higher bandgap [19], and decreases for materials with lower bandgap (this work and work from other groups [36]).
4. V_{DS} is limited by gate breakdown for L_G as small as 0.28 μm (this work, [30]).
5. BV_{DS} and BV_{DG} have a negative temperature coefficient (this work, [30]).
6. I_G is thermally activated approaching breakdown with $E_A \approx 0.1$ eV (this work).
7. Holes are generated during breakdown (this work).
8. Gate electrons, *not* channel electrons, are responsible for off-state breakdown (this work, discussed later).

There is no simple theory that can explain the above findings. Since the breakdown voltage due to impact-ionization has a positive temperature coefficient [7], it follows that breakdown cannot be a simple impact-ionization phenomena. Furthermore, if breakdown was due to thermionic-field emission alone, holes would not be generated in the process. The findings summarized above, however, are qualitatively identical to those that we obtained on InAlAs/n^+–InGaAs HFET's [32]. In a way, this is rather remarkable since the present devices differ considerably from those in [32] in their much shorter gate-length, different cap design, the presence

of dopants in the insulator, the absence of dopants in the channel, incorporation of gate-recessing, and different buffer-layer. The similitude of experimental observations regarding off-state breakdown in such dissimilar devices reveals how fundamentally the breakdown process is associated with the materials involved.

The thermionic-field emission/Auger-generation hypothesis we proposed for the InAlAs/n^+—InGaAs HFET [32] can explain all the findings for the MODFET. Auger generation [34] is also referred to as "impact-ionization at a potential step" [37]. This phenomena finds use in avalanche photodiodes to reduce the multiplication noise [38]. Essentially, electrons going from the InAlAs insulator to the InGaAs channel suddenly gain a kinetic energy equal to ΔE_c from the conduction-band step. This is in addition to the energy they already acquired from the electric-field in the insulator. For $In_{0.52}Al_{0.48}As$ /$In_{0.53}Ga_{0.47}As$, $\Delta E_c = 0.5$ eV [39], which is considerable compared to the bandgap of $In_{0.53}Ga_{0.47}As$ (0.73 eV) [3]. In this case, the presence of even a low electric-field in the insulator can give rise to impact-ionization in the channel. The combined thermionic-emission/Auger-generation process, shown schematically in Fig. 9(a), is a two step process. First, electrons are injected from the gate edge into the high-field drain-gate region of the insulator by thermionic-field emission. Second, because of the large conduction-band offset and the electric-field in the insulator, they enter the channel hot, and immediately relax their energy through impact-ionization. The electrons flow towards the drain, and the holes can either be extracted by the gate or flow towards the source, where they recombine with electrons. This process actually occurs in two-dimensions, with electron injection likely to take place sideways from the gate into the drain-gate gap, as illustrated on a two-dimensional sketch in Fig. 9(b). The need to assume sideways injection arises because, similar to the AlGaAs/GaAs HEMT [40], [41], the GaAs MESFET [42], and the InAlAs/n^+-InGaAs HFET [32], there is a high-field region at the gate edge of the drain-gate gap.

Before we proceed, we must first rule out another mechanism. Zener tunneling in the channel is qualitatively consistent with some of our findings. In this process, BV would show a negative temperature dependence through the temperature dependence of the channel bandgap [3], and holes would also be generated in the channel. These holes could be extracted by the negatively biased gate and appear as gate-current. To investigate this hypothesis, we have examined the dependence of I_G on E_G (which changes with temperature [3]) as a function of V_{DG} approaching breakdown. Simple Zener theory [34] demands that the dependence of I_G on E_G weakens at higher V_{DG}. We find precisely the contrary. We therefore rule out Zener tunneling in the channel as a dominant mechanism.

The absence of Zener tunneling in the channel is consistent with results in the literature that for a fixed channel design, BV improves with methods which increase the gate Schottky-barrier height [12]–[14]. It is also consistent with the fact that the InAlAs/n^+-InGaAs HFET (heavily doped channel) has higher BV than the InAlAs/InGaAs MODFET (undoped channel). An increase in BV with channel doping is not consistent with Zener [7].

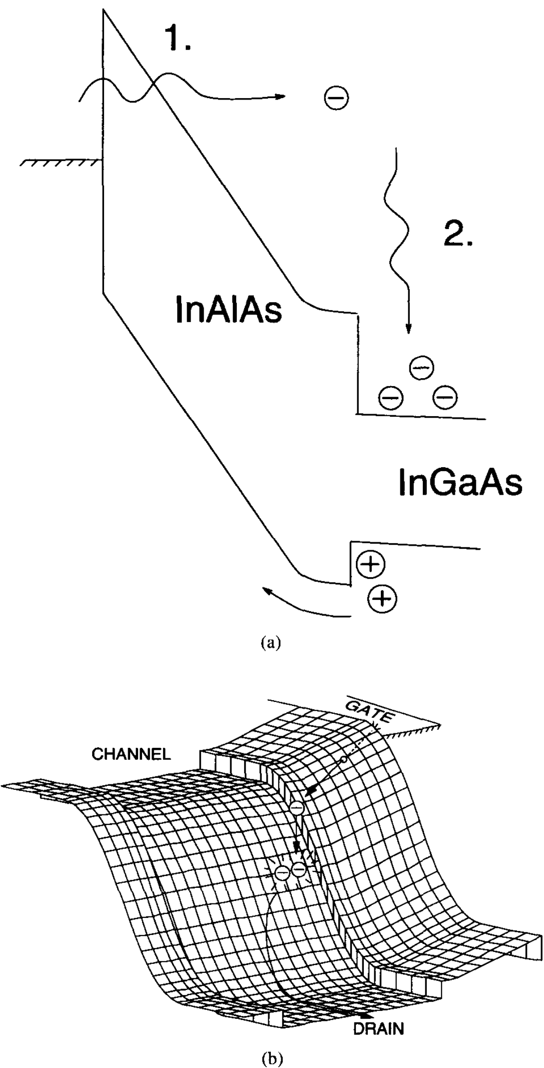

Fig. 9. A schematic diagram showing the combined effect of electron thermionic-field emission and Auger generation. (a) Basic mechanism, (b) two-dimensional drawing. Electrons are injected sideways through thermionic-field emission from the gate into the high-field drain-gate region of the insulator (step 1). They enter the channel hot and impact-ionize by Auger generation (step 2).

We will now explain the experimental findings on MODFET's in terms of the Thermionic-field emission/Auger-generation hypothesis. First, off-state breakdown depends upon insulator design because electron thermionic-field emission depends upon the insulator composition and the potential distribution under the gate. The activation energies obtained in the previous section for the gate current are substantially lower than the Schottky barrier height of metals on InAlAs [5]. This is most surely due to the presence of a high doping concentration inside the InAlAs pseudoinsulator which produces sharp band bending underneath the gate metal (see Fig. 9(a)). The removal of dopants from the insulator can increase the effective gate-Schottky barrier height [43], as can

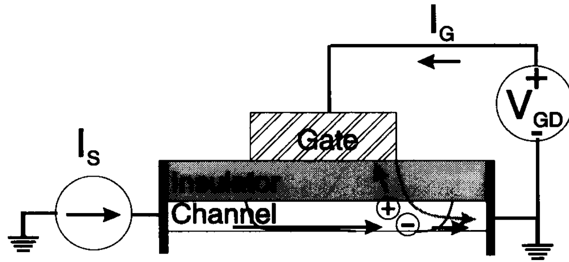

Fig. 10. A schematic showing the biasing circuit for the experiment of Fig. 11. The solid arrows show the flow of source electrons and their generated holes (if any). The shaded arrow shows electron flow from the gate to the drain.

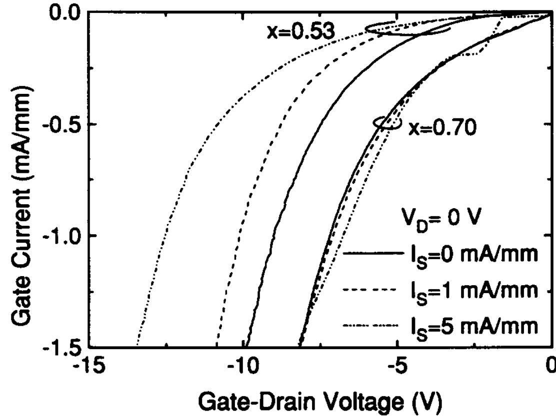

Fig. 11. I_G vs. V_{GD} as a function of I_S. The measurement shows that source electrons do not appear to trigger breakdown.

also a low-InAs insulator [10], [11]. Therefore, the use of an undoped or lower-doped InAlAs layer [9], [14], [32], or the use of low-InAs InAlAs [12], will increase BV. In the case of the (undoped-insulator) $In_{0.41}Al_{0.59}As/n^+$-$In_{0.53}Ga_{0.47}As$ HFET, we measured [32] $E_A \approx 0.45$ eV approaching breakdown. In this case, BV_{DS} was 17 V at 300 K. As a further note on the relevance to breakdown of electron injection from the gate to the insulator, our hypothesis is consistent with the observed increase in BV at lower temperatures, shown in Fig. 3, since electron emission from the gate is reduced.

Second, methods which reduce the peak electric-field at the gate-edge [15, 16, 18] are found to increase BV. In our hypothesis, this would occur by increasing the effective Schottky barrier height for thermionic emission sideways into the drain. And third, a decrease in channel bandgap [19] will enhance Auger generation in the channel and degrade BV. In the InAs-rich channel devices, Auger generation is increased both because the channel bandgap is lower [3], and ΔE_c to $In_{0.52}Al_{0.48}As$ increases [39]. An enhancement of Auger generation may also explain our observation of lower activation energy of the gate current for the high-InAs samples. This can arise from a partial offset of the negative temperature coefficient of the thermionically emitted electron current with the positive temperature coefficient of holes generated by impact-ionization and to some extent collected at the gate.

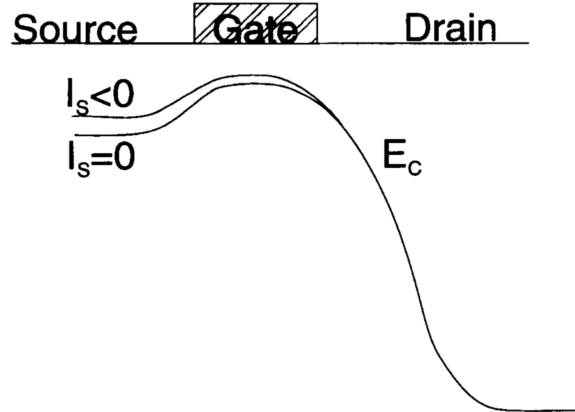

Fig. 12. A conduction-band diagram, drawn from source to drain. The injection of source current can reduce the electric-field in the insulator through *short-channel* effects (see text).

We now discuss the effect of source current on off-state breakdown. The experiment is motivated by results from the InAlAs/InGaAs MODFET literature, which shows that electron flow through a high-field region in the InGaAs channel causes impact-ionization [27], [29]. Some of the generated holes are collected by the gate and comprise gate current [28], [44]. We wish to see to what extent this mechanism plays a role at around threshold. The biasing circuit in our measurement is shown in Fig. 10. Essentially, we have carried out a measurement of gate-drain I-V characteristics with varying amounts of source current. The flow of source electrons and their generated holes has been illustrated schematically by the solid arrows. Also illustrated, by the lightly shaded arrow, is the flow of gate electrons.

The experimental data is presented in Fig. 11. First, a two-terminal gate-drain (source floating) scan was carried out. This scan was then repeated with $I_S = -1$ and -5 mA/mm. Data is presented for $x = 0.53$ and $x = 0.70$. For $x = 0.70$, larger I_S causes a slight reduction in BV. We attribute this small effect to residual impact-ionization caused by electrons flowing through the high-field channel region [27], [29]. For $x = 0.53$, larger I_S actually *increases* the gate breakdown voltage. This is an unexpected result.

Short-channel effects provide a possible explanation for this apparently anomalous behavior. As sketched in the conduction band diagram of Fig. 12, in a very short device, the potential tails of the source and drain partially overlap in the channel under the gate. This reduces the potential barrier to injecting electrons from the source into the channel. This is the well known Drain-Induced Barrier Lowering (DIBL) phenomenon [45]. As a consequence of this, when the source conduction band is raised to accomodate source current, it lifts up slightly with it the conduction band under the gate, as illustrated in Fig. 12. This reduces the field in the insulator and enhances the barrier against electron injection from gate to drain, therefore suppressing breakdown. The reason for not observing this effect in the $x = 0.70$ device is that in this case the channel is much thinner and DIBL is mitigated. The $x = 0.62$ device

(not shown) also has a 400 Å thick channel and displays the same effect as the lattice-matched device. The main result of this experiment is that a small amount of source electrons do not degrade in any significant way the off-state breakdown of InAlAs/InGaAs MODFET's. This is an important validation for the hypothesis put forward in this paper.

V. Conclusion

We present a temperature-dependent study of the physics of off-state breakdown in ($L_G = 0.28$ μm) InAlAs/InGaAs MODFET's. Breakdown is found to be drain-gate limited and BV shows a negative temperature coefficient. As in InAlAs/n^+–InGaAs HFET's, breakdown is hypothesized to be a two step process. First, electrons are injected from the gate edge into the high-field drain-gate region of the insulator by thermionic-field emission. Second, because of the large conduction-band offset and the electric-field in the insulator, they enter the channel hot, and immediately relax their energy through impact-ionization. This combined mechanism also explains a variety of findings about the off-state breakdown behavior of InAlAs/InGaAs MODFET's from the literature. The understanding gained provides a path for future improvements in the off-state breakdown voltage.

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