Physics of Breakdown in InAlAs/n$^+$—InGaAs Heterostructure Field-Effect Transistors

Sandeep R. Bahl, *Member, IEEE*, and Jesús A. del Alamo, *Senior Member, IEEE*

***Abstract*—InAlAs/n$^+$—InGaAs HFET's on InP have demonstrated a high breakdown voltage in spite of the narrow bandgap of the InGaAs channel. In order to understand this unique feature, we have carried out a systematic temperature-dependent study of off-state breakdown. We find that off-state breakdown at room-temperature is drain-gate limited and that the breakdown voltage shows a negative temperature coefficient. Based on these and other findings, we propose that off-state breakdown is a two-step process. First, electrons are injected by thermionic-field emission from the gate to the insulator. Second, electrons enter into the high-field drain-gate region of the channel hot, and relax their energy through impact-ionization. This combined mechanism explains our experimental observations that off-state breakdown in InAlAs/n$^+$—InGaAs HFET's depends both on channel and insulator design. Our findings are relevant to other InAlAs/InGaAs HFET's, such as the MODFET, as well as HFET's based on other narrow-bandgap materials.**

I. Introduction

InAlAs/InGaAs heterostructure field-effect transistors (HFET's) on InP have emerged as promising candidates for applications in microwave and lightwave communication systems. Modulation-Doped FET's (MODFET's) from this material system have achieved world-record frequency and low-noise performance[1]. There is, however, one fundamental weakness of InAlAs/InGaAs HFET's when compared to GaAs-based FET's. $In_{0.53}Ga_{0.47}As$ has a bandgap (E_G) of 0.73 eV [2], about half the bandgap of GaAs (E_G=1.42 eV) [3]. This limits the breakdown voltage of $In_{0.53}Ga_{0.47}As$-based devices. It is for this reason that, although the advantages of InAlAs/InGaAs HFET's for power microwave applications have been recognized [4], they have yet to be exploited [1]. This is also an important limitation for InP photonics receivers based on InAlAs/InGaAs HFET's, which need a separate low-voltage supply, since the HFET's cannot support the voltages required for optimum MSM photodetector operation [5].

A device structure that might alleviate this problem is the InAlAs/n$^+$—InGaAs HFET [6]–[8]. This device, by virtue of its undoped *pseudo*-insulator, has demonstrated high off-state (channel turned-off) breakdown voltage, BV. In previous work we have shown that BV is engineerable [8], can be increased by using AlAs-rich insulators [9] and is degraded in channels with higher InAs-mole fractions [10] and heavier doping [11]. BV can also be increased by reducing the channel thickness so that the effective channel bandgap is artificially enhanced by quantum-size effects [12]. The empirical work above presents a puzzling picture in which BV depends strongly on both insulator and channel design. No available theory can explain all our experimental observations.

In this paper, we present the first comprehensive experimental study of off-state breakdown in InAlAs/n$^+$—InGaAs HFET's. Our findings allow us to formulate a convincing hypothesis for the physics of breakdown in InAlAs/n$^+$—InGaAs HFET's. Our work also sheds light on the reasons for the low BV of InAlAs/InGaAs MODFET's.

Manuscript received August 19, 1993; revised August 1, 1994. The review of this paper was arranged by Associate Editor N. Moll. This work was supported by the Joint Services Electronic Program under the Research Laboratory of Electronics (DAAL-03-92-C-0001), the C. S. Draper Laboratory (DL-H-441694), Texas Instruments, and Nippon Telegraph and Telephone.

S. R. Bahl was with the Massachusetts Institute of Technology, Cambridge, MA 02139 USA; he is now with Hewlett-Packard Laboratories, Palo Alto, CA 94303 USA.

J. del Alamo is with the Massachusetts Institute of Technology, Cambridge, MA 02139 USA.

IEEE Log Number 9406192.

II. Experimental

Our study is based primarily on the heterostructure in Fig. 1. It was grown by MBE on S.I. InP and consists of (bottom to top), a 1000 Å $In_{0.52}Al_{0.48}As$ buffer, a 75 Å $In_{0.53}Ga_{0.47}As$ undoped subchannel, a 100 Å n$^+$—$In_{0.53}Ga_{0.47}As$ Si-doped channel (N_D=4$\times 10^{18}$ cm^{-3}), a 300 Å $In_{0.41}Al_{0.59}As$ strained insulator, and a 50 Å undoped $In_{0.53}Ga_{0.47}As$ cap. We call this the *default* structure. Another structure, identical except for a larger channel doping (N_D=8$\times 10^{18}$ cm^{-3}) was also used. The heterostructures had sheet charge densities, measured by Hall-effect at 300 K, of 1.2$\times 10^{12}$ cm^{-2} and 3.1$\times 10^{12}$ cm^{-2}, respectively. Mesa-sidewall isolation was used in both heterostructures [13]. Processing is described in [8], and detailed device characterization is presented in [8], [11].

The following devices were used in this study. First, an HFET with (optically measured) gate-length, gate-width, and gate-drain gap; L_G=1.9 μm, W_G=30 μm, and L_{GD}=1.7μm respectively. HFET's with larger L_G were also characterized. Second, a sidegate structure with L_G=2.9 μm and W_G=30 μm. The sidegate contact is formed by ohmic metallization to a heterostructure mesa with dimensions of 15 μm by 40 μm, and lies parallel to the HFET mesa with a separation of 15 μm. It is isolated from the HFET by etching the mesa down to the semi-insulating substrate. A sketch is shown in the inset of Fig. 7.

Both drain-source breakdown voltage, BV_{DS}, and drain-gate breakdown voltage, BV_{DG}, were measured. The "drain-source breakdown voltage" refers to the breakdown of the drain with respect to the grounded source, *i.e.*, the sharp rise of I_D on the output I-V characteristics [1]. It does not necessarily imply that breakdown occurs in the drain-source path. We have defined BV_{DS} as the peak V_{DS} attained with the channel off

0018–9383/94$04.00 © 1994 IEEE

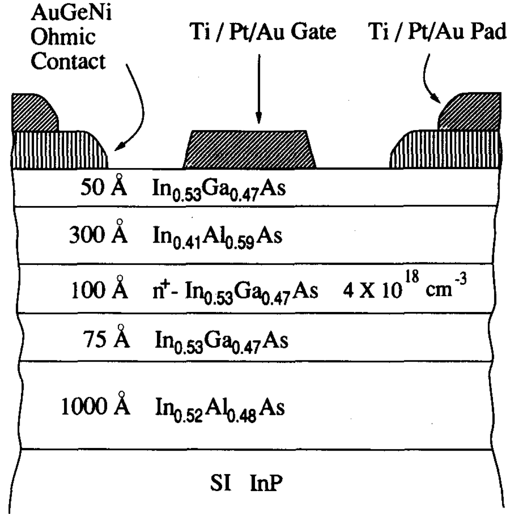

Fig. 1. Cross section of device structure.

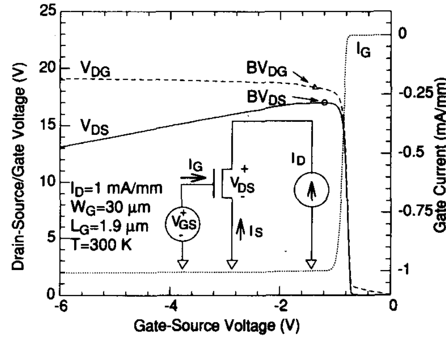

Fig. 2. A Drain-Current Injection scan at I_D=1 mA/mm for the HFET at 300 K. V_{DS} is limited by drain-gate breakdown. The inset shows the schematic circuit diagram.

and I_D=1 mA/mm of gate width, regardless of V_{GS} [14]. We have defined BV_{DG}, according to convention [15]–[17], at I_D=1 mA/mm of gate width with source floating.

To characterize breakdown, we have used the Drain-Current Injection technique [14]. Both BV_{DS} and BV_{DG} are non-destructively obtained in a single sweep. The technique also provides physical insight since it discriminates between gate and channel breakdown (defined by the terminals between which current flows during breakdown). The circuit schematic is shown in the inset of Fig. 2, and is implemented using a HP4145B semiconductor parameter analyzer.

Temperature dependent studies were performed by use of a low-temperature probe station from MMR Technologies, Inc. We scanned from high to low temperatures to avoid the presence of moisture from the melting of the slight condensate that forms on the sample below about 273 K. The initial instability due to device degradation was minimized by repeatedly scanning the device (typically 2-4 times) at the starting temperature until a steady-state characteristic was obtained.

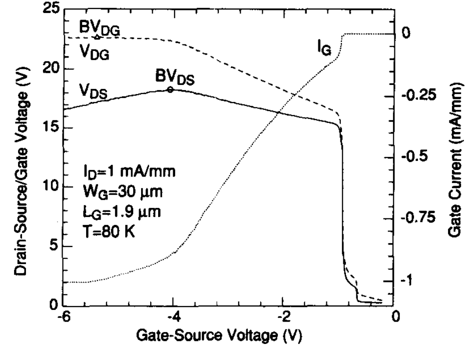

Fig. 3. A drain-current injection scan at I_D=1 mA/mm for the HFET at 80 K. The graph also shows the ability of the drain-current injection technique in resolving channel and gate breakdown regimes.

III. Results

In this section, we present our findings from a systematic study carried out on the sample in Fig. 1. We present the results after a header that captures the key conclusion.

A. At 300 K, V_{DS} Is Limited by Gate Breakdown

Fig. 2 shows a Drain-Current Injection scan at 300 K for a typical HFET. The plot shows V_{DG}, V_{DS} and I_G versus V_{GS} for I_D=1 mA/mm. As V_{GS} is ramped (from 0 V) below threshold, (V_T=-0.8 V) the channel shuts off and both V_{DS} and V_{DG} rise sharply to meet the condition of a constant 1 mA/mm injected into the drain terminal, and the device is driven into breakdown. At V_{GS}=-1.2 V, V_{DS} peaks at 17 V and V_{DG} plateaus to $\approx$ 18.3 V. The peak V_{DS} unambiguously defines BV_{DS}. Furthermore, the drain-gate voltage at I_G=-1 mA/mm unambiguously defines BV_{DG}, since at this point there is negligible leakage current from the reverse-biased gate-source junction ($I_S \approx 0$). Upon reducing V_{GS} further, V_{DS} decreases linearly with V_{GS}, showing a slope of ≈ 1, while V_{DG} remains constant at ≈ 19 V. This behavior together with the fact that when the channel is turned off, all the injected drain current comes out of the gate, is a clear signature of gate breakdown. It shows that gate breakdown limits the maximum drain-source voltage that the device can attain.

In contrast, the physics of breakdown are considerably different at sufficiently low temperatures. We include the Drain-Current Injection scan (Fig. 3, I_D=1 mA/mm, T=80 K) to illustrate the difference. The scan at 80 K shows the appearance of a facet between V_{GS}=-1 V and -4.1 V. At V_{GS}=-1 V, I_G is small and V_{DG} does not reach a plateau, therefore breakdown is channel dominated. As V_{GS} is made more negative, however, corresponding to larger V_{DG}, breakdown becomes gate dominated. The peak V_{DS} of 18.3 V occurs at V_{GS}=-4.1 V, *i.e.*, when breakdown is gate dominated. However, since BV_{DS} is clearly less than BV_{DG} (22.4 V) + V_T, we can see that V_{DS} is limited by channel breakdown.

B. At Breakdown, There Is a High-Field Region in the Drain-Gate Gap

This fact is well known for the AlGaAs/GaAs HEMT [18], [19], and the GaAs MESFET [20], and is probably true for

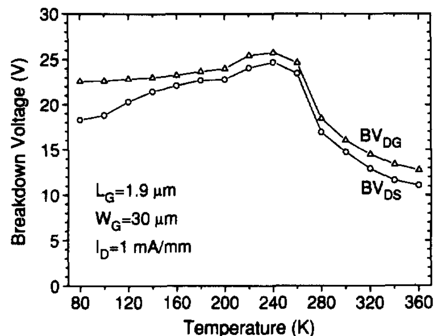

Fig. 4. A plot of BV_{DS} and BV_{DG}, versus temperature. Above T=240 K, BV shows a negative temperature coefficient, and below 240 K, BV shows a small positive temperature coefficient.

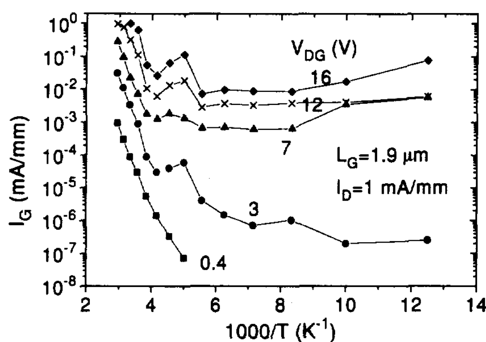

Fig. 5. A semilogarithmic plot of I_G versus 1000/T for several values of V_{DG} from above threshold to breakdown.

HFET's in general. We have confirmed this experimentally for our devices by measurements on a gated Hall-bar structure [21], and by 2-D simulations performed using PISCES-2b [7].

C. Around 300 K, BV_{DS} and BV_{DG} Have a Negative Temperature Coefficient

Fig. 4 is a plot of BV_{DS} and BV_{DG} between T=80 K and 360 K. At higher temperatures (240 K to 360 K) BV_{DS} and BV_{DG} show a negative temperature coefficient, with BV_{DS} decreasing from 24.7 V at 240 K to 11.1 V at 360 K. Above 140 K, BV_{DS} also closely tracks BV_{DG} and the drain-current injection scan behaves like the scan in Fig. 2.

At low temperatures (below 240 K), BV shows a small positive temperature coefficient. Below 140 K, BV_{DS} and BV_{DG} start diverging. This loss of tracking coincides with the appearance of the channel breakdown facet (Fig 3). These facts clearly show that the physics of breakdown are different in the low- and room-temperature regimes.

D. Around 300 K, I_G Is Thermally Activated Approaching Breakdown

We investigated the temperature dependence of the gate current approaching breakdown. Fig. 5 shows a plot of I_G versus 1000/T. Data from the locus of the drain-current injection technique (I_D=1 mA/mm) was used for several values of V_{DG}. Down to about 240 K, I_G drops quickly with temperature. For lower T, I_G plateaus or increases slightly.

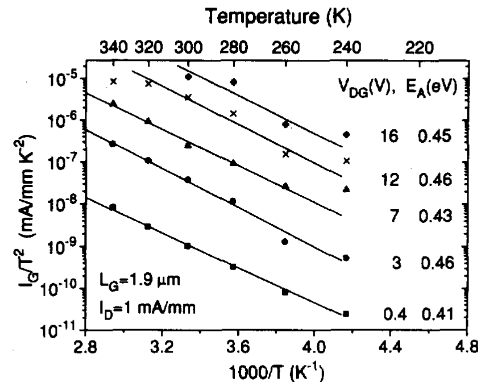

Fig. 6. An Arrhenius plot of I_G/T^2 for V_{DG} steps from 0.4 V to 16 V in the range of temperatures around room temperature. I_G is thermally activated in the breakdown regime.

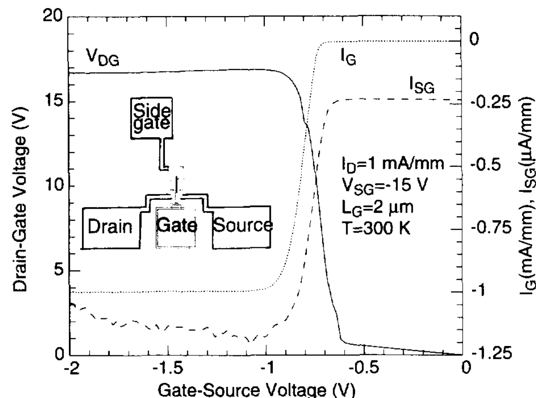

Fig. 7. A drain-current injection scan on a sidegate structure (inset). The rise in I_{SG} corresponds to electron-hole pair generation in the channel when the device enters breakdown.

An Arrhenius plot of I_G/T^2 was generated for several values of V_{DG} around room temperature (Fig. 6). In this temperature regime, the gate current was found to be thermally activated with an activation energy of 0.41–0.46 eV, regardless of V_{DG}.

E. Holes Are Generated During Breakdown

To investigate whether electron-hole pairs are generated during breakdown, we carried out a drain-current injection scan at I_D=1 mA/mm on a sidegate structure (inset of Fig. 7). Sidegating structures have previously been used for detecting holes generated by impact-ionization in the channels of GaAs-based devices [22].

Fig. 7 is a plot of V_{DG}, I_G and sidegate current, I_{SG}, versus V_{GS} at T=300 K for I_D=1 mA/mm. To extract holes, the sidegate was biased at -15 V with respect to the grounded source. As the device is turned off, V_{DS} increases, accompanied by a simultaneous rise (in absolute terms) in both I_G and I_{SG}.

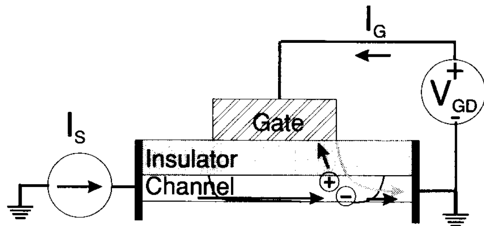

Fig. 8. A schematic showing the biasing circuit for the experiment of Fig. 9. The solid arrows show the flow of source electrons and their generated holes. The shaded arrows show electron flow from the gate to the drain. A detailed cross-sectional structure of the FET is shown in Fig. 1.

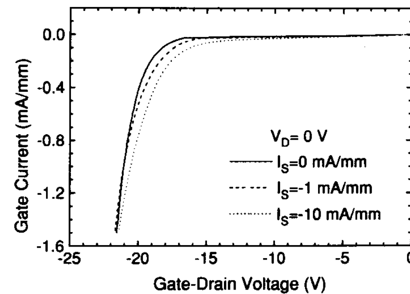

Fig. 9. Gate-drain characteristics taken with I_S=0, -1, -10 mA/mm, showing that source electrons are not responsible for off-state breakdown. The device had L_G=1.9 μm and W_G=30 μm.

The larger I_{SG} is not due to a parasitic drain-sidegate path. We verified this (not shown) by carrying out (a) a two-terminal drain-sidegate measurement (I_S=I_G=0), and (b) drain-current Injection scans at 1 mA/mm, 1.5 mA/mm, and 2 mA/mm. For the two-terminal measurement, I_{SG} became monotonically larger to -0.51 μA/mm when V_{D-SG} was increased up to 35 V. For the drain-current Injection scans, I_{SG} behaved like the scan in Fig. 7, and its peak value grew approximately linearly with the injected drain current from -1.2 μA/mm at I_D=1 mA/mm to -2.4 μA/mm at I_D=2 mA/mm. Since I_{SG} increases with I_D only when a large negative bias is applied to the sidegate, the larger I_{SG} in Fig. 7 can only be due to partial collection of holes generated at breakdown in the HFET.

F. Gate Electrons, Not Source Electrons, Are Responsible for Off-State Breakdown

We have carried out an experiment to assess the relative effects of gate and source electrons in off-state breakdown. The biasing circuit is shown in Fig. 8. Essentially, we have carried out a measurement of gate-drain breakdown with varying amounts of source current. The experiment is motivated by results from the InAlAs/InGaAs HFET literature showing that electron flow through a high-field region in the InGaAs channel will cause impact-ionization [23]–[26]. Some of the generated holes will be collected by the gate and contribute to the gate current [25]–[27]. This flow of source electrons and their generated holes has been illustrated schematically by the solid arrows in Fig. 8. Also illustrated, by the lightly shaded arrow, is the flow of gate electrons.

The experimental data is presented in Fig. 9. First, a two-terminal gate-drain (source floating) scan was carried out. This scan was then repeated with I_S=-1 and -10 mA/mm. The plot shows that these low values of source current do not significantly affect the gate-drain breakdown characteristics.

An increase in I_S, however, does lower BV slightly. We attribute this to impact-ionization caused by electrons flowing through the high-field channel region [23]–[26]. An estimate of the effectiveness of source current in off-state breakdown may be obtained from Fig. 9. At I_S=-10 mA/mm, I_G is -1 mA/mm at V_{GD}=-20.6 V for this particular device. If I_S is now lowered to 0 mA/mm, I_G falls from -1 mA/mm to -0.7 mA/mm. This shows that it takes about 33 times more source current to produce a corresponding effect to the gate current, and demonstrates that source electrons are not responsible for off-state breakdown. The difference could arise because source electrons enter the high-field channel region cold, whereas gate electrons enter hot, as discussed in the next section. As the device turns on, impact-ionization will increase and it is very likely that channel breakdown could limit the maximum V_{DS} [23]–[26]. The study of on-state breakdown is beyond the scope of the present paper, however.

Based on the above set of experiments, the next section outlines a hypothesis for a physical mechanism that can explain our observations, including earlier findings that breakdown is strongly affected by both insulator [9] and channel [10], [12] design.

IV. Proposed Breakdown Hypothesis

The InAlAs/n$^+$–InGaAs HFET consists of a thin undoped wide-bandgap *pseudo*-insulator (InAlAs) and a thin heavily doped narrow-bandgap channel (InGaAs), with substantial ΔE_C between both layers. Breakdown in these devices can potentially result from many effects, such as avalanche multiplication, thermionic or thermionic-field emission across the insulator, electron tunneling through the insulator, or Zener breakdown in the channel [28]. It can also occur by Auger generation [29], which is also referred to as "impact-ionization at a potential step" [30]. In our heterostructure, this could happen as a result of gate electrons crossing from the InAlAs insulator into the InGaAs channel. For $In_{0.40}Al_{0.60}As/In_{0.53}Ga_{0.47}As$, the electrons would suddenly gain an energy of ΔE_c= 0.67 eV [9], almost as large as the bandgap of $In_{0.53}Ga_{0.47}As$ (0.73 eV) [2]. In this case, the presence of even a low electric-field in the insulator can give rise to impact-ionization in the channel.

We have been unable to identify a single process that can satisfactorily explain all our experimental observations. Breakdown cannot be explained by simple impact-ionization. BV shows a negative temperature coefficient (Fig. 4) at room temperature. This is contrary to conventional impact-ionization behavior [31], although qualitatively in agreement with a recent finding showing an anomalous increase in collector multiplication with temperature in an $In_{0.53}Ga_{0.47}As$/InP bipolar transistor [32]. However, light-emission measurements show

that impact-ionization in our HFET is larger at low temperature [33]. The negative temperature coefficient of BV at 300 K therefore does not arise from impact-ionization. Also, since breakdown is from drain to gate, the involvement of the buffer layer is unlikely.

We additionally deduce that room-temperature breakdown is not due to Zener tunneling in the channel. We plotted (not shown) the data of Fig. 6 on a semilogarithmic scale with I_G as the ordinate and $E_G^{3/2}$ as the abscissa. E_G was calculated as a function of temperature using the Varshni equation for $In_{0.53}Ga_{0.47}As$ [2]. Assuming tunneling through a triangular barrier [29], the data should follow approximately a straight line with slope inversely proportional to the electric field. In contrast, we found that the slope of best-fitted lines to the data remained approximately constant for V_{DG} between 0.4 V and 16 V. The absence of Zener tunneling in the channel is consistent with our previous results that for a fixed channel design, BV is much higher for insulators with low InAs-mole fraction [9].

Thermal emission of electrons from the gate into the insulator deserves special consideration, since we found I_G to be thermally activated. Our value of E_A of about 0.4 - 0.5 eV is lower than the Schottky barrier height (ϕ_B) of 0.84 eV reported for Al-$In_{0.41}Al_{0.59}As$ [34]. It is, however, consistent with barrier height measurements of InAlAs under reverse bias conditions [35]. A reduction in the measured barrier height can be attributed to electrons tunneling through the tip of the triangular gate-InAlAs barrier, to weak surface Fermi-level pinning, and in our device, the voltage dropped across the InGaAs capping layer (Fig. 10(a)).

We therefore propose that off-state breakdown at around room temperature is governed by a two-step process involving thermionic-field emission and Auger generation, as shown schematically in Fig. 10(a). First, electrons are injected from the gate edge into the high-field drain-gate region of the insulator by thermionic-field emission. Second, because of the large conduction-band offset and the electric-field in the insulator, they enter the channel hot, and immediately relax their energy through impact-ionization. The electrons flow towards the drain, and the holes can either be extracted by the gate or flow towards the source, where they recombine with electrons. Since this process actually occurs in two-dimensions, with electron injection likely to take place sideways, we have illustrated it on a two-dimensional sketch in Fig. 10(b). The need to assume sideways injection from the drain-edge of the gate arises because we have seen from measurements on a gated Hall-bar structure [21], that the vertical voltage drop in the interior of the channel gets pinned at V_T. Since breakdown does not occur at V_{GD}=V_{GS}=-V_T, this means that the area-leakage component of I_G flowing vertically from gate to channel does not contribute to breakdown. We discuss the implications of the thermionic-field emission/Auger-generation hypothesis in the next section.

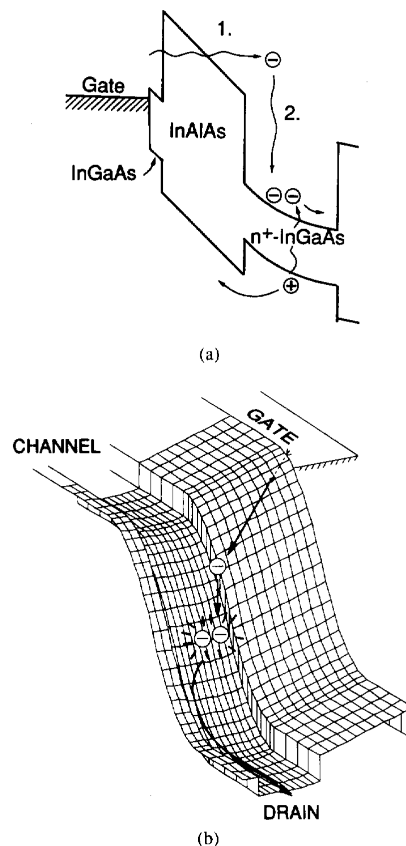

Fig. 10. A schematic showing the combined effect of electron thermionic-field emission and Auger generation. (a) Basic mechanism and (b) two-dimensional drawing.

V. Discussion

The hypothesis presented above qualitatively explains all our other experimental observations to date on the off-state breakdown of the InAlAs/n^+—InGaAs HFET. We have previously found that BV increases with lower InAs mole fraction in the insulator [9] and enhanced channel bandgap (by quantum-size effects in thin channels [12]). The lower-InAs insulator has a larger Schottky barrier height [34], [36], and in our hypothesis, enhances breakdown by suppressing thermionic-emission. An increase in channel bandgap (by quantum size effects) increases breakdown voltage by suppressing impact-ionization [12].

We also found that BV decreases with higher InAs-mole fractions in the channel [10], and higher channel doping [11]. The InAs-rich channel has a lower bandgap [3], therefore impact-ionization will be enhanced. With a higher channel doping, electron emission from the gate is enhanced because the increased electric-field in the insulator and cap results in a lower effective Schottky-barrier height as we discuss below.

To investigate the effect of channel doping, we carried out Drain-Current Injection scans at I_D=1 mA/mm on a sample with N_D=8×10^{18} cm^{-3}. As for lower doping, we found that BV was limited by gate breakdown and I_G was thermally activated between 360 K and 240 K. At 300 K, BV_{DS} and BV_{DG} were 1.6 V and 3.2 V, respectively. I_G/T^2 was plotted

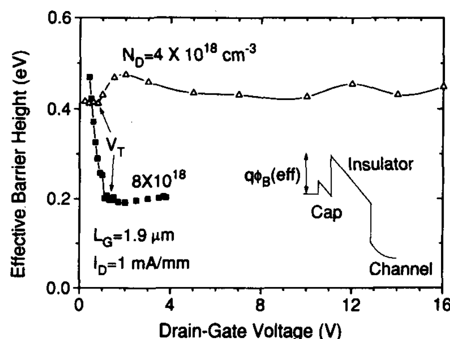

Fig. 11. A plot of the activation energy, E_A, of the gate current at around room temperature versus V_{DG} for the low and heavily doped samples. The data was obtained by use of the drain-current injection technique.

versus 1000/T [21] (not shown), and E_A was extracted in a manner similar to Fig. 6. We also verified, in the same manner as for the sample with lower doping (see discussion above), that simple Zener tunneling is inoperative.

A plot of E_A versus V_{DG} for the heavily-doped sample is shown in Fig. 11. At V_{DG}=0.4 V, E_A is 0.47 eV. As V_{DG} increases, E_A rapidly decreases until threshold (V_T=-1.5 V), beyond which E_A plateaus at approximately 0.2 eV. The E_A versus V_{DG} data for the low-doped sample is also shown in Fig. 11. For low V_{DG}, E_A in both devices is about the same, but at breakdown, E_A is much lower for the heavily-doped sample. This behavior can be explained in the following manner. With heavier channel doping, a given gate voltage results in higher electric field in the insulator and cap layers. This can lower E_A by making the barrier more triangular (Fig. 10(a)), or by shifting the Fermi-level position if the pinning is weak. In this device, an additional (calculated [7]) 0.25 eV of lowering at V_{GS}=V_T (-1.5 V) is due to the voltage dropped across the cap (see inset of Fig. 11). Below threshold, the fringing field becomes important, and will be much higher for a heavily-doped channel because of the smaller penetration of the depletion region into the drain-gate gap.

Sidegate measurements on the heavily-doped sample (not shown) verified that, in spite of the low BV, hole generation still occurs during breakdown. This suggests that the mechanism responsible for breakdown is the same as for the low-doped device, however the strong reduction in E_A causes premature breakdown by increasing I_G.

The hypothesis articulated in section 4 is able to explain the temperature dependence of BV as follows (see Figs. 4–6). At around room temperature, a decrease in T results in lower thermal emission of electrons into the insulator, and BV increases. As T is lowered, electron flow through the insulator becomes increasingly governed by (temperature independent) tunneling. At the same time, impact ionization increases in the channel due to the enhanced mean-free path [31] and the higher electric field (due to the higher BV). Eventually, the two mechanisms balance and BV peaks. This occurs at 240 K for our low-doped device (Fig. 4). Below 240 K, both BV_{DS} and BV_{DG} show a positive temperature coefficient, consistent with impact-ionization [31].

We also investigated the dependence of BV on L_G. Devices with (measured) L_G between 1.9 µm and 53.6 µm were characterized. We found (not shown) that in all cases, V_{DS} was limited by gate breakdown. We could not identify any gate length scaling. BV_{DS} varied between 15.5 V and 19.3 V. The differences in BV were correlated with the (unintentional) differences in gate-drain gaps (measured optically), which were found to range between 1.2 and 1.7 µm. As L_G is shrunk further, it is reasonable to expect that the higher channel electric field will cause channel breakdown to eventually dominate, and BV would decrease for smaller L_G. We have found, however, in a separate study on L_G=0.28 µm MODFET's, that in the off-state, V_{DS} is still limited by gate breakdown [37].

The combined thermionic-emission / Auger-generation process can also explain our previous observations on the effect of *Mesa-sidewall gate-leakage*. Our results show [13], [38] that sidewall-leakage current does not cause premature breakdown, even though it increases the gate current at the onset of breakdown. This is because sidewall-leakage is a parasitic current path from the gate directly into the interior of the gated channel [38]. This means that first, this parasitic contact does not see a large voltage because the interior of the channel is shielded by the gate [21], and second, electrons introduced by the sidewall-contact enter directly into the channel, and as a result they are cold and do not significantly affect breakdown, in a manner similar to the cold electrons originating from the source (see Fig. 9).

The thermionic-emission/Auger-generation process postulated here is also likely to limit BV in InAlAs/InGaAs MODFET's, since in these devices, doping the insulator results in a higher electric field, and therefore a reduced effective barrier to electron emission from the gate. Measurements on state-of-the-art lattice-matched and pseudomorphic MODFET's on InP are consistent with our hypothesis [37].

VI. Conclusion

We have carried out an experimental study of the physics of off-state breakdown in InAlAs/n$^+$—InGaAs HFET's. Our measurements have been presented as a function of temperature, doping, gate-length, and on a sidegate structure. At around room temperature, breakdown is found to be drain-gate limited and BV shows a negative temperature coefficient. Breakdown is hypothesized to be a two step process. First, electrons are injected sideways from the gate edge into the high-field drain-gate region of the insulator by thermionic-field emission. Second, because of the large conduction-band offset and the electric-field in the insulator, they enter the channel hot, and immediately relax their energy through impact-ionization. This combined mechanism explains all our experimental observations to date on breakdown phenomena in InAlAs/n$^+$–InGaAs HFET's.

Acknowledgment

The authors wish to thank Dr. Brian Bennett for sample growth, Prof. C. G. Sodini for the donation of the MMR low-temperature probe station, and Prof. C. G. Fonstad for the use of his MBE system.

REFERENCES

[1] L. D. Nguyen, L. E. Larson, and U. K. Mishra, "Ultra-high-speed modulation-doped field-effect transistors: A tutorial review," *Proc. IEEE*, vol. 80, p. 494, Apr. 1992.

[2] D. K. Gaskill and N. Bottka, "Band-gap determination by photoreflectance of InGaAs and InAlAs lattice matched to InP," *Appl. Phys. Lett.*, vol. 56, no. 13, p. 1269, 1990

[3] S. Adachi, "Material parameters of $In_{1-x}Ga_xAs_yP_{1-y}$ and related binaries," *J. Appl. Phys.*, vol. 53, no. 12, p. 8775, 1982.

[4] P. M. Smith, P. C. Chao, P. Ho, K. H. Duh, and M. Y. Kao, "Microwave InAlAs/InGaAs/InP HEMT's: Status and applications," *Proc. 2nd Int. Conf. on InP and Related Materials*, Denver, CO, Apr. 23-25, p. 39, 1990.

[5] J. H. Burroughes and M. Hargis, "1.3 μm InGaAs MSM photodetector with abrupt InGaAs/AlInAs interface," *IEEE Photonics Technol. Lett.*, vol. 3, no. 6, p. 532, 1991.

[6] J. A. del Alamo and T. Mizutani, "An $In_{0.52}Al_{0.48}As/n^+$-$In_{0.53}Ga_{0.47}As$ MISFET with a heavily doped channel," *IEEE Electron Device Lett.*, vol. EDL-8, p. 534, Nov. 1987.

[7] S. R. Bahl, "Physics and technology of InAlAs/InGaAs heterostructure field-effect transistors," Ph.D. dissertation, 1993, Dept. of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA.

[8] S. R. Bahl, B. R. Bennett, and J. A. del Alamo, "Doubly Strained $In_{0.41}Al_{0.59}As/n^+$-$In_{0.65}Ga_{0.35}As$ HFET with high breakdown voltage," *IEEE Electron Device Lett.*, vol. 14, p. 22, Jan. 1993.

[9] S. R. Bahl, W. J. Azzam, and J. A. del Alamo, "Strained-insulator $in_xAl_{1-x}As/n^+$-$In_{0.53}Ga_{0.47}As$ heterostructure field-effect transistors," *IEEE Trans. Electron Devices*, vol. 38, p. 1986, Sept. 1991.

[10] S. R. Bahl and J. A. del Alamo, "An $In_{0.52}Al_{0.48}As/n^+$-$In_xGa_{1-x}As$ heterostructure field-effect transistor with an In-enriched channel," *Proc. 2nd Int. Conf. on InP and Related Materials*, Denver, CO, p. 100, 1990.

[11] S. R. Bahl, B. R. Bennett, and J. A. del Alamo, "A high-voltage doubly-strained $In_{0.41}Al_{0.59}As/n^+$-$In_{0.65}Ga_{0.35}As$ HFET," *Proc. 4th Int. Conf. on InP and Related Materials*, Newport, RI, Apr. 1992, p. 222.

[12] S. R. Bahl and J. A. del Alamo, "Breakdown voltage enhancement from channel quantization in InAlAs/n^+-InGaAs HFET's," *IEEE Electron Device Lett.*, vol. 13, p. 123, Feb. 1992.

[13] S. R. Bahl and J. A. del Alamo, "Elimination of mesa-sidewall gate-leakage in InAlAs/InGaAs heterostructures by selective sidewall recessing," *IEEE Electron Device Lett.*, vol. 13, p. 195, Apr. 1992.

[14] S. R. Bahl and J. A. del Alamo, "A new drain-current injection technique for the measurement of off-state breakdown voltage in FET's," *IEEE Trans. Electron Devices*, vol. 40, p. 1558, Aug. 1993.

[15] P. Saunier, R. J. Matyi, and K. Bradshaw, "A double-heterojunction doped-channel pseudomorphic power HEMT with a power density of 0.85 W/mm at 55 GHz" *IEEE Electron Device Lett.*, vol. 9, p. 397, Aug. 1988.

[16] P. Saunier, private communication, 1991.

[17] J. B. Boos and W. Kruppa, "InAlAs/InGaAs/InP HEMT's with high breakdown voltages using double-recess gate process," *Electron. Lett.*, vol. 27, no. 21, p. 1909, 1991.

[18] F. Temcamani, Y. Crosnier, D. Lippens, and G. Salmer, "Modeling and experimental study of breakdown mechanisms in multichannel AlGaAs/GaAs power HEMT's," *Microwave and Optical Technol. Lett.*, vol. 3. no. 6, p. 195, 1990.

[19] H-F. Chau, D. Pavlidis, and K. Tomizawa, "Theoretical analysis of HEMT breakdown dependence on device design parameters," *IEEE Trans. Electron Devices*, vol. 38, p. 213, Feb. 1991.

[20] T. M. Barton and P. H. Ladbroke, "The role of the device surface in the high voltage behavior of the GaAs MESFET's," *Solid State Electron.*, vol. 29, no. 8, p. 807, 1986.

[21] S. R. Bahl and J. A. del Alamo, "Physics of breakdown in InAlAs/n^+-InGaAs heterostructure field-effect transistors," *Proc. 5th Int. Conf. on InP and Related Materials*, Paris, France, Apr. 1993, p. 243.

[22] T. Yokoyama and A. Tamura, "The substrate current by impact ionization in GaAs MESFET's,"*Inst. Phys. Conf. Series*, no. 120, p. 239, 1991.

[23] G. G. Zhou, A. Fischer-Colbrie, J. Miller, Y. C. Pao, B. Hughes, L. Studebaker, and J. S. Harris, Jr., "High output conductance of InAlAs/InGaAs/InP MODFET due to weak impact ionization in the InGaAs channel," *Int. Electron Devices Meet., Techn. Dig.*, p. 247, 1991.

[24] C. Heedt, F. Buchali, W. Prost, D. Fritzche, H. Nickel, and F. J. Tegude, "Characterization of impact-ionization in InAlAs/InGaAs/InP HEMT structures using a novel photocurrent-measurement technique," paper presented at *5th Int. Conf. on InP and Related Materials*, Paris, France, 1993, Conf. Proc., p. 247.

[25] F. Buchali, C. Heedt, W. Prost, I. Gyuro, and F. J. Tegude, "Analysis of gate leakage on MOVPE grown InAlAs/InGaAs/InP-HFET," *Microelectronic Engineering*, vol. 19, p. 401, 1992. Paper presented at *Europe. Solid-State Device Res. Conf. (ESSDERC)*, Sept. 1992, Leuven, Belgium.

[26] D. J. Newson, R. P. Merrett, and B. K. Ridley, "Control of gate leakage in InAlAs/InGaAs HEMT's," *Electronics Lett.*, vol. 27, no. 17, p. 1592, 1991.

[27] C. Canali, A. Paccagnella, P. Pisoni, C. Tedesco, P. Telaroli, and E. Zanoni, "Impact ionization phenomena in AlGaAs/GaAs HEMT's," *IEEE Trans. Electron Devices*, vol. 38, p. 2571, Nov. 1991.

[28] D. J. Newson, R. P. Merrett, M. Lee, and E. G. Scott, "Control of gate leakage in AlInAs-insulator HIGFET's," *Electron. Lett.*, vol. 25, no. 25, p. 1728, 1989.

[29] S. Tiwari, *Compound Semiconductor Device Physics*. New York: Academic, 1992.

[30] K. Brennan, T. Wang, and K. Hess, "Theory of electron impact ionization including a potential step: Application to GaAs-AlGaAs," *IEEE Electron Device Lett.*, vol. 6, p. 199, Apr. 1985.

[31] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. New York: Wiley, 1981.

[32] D. Ritter, R. A. Hamm, A. Feygenson, and M. B. Panish, "Anomalous electric field and temperature dependence of collector multiplication in InP/$Ga_{0.47}In_{0.53}As$ heterojunction bipolar transistors," *Appl. Phys. Lett.*, vol. 60, no. 25, p. 3150, 1992.

[33] G. Berthold, E. Zanoni, M. Manfredi, M. Pavesi, C. Canali, J. A. del Alamo, and S. R. Bahl, "Electroluminescence and gate current components of InAlAs/InGaAs HFETs," to be presented at *Device Research Conf.*, 1994.

[34] K. Imanishi, T. Ishikawa, and K. Kondo, "N-$In_xAl_{1-x}As$/$In_{0.53}Ga_{0.47}As$ pseudomorphic selectively doped heterostructures with improved Schottky characteristics," *Inst. Phys. Conf. Series No. 106*, p. 637, 1990

[35] P. D. Hodson, R. H. Wallis, J. I. Davies, J. R. Riffat, and A. C. Marshall, "Characteristics of Schottky diodes on $Al_xIn_{1-x}As$ grown by MOCVD," *Semicond. Sci. Technol.*, vol. 3, p. 1136, 1988.

[36] C. L. Lin, P. Chu, A. L. Kellner, and H. H. Wieder, "Composition dependence of Au/$In_xAl_{1-x}As$ Schottky barrier heights," *Appl. Phys. Lett.*, vol. 49, no. 23, p. 1593, 1986.

[37] S. R. Bahl, J. A. del Alamo, J. Dickmann, and S. Schildberg, "Off-state breakdown in InAlAs/InGaAs MODFET's," to be published in *IEEE Trans. Electron Devices*.

[38] S. R. Bahl, M. H. Leary, and J. A. del Alamo, "Mesa-sidewall gate-leakage in InAlAs/InGaAs HFET's," *IEEE Trans. Electron Devices*, vol. 39, p. 2037, Sept. 1992.

Sandeep R. Bahl (S'84–M'93) received the B.S. degree (summa cum laude) in electrical engineering from Rensselaer Polytechnic Institute, Troy, NY, in 1985, and the M.S. and Ph.D. degrees in electrical engineering from MIT, Cambridge, MA, in 1988 and 1993, respectively.

From 1986 to 1988 he designed and fabricated a Si-power MOSFET for a 10 MHz dc-dc converter. From 1988 to 1993 he carried out research on the physics and technology of the InAlAs/n^+—InGaAs HFET. He is currently at Hewlett-Packard Laboratories, Palo Alto, CA, where he is responsible for the development of next-generation HBT technology. His current research interests include the physics and technology of compound semiconductor transistors and their application to high-speed circuits.

Dr. Bahl received the Rensselaer International Scholarship during his undergraduate years. He received the Best Student Paper Award at the Indium Phosphide and Related Materials Conference in 1993 for his work on the physics of breakdown in InAlAs/n^+—InGaAs heterostructure field-effect transistors. He is a member of Eta Kappa Nu and Tau Beta Pi.

Jesús del Alamo (S'79–M'85) received the telecommunication engineer degree from the Polytechnic University of Madrid in 1980, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University in 1983 and 1985.

From 1977 to 1981 he was a Research Assistant at the Institute of Solar Energy of the Polytechnic University of Madrid, where he worked on silicon solar cells. From 1985 to 1988 he was a Research Engineer with NTT LSI Laboratories in Atsugi, Japan, where he conducted research on heterostructure field-effect transistors (HFET's) based on InP, InAlAs, and InGaAs. In 1988 he joined the Department of Electrical Engineering and Computer Science at MIT as an Assistant Professor and was promoted to Associate Professor in 1991. His research interests include high-performance HFET's and metal-semiconductor-metal photodiodes based on compound semiconductors that contain In, and novel quantum-effect devices with one-dimensional electron confinement.

Dr. del Alamo held the ITT Career Development Professorship at MIT from 1990 to 1993. In 1991 he received the Presidential Young Investigator Award by NSF. In 1992 he was awarded the Baker Memorial Award for Excellence in Undergraduate Teaching at MIT. In 1993 he received the H. E. Edgerton Junior Faculty Achievement Award. He is a member of the American Physical Society and the Japanese Society of Applied Physics.