Impact Ionization in InAlAs/InGaAs HFET's

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Abstract—**The presence of an energy barrier to the transfer of holes from the channel to the gate electrode of InAlAs/InGaAs HFET's prevents the gate current from being a reliable indicator of impact ionization. Consequently, we have used a specially designed sidegate structure to demonstrate that due to the narrow bandgap of InGaAs, impact ionization takes place in the channel of these devices under normal operating conditions. The ionization coefficient was found to follow a classic exponential dependence on the inverse electric field at the drain end of the gate, for over three orders of magnitude.**

IMPACT ionization in the channel of InAlAs/InGaAs Heterostructure Field-Effect Transistors (HFET's) on InP is a severe problem that seriously limits their use in many applications [1]. A high impact ionization rate in the narrow bandgap InGaAs channel is blamed for the poor on- and off-state breakdown voltage [2], [3], the high output conductance at low drain currents [4], excessive shot noise in the drain current [5], and the large gate leakage current [5]–[8] observed in InAlAs/InGaAs HFET's. A detailed understanding of impact ionization is therefore required before the outstanding properties of InAlAs/InGaAs HFET's can be fully exploited [1].

Recently, a method originally proposed by Hui *et al.* [9] has become widespread in the study of impact ionization phenomena in GaAs MESFET's [10] and AlGaAs/GaAs HEMT's [11]. In this technique and in analogy with the substrate current in Si MOSFET's [9], the gate current is used to monitor hole generation in the high-electric field region of the device. Using this method, it has been verified that the ionization coefficient, α_n, in GaAs MESFET's and AlGaAs/GaAs HEMT's follows theoretical expectations over many orders of magnitude [10], [11]. This is essential information for accurate device modeling. No such studies have been carried out for InAlAs/InGaAs HFET's on InP where impact ionization is considerably more prevalent than in GaAs-based devices. Our paper addresses this issue.

The method of Hui *et al.* [9] requires that the holes generated in the high-field region of the device escape through the gate. This is not entirely possible in the InAlAs/InGaAs system where the valence-band discontinuity for holes is substantial, about 0.2 eV for the compositions lattice-matched to InP [12]. Recently, Yokoyama and Tamura showed that a negatively biased sidegate is an effective collector of impact-ionized holes in GaAs MESFET's [13]. We have used this observation to experimentally study impact ionization in InAlAs/InGaAs HFET's on InP.

The device structure utilized in this work has been described in [14]. It consists of a 300 Å undoped $In_{0.41}Al_{0.59}As$ strained pseudoinsulator layer and a 100 Å heavily doped (8×10^{18} cm^{-3} Si) $In_{0.53}Ga_{0.47}As$ active channel, latticed-matched to InP. The fabrication details for these HFET's have been reported in [15]. An important feature of the process is mesa sidewall isolation which was performed as described in [16]. All the measurements reported here were made on a sidegate structure which consists of an HFET ($L_G = 2$ μm and $W_G = 30$ μm) with a sidegate centered relative to it, and located parallel to the direction of current flow, at a distance of 15 μm from the device. The sidegate, itself, has an ohmic contact deposited on a 40 μm $\times$ 15 μm mesa island of the heterostructure material. The mesa in the region between the HFET and sidegate contact is etched down to the substrate. By applying a sufficient negative bias to the sidegate contact, it is possible to remove a small fraction of the holes that might be produced in the HFET channel as a result of impact ionization [3]. For this work, the sidegate was maintained at -20 V with respect to the source.

Fig. 1 shows typical drain current (I_D), gate current (I_G) and sidegate current (I_{SG}) vs. V_{GS} characteristics as a function of V_{DS}. For $V_{DS} < 1.4$ V, the I_G plot reflects simple Schottky-diode behavior, while I_{SG} stays featureless and small in magnitude ($I_{SG0} \simeq -11$ nA) over the entire V_{GS} range. For $V_{DS} > 1.4$ V, on the other hand, as soon as the device turns on (at $V_{th} \simeq -1.4$ V), a prominent negative-valued hump appears in both I_G and I_{SG}; the height of which is found to increase with V_{DS}. The negative nature of this hump in the I_G and I_{SG} plots suggests that holes are being removed from the HFET channel via the gate [17] and the sidegate [13] contacts, respectively. This idea is supported by the observation (not shown here) that I_{SG} stays featureless for all values of both V_{DS} and V_{GS} if the sidegate is maintained at a positive potential relative to the source.

We analyzed I_{SG} on the basis of the model proposed by Hui *et al.* for impact ionization in GaAs MESFET's [9]. Since in the case of MESFET's the generated holes are extracted by the gate ($I_G \simeq I_{\text{hole}}$), Hui *et al.* plotted semilog graphs of $|I_G/I_D|$ vs. $1/(V_{DS} - V_{DSsat})$ and demonstrated that, as expected theoretically [18], α_n follows the classic relationship:

$$\alpha_n \propto e^{-\frac{\beta}{\mathcal{E}_{\max}}} = e^{-\frac{\beta L_{\text{eff}}}{(V_{DS}-V_{DSsat})}} \quad (1)$$

where β is a constant, L_{eff} is the effective length over which ionization occurs and $\mathcal{E}_{\max}$is the peak electric field in this region.

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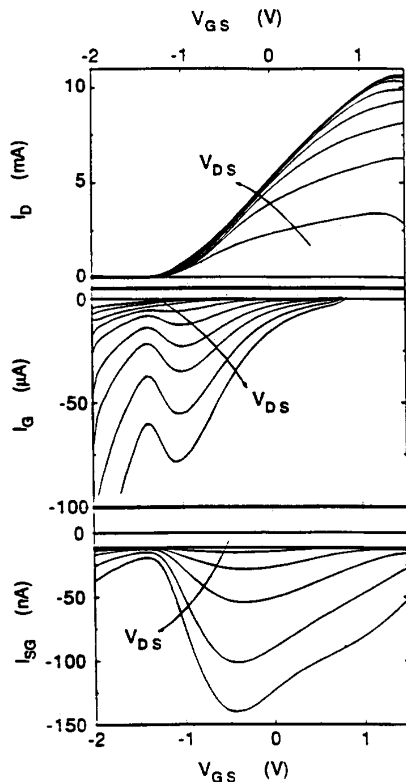

Fig. 1. Typical I_D, I_G, and I_{SG} vs. V_{GS} characteristics for a sidegate HFET structure for $V_{DS} = 0.4, 0.8, 1.2, 1.6, 2, 2.4, 2.8, 3.2$, and 3.6 V.

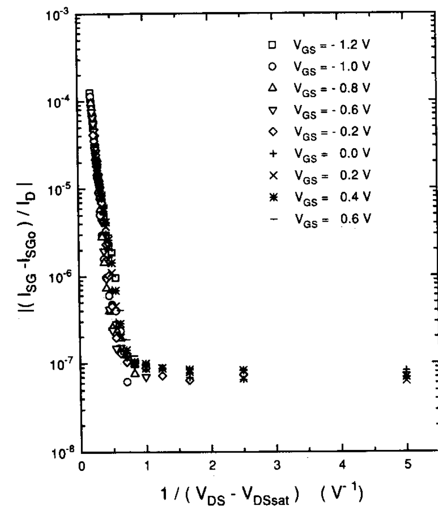

Fig. 2. Semilog graph of $|(I_{SG} - I_{SG0})/I_D|$ vs. $1/(V_{DS} - V_{DSsat})$ for various values of V_{GS}. The straight line observed for low values of $1/(V_{DS} - V_{DSsat})$ confirms the occurrence of impact ionization in the device.

In the case of HFET's, however, there is a barrier to hole extraction by the gate electrode, as discussed below. Furthermore, conventional gate-drain leakage and real-space transfer of electrons results in $I_G \neq I_{\text{hole}}$, and the method of Hui *et al.* fails. To overcome these shortcomings, we used I_{SG} in our analysis. Fig. 2 shows a semilog graph of $|(I_{SG} - I_{SG0})/I_D|$ vs. $1/(V_{DS} - V_{DSsat})$ for our device, where we have taken $V_{DSsat} = V_{GS}$ (a valid assumption in the velocity saturation regime; for $V_{GS} \succeq -0.6$ V). For low values of $1/(V_{DS} - V_{DSsat})$, the data in Fig. 2 approaches a common straight line which is independent of V_{GS}. This clearly indicates that impact ionization is taking place in the device and that the process is well depicted, over at least three orders of magnitude, by the simple theory presented by Hui *et al.* [9].

The bell-shaped structure seen in the I_{SG} and I_G plots can now be explained easily [17]. The ionization process depends on both I_D and the accelerating electric field, $\mathcal{E}_{\max}$, at the drain end. These, however, move in opposite sense relative to each other with V_{GS}. Immediately after the device turns on, for example, $\mathcal{E}_{\max}$ is high and the electron supply proves to be the bottleneck for impact ionization. This causes both I_{SG} and I_G to increase towards more negative values as the gate bias is raised. At larger values of V_{GS}, on the other hand, I_D increases but $\mathcal{E}_{\max}$ drops. The exponential relationship between α_n and $\mathcal{E}_{\max}$ then begins to dominate and brings the impact ionization rate down.

Moreover, I_G peaks at a more negative value of V_{GS} than I_{SG}. This is because as V_{GS} is increased to more positive values, the gate electrode loses its ability to extract holes from the HFET channel. The sidegate, on the other hand, is maintained at a constant negative bias over the entire V_{GS} range and, therefore, suffers from no such problem. Consequently, if the method of Hui *et al.* is applied to I_G instead of I_{SG}, it fails to display the classic behavior seen in Fig. 2.

This fact is best understood by considering the energy band diagrams at the source end of the intrinsic device at different gate biases. Even though the holes are produced in the gate-drain gap, they most probably get swept towards the source end of the channel by the lateral electric field before some of them can escape via the gate electrode. Fig. 3(a) shows the band diagram for $V_{GS} < 0$. In this case, the vertical electric field points from the channel towards the gate. As a result, some of the holes that are produced during impact ionization can get across the InAlAs barrier layer and are collected at the gate. As V_{GS} is made more positive, the bands straighten out and the vertical field drops. Hence, at flat-band, Fig. 3(b), there is no field to aid hole collection by the gate. When V_{GS} is increased beyond flat-band, the field changes direction, Fig. 3(c), and hole transfer to the gate gets suppressed completely. Our experimental results substantiate these arguments (see Fig. 1). In fact, as V_{GS} is raised beyond the peak of the hump in I_G (at $V_{GS} \simeq -1$ V), the gate current decays nearly linearly with an extrapolation to zero at about $V_{GS} = 0.2$ V, for all values of $V_{DS} > 1.4$ V. This is approximately the flat-band voltage of the structure, which gives credibility to our assumption that the holes escape to the gate mainly on the source end of the channel.

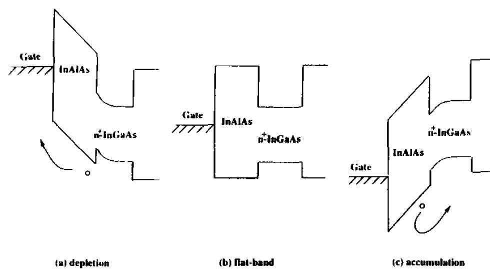

Fig. 3. Band diagrams for the source end of the intrinsic device for: (a) depletion, (b) flat-band, and (c) accumulation, indicating the effect of the barrier between the gate and channel on hole extraction by the gate electrode.

The sidegate current, on the other hand, is not affected by the presence of the gate-channel barrier, and therefore extrapolates to I_{SG0} at a constant value of $V_{DG} \simeq 1.4$ V, independent of V_{GS} (see Fig. 1). This value is consistent with the minimum V_{DS}, also 1.4 V as stated earlier, that is required for the onset of impact ionization just beyond threshold.

In conclusion, by examining the sidegate current, we have demonstrated that impact ionization takes place in the channel of InAlAs/InGaAs HFET's under normal operating conditions. Our study reveals a well behaved exponential relationship between the impact ionization coefficient and the inverse electric field at the drain end of the gate.

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