WP4

A Submicron InAlAs/n$^+$-InP HFET with Reduced Impact Ionization

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Abstract

We have fabricated submicron InAlAs/n$^+$-InP HFETs that employ an InP channel layer to eliminate impact ionization and thus reduce gate leakage, decrease drain conductance, and improve breakdown voltage. Under typical bias conditions, our L_g = 0.8 μm devices achieve a low g_d of 5.1 mS/mm, leading to a voltage gain of 25, while gate current never exceeds 17 $\mu A/mm$. This is approximately 60 times lower gate current than for typical InAlAs/InGaAs HEMTs, including edge-isolated devices. Off-state drain-source breakdown voltage is about 10 V at 1 mA/mm and *increases* as the device is turned on, confirming that impact ionization is negligible. Our results on a lattice-matched structure suggest considerable potential for optimization by using a strained insulator layer to reduce gate leakage and to improve breakdown still further.

Introduction

InAlAs/InGaAs HFETs have shown promise as candidates for use in long wavelength optoelectronic receivers [1]. Despite their outstanding frequency response, however, InAlAs/InGaAs HFETs are vulnerable to impact ionization occurring at the drain end of the narrow bandgap channel even under normal biasing conditions [2]. This phenomenon brings down voltage gain (a_v) through increased g_d, lowers the drain-source breakdown voltage (BV_{DS}), and, in applications to optoelectronic receivers, degrades sensitivity through excess gate leakage noise [2-5]. Previous studies have explored the use of strained barrier layers to reduce the multiplication hole current into the gate [6-7] as well as the engineering of the cap layer over the drain-gate gap to lower the peak electric field in the drain [8]. The performance tradeoffs associated with these methods are still unclear.

To date, however, there has been little work exploring the use of the wide bandgap material InP rather than InGaAs as the channel layer in optoelectronic devices. InP is an attractive material for use in devices targeted at high-power telecommunications applications because of its exceptional breakdown field and high peak electron velocity. In addition, the existence of highly selective etchants for InGaAs and InAlAs over InP make InP an ideal etch-stop layer for use in recessed-gate and recessed-ohmic-contact fabrication processes. InP-channel HFETs have recently been demonstrated in both doped-channel [9] and modulation-doped [10] designs, achieving an excellent combination of high transconductance, current density, power density, and breakdown voltage.

This work examines the potential of submicron InAlAs/n$^+$-InP HFETs for optoelectronic applications. In particular, we study the relative magnitude of impact ionization in this device structure. The heterostructure design, first demonstrated in $L_g \cong 2$ μm devices in [9], relies on an InP layer as the active channel of the device. We find that the wide bandgap channel of InP eliminates any discernible impact ionization, resulting in low gate leakage current combined with low g_d, high a_v, and high BV_{DS}.

Experiment

We have fabricated 0.8 μm × 200 μm devices using the MOCVD-grown heterostructure of Fig. 1. The heterostructure consists, from top to bottom, of a 500 Å $In_{0.53}Ga_{0.47}As$ cap ($N_D = 1 \times 10^{19}$ cm^{-3}), a 50 Å undoped InP etch-stop layer, a 250 Å undoped $In_{0.52}Al_{0.48}As$ pseudoinsulator, a 100 Å n$^+$-InP channel ($N_D = 5 \times 10^{18}$ cm^{-3}), a 100 Å undoped InP subchannel, and a 1000 Å undoped $In_{0.52}Al_{0.48}As$ buffer/electron confinement layer grown on a S.I. InP substrate.

Fabrication begins with a mesa wet etch, followed by Ni/Au/Ge ohmic contact deposition, patterning, and rapid thermal annealing (390° C, 15 s). After gate photolitho-

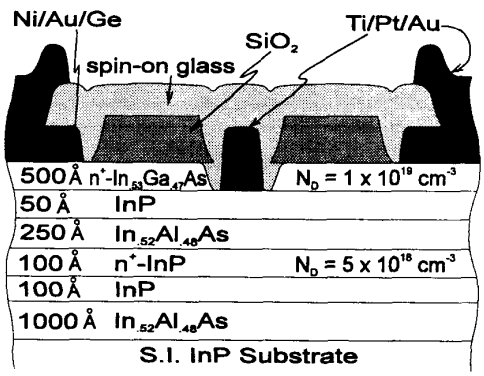

Figure 1: Schematic cross-section of the InAlAs/n$^+$-InP HFET.

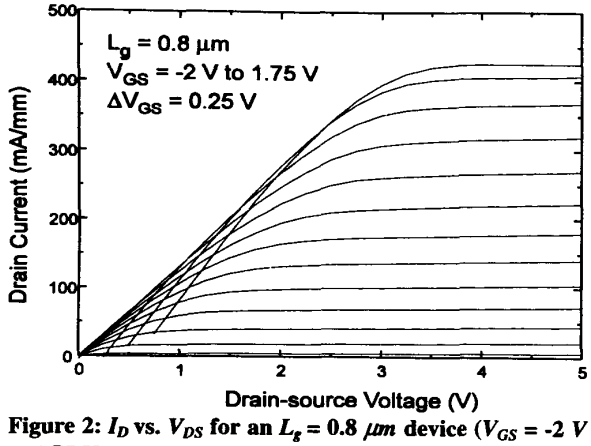

Figure 2: I_D vs. V_{DS} for an L_g = 0.8 μm device (V_{GS} = -2 V to 1.75 V).

graphy, the n^+-InGaAs cap is selectively etched down to the InP etch-stop layer with 1:10:220 H_2SO_4:H_2O_2:H_2O etchant just prior to the deposition and lift-off of Ti/Pt/Au gates. Precise timing of the etch or iterative monitoring of I_D is obviated by the better than 300:1 selectivity of this etchant for InGaAs on InP, which we have verified in etch tests. The resulting increased reliability and threshold voltage control is essential for circuit fabrication. Finally, we conclude fabrication with spin-on glass intermetal dielectric deposition and patterning (necessary for making circuits) followed by Ti/Pt/Au pad/second-level metal formation.

Results and Discussion

Figs. 2 and 3 show I_D and g_m for a typical device (4.8 μm source-drain spacing). Peak extrinsic and intrinsic values of g_m are typically 200 mS/mm and 370 mS/mm, respectively, for $V_{DS} \geq 4$ V. The thin, heavily-doped channel and the use of an undoped insulator result in g_m with less than 10% frequency dispersion from DC to 3 GHz and sustained over a broad V_{GS} swing, contributing to a large typical maximum

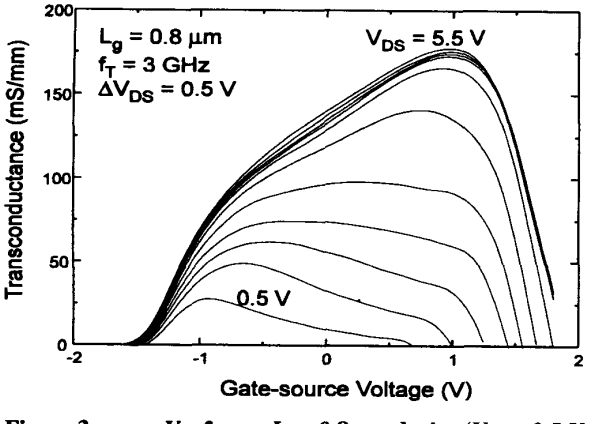

Figure 3: g_m vs. V_{GS} for an L_g = 0.8 μm device (V_{DS} = 0.5 V to 5.5 V).

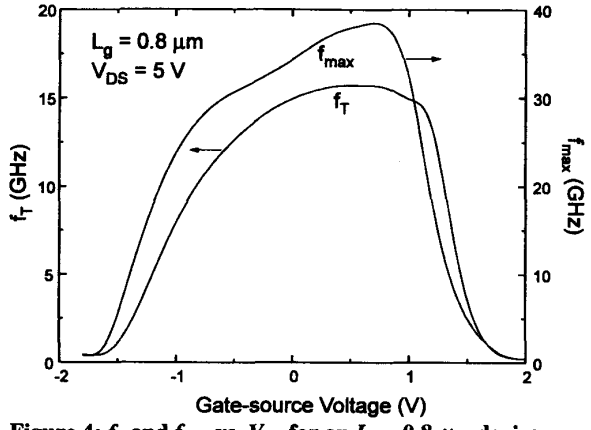

Figure 4: f_T and f_{max} vs. V_{GS} for an L_g = 0.8 μm device (V_{DS} = 5 V).

drain current of 450 mA/mm. Fig. 4 shows the behavior of f_T and f_{max} vs. V_{GS}, with f_T and f_{max} achieving peak values of 15 GHz and 38 GHz, respectively. We have examined the scaling behavior of g_{m0} and f_T with L_g in the range between 0.6 μm and 5 μm. We find that our devices are governed by mobility-limited transport for L_g > 1.8 μm and by velocity-saturation-limited transport for shorter gate lengths. Specifically, we extract a channel electron mobility of 1750 $cm^2/V\text{-}s$ and a saturation velocity of 1×10^7 cm/s.

Since low gate leakage is particularly important in high sensitivity optoelectronic receivers, we plot I_G vs. V_{GS} for several values of V_{DS} for a typical device in Fig. 5. Despite the low ΔE_c (0.27 eV - 0.39 eV [11,12]) of the InAlAs/InP system, we find that $|I_G|$ remains less than 17 $\mu A/mm$ in the useful V_{GS} range between -1 V and 1 V, at a typical V_{DS} of 4 V. This value is almost 60 times lower than for reported lattice-matched InGaAs HEMTs operated at a lower V_{DS} of 2 V (including devices with edge isolation) [6,7,13,14]. Significantly, the curves also lack the characteristic negative

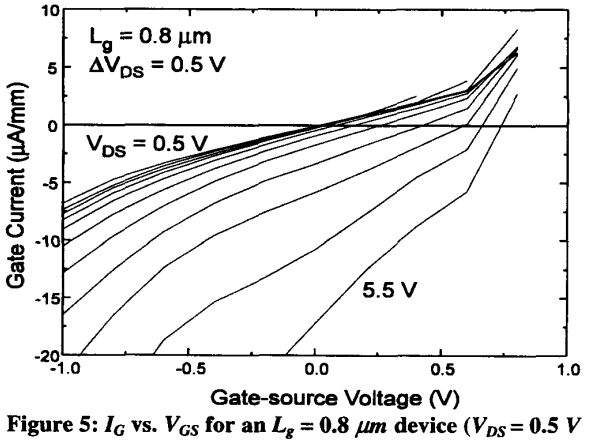

Figure 5: I_G vs. V_{GS} for an L_g = 0.8 μm device (V_{DS} = 0.5 V to 5.5 V).

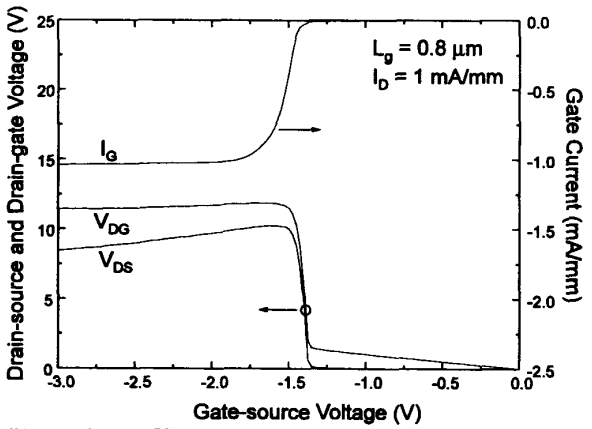

Figure 6: V_{DS}, V_{DG}, and I_G vs. V_{GS} at I_D = 1 *mA/mm* for an L_g = 0.8 *μm* device.

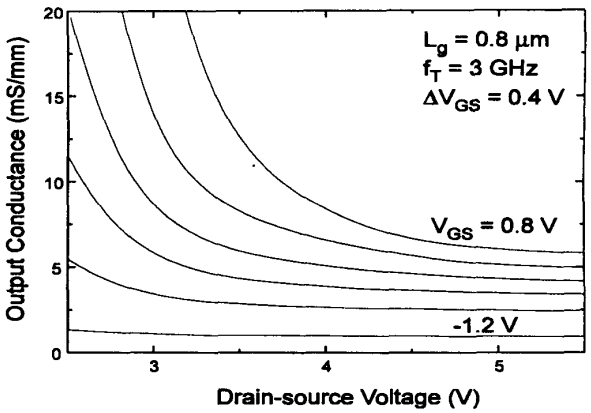

Figure 8: g_d vs. V_{DS} for an L_g = 0.8 *μm* device (V_{GS} = -1.2 *V* to 0.8 *V*).

hump in I_G which is the signature of impact ionization [6,7,13,14], proving that these devices are indeed completely free of this deleterious effect.

The behavior of drain-source and drain-gate breakdown voltage is another test for the presence of impact ionization. In Fig. 6, we plot both V_{DS}, V_{DG}, and I_G vs. V_{GS} at I_D = 1 *mA/mm* using the Drain-Current Injection technique described by Bahl [15]. This figure indicates drain-source and drain-gate breakdown voltages (BV_{DS} and BV_{DG}) of 10 *V* and 12 *V*, respectively. The fact that breakdown in our device occurs at constant V_{DG} means that breakdown is gate-drain limited. This behavior, and the values of BV_{DS} and BV_{DG}, do not depend on gate length in the examined range from 0.8 *μm* to 2 *μm* (within statistical variation).

The role of impact ionization in breakdown is best studied by examining the I_D dependence of the three-terminal drain-source breakdown voltage as the device is turned on. We plot I_D vs. V_{DS} in Fig. 7 for a typical device as V_{GS} is

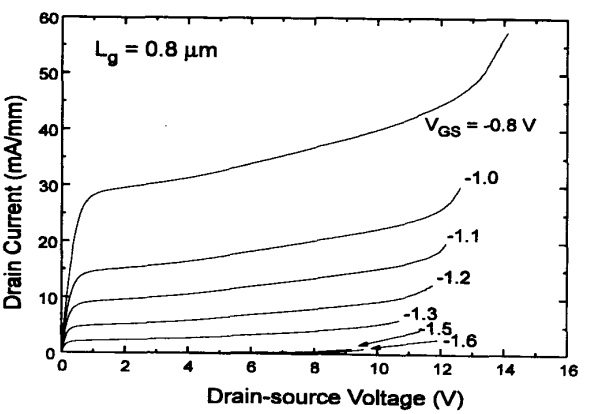

Figure 7: I_D vs. V_{DS} for an L_g = 0.8 *μm* device showing I_D dependence of drain-source breakdown above threshold.

varied from just below to moderately above threshold. Since I_D increases with increasing V_{GS}, the drain-source breakdown voltage should degrade with rising V_{GS} if it involves impact ionization in the channel. Instead, the breakdown voltage *improves* as the device is turned on, contrary to the behavior of InAlAs/InGaAs HFETs and indicating that channel impact ionization is negligible. This behavior is consistent with breakdown being set by thermionic field-emission of electrons from the gate, over the insulator, and into the channel. As a result of low impact ionization and the thin-channel design, our devices display very low g_d as illustrated in Fig. 8 (for 3 *GHz*). This yields good values for a_v despite only modest values for g_m. At a typical bias of V_{GS} = 0 *V* and V_{DS} = 4 *V*, for example, our devices simultaneously achieve g_m = 133 *mS/mm*, g_d = 5.1 *mS/mm*, a_v = 26, and I_G = 3.3 *μA/mm*. At this bias, our devices also achieve an f_T of 12 *GHz* and an f_{max} of 35 *GHz*, sufficient for multigigabit applications. Additionally, pulse measurements show less than 5 % gate and drain lag.

Conclusion

In summary, we have fabricated submicron InAlAs/n^+-InP HFETs which, by virtue of their InP channel layer, are completely free of impact ionization. The absence of impact ionization results in very low I_G (and thus potentially low input noise in optoelectronic receiver applications), low g_d, excellent voltage gain, and high breakdown voltage. Our results on a lattice-matched structure suggest great potential for optimization by using a strained insulator layer to reduce gate leakage and to improve breakdown still further.

Acknowledgements

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