A Novel Analog-to-Digital Conversion Architecture Using Electron Waveguides

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***Abstract*—We have demonstrated a novel analog-to-digital (A/D) conversion architecture based on the quantized conductance of electron waveguides. In our scheme, a dual electron waveguide (DWG) device implements a binary quantizer and encoder for one significant bit of resolution. The conductance values of the on and off states in the binary code are $2e^2/h$ and zero, respectively. By cascading multiple DWG devices, higher order significant bits can be attained. In this paper, we demonstrate the first significant bit and the second significant bit of our analog-to-digital conversion architecture using a DWG device fabricated in an AlGaAs/GaAs modulation-doped heterostructure.**

I. Introduction

MUCH of the excitement behind quantum-effect devices can be attributed to the rich features borne out in their electrical characteristics [1]. Such features provide an inherent advantage, in terms of functionality, over the simple on/off properties of conventional transistors. This could potentially lead to more efficient circuits which require only a small number of active components [2]. In this work, we help establish the feasibility of such concepts by exploiting the unique "quantized conductance" of electron waveguide devices to implement a novel analog-to-digital (A/D) conversion architecture.

An electron waveguide is essentially a one-dimensional (1D) channel through which electrons travel without scattering [3]. The propagation modes of the electron waveguide correspond to the 1D subbands in the channel. The contribution to the waveguide conductance from each mode, or subband, is equal to a fundamental constant $2e^2/h$ [4]. This results from the cancellation of the energy dependence in the 1D density of states with that of the electron velocity. Therefore, the total conductance of an electron waveguide is simply the summation of all the $2e^2/h$ contributions from the occupied modes, i.e., from the subbands below the Fermi level.

The most common way to implement an electron waveguide is by using a high mobility split-gate transistor configuration [5], [6], conceptually shown in Fig. 1. In such a scheme, a split-gate pattern is fabricated on top of a normally-on modulation-doped heterostructure. By applying a sufficiently negative split-gate bias, the two-dimensional electron gas (2DEG) can be depleted underneath the gates, leaving a narrow conducting channel in between. If the channel width is comparable to the electron wavelength (~ 500 Å), then electrons are free to move only in one direction. If inelastic and elastic scattering are suppressed through low-temperature operation and the use of high-purity material, then the 1D channel becomes a true electron waveguide [3].

The unique aspect of a split-gate scheme is that the electrons in the channel can be depleted through the fringing fields of the gate bias. We are therefore able to sweep the 1D subbands through the Fermi level by modulating the split-gate bias. Stated in a different way, through an external bias we can control the number of occupied modes in our electron waveguide. Each time a subband is swept through the Fermi level, the current changes by $(2e^2/h)V_{DS}$, with the result being a "staircase" structure in the I–V characteristics [3], [7], [8], shown in Fig. 2 for one of our devices [9]. This is referred to as the quantized conductance of an electron waveguide.

In the electron waveguide regime, the constant height of each conductance step is independent of device length and, to first order, the specific material in which the channel is implemented. Such a universal feature is very attractive from a circuit standpoint. In fact, it is most amenable for the implementation of an analog-to-digital conversion architecture. This is the topic of this work.

The basic device element in our A/D circuits is a dual electron waveguide (DWG) device [10], shown conceptually in Fig. 3. This device consists of two electron waveguides which are located right next to one another. Three gates are patterned on the surface of the modulation-doped structure; two side-gates which are used to control the number of occupied modes in each respective waveguide and a middle-gate which is used to separate and isolate the waveguides from each other. There are also four ohmic contacts to the 2DEG which allow access to the input and output of each electron waveguide. The I–V characteristics for such a device biased so as to implement two isolated electron waveguides is shown in Fig. 4 [10]. Quantized conductance in each waveguide is observed. In this paper, we use the unique double staircase I–V characteristics to implement a binary encoder for an analog signal. While this could be equally carried out by

Manuscript received March 8, 1993. This work was supported by NSF Contract DMR-9022933 and by an NSF Presidential Young Investigator Award 9157305-ECS. The review of this paper was arranged by Associate Editor J. Xu.

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IEEE Log Number 9211733.

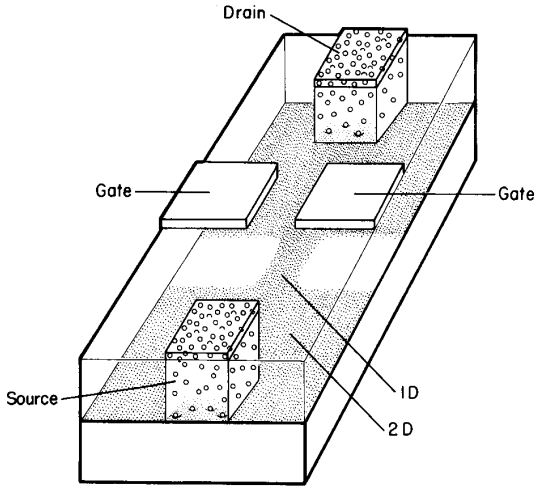

Fig. 1. Conceptual picture of a split-gate electron waveguide device. Shaded region represents electron concentration at the heterointerface of an AlGaAs/GaAs modulation-doped heterostructure.

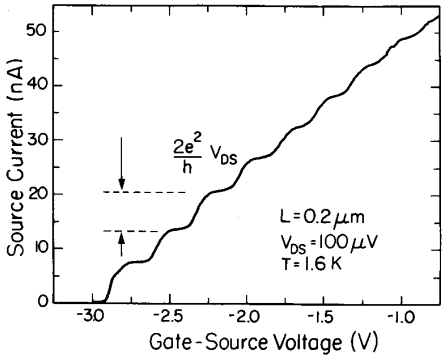

Fig. 2. I_S–V_{GS} characteristics of a 0.2 μm long split-gate electron waveguide device.

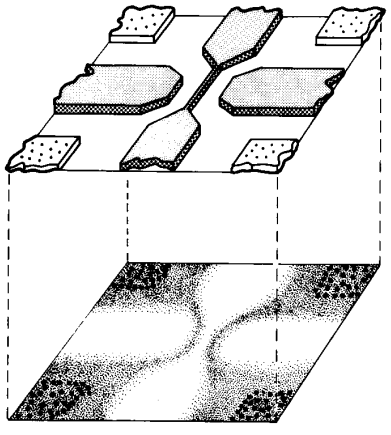

Fig. 3. Conceptual picture of a dual electron waveguide (DWG) device. The top plane represents wafer surface. The bottom plane depicts the electron gas at heterointerface.

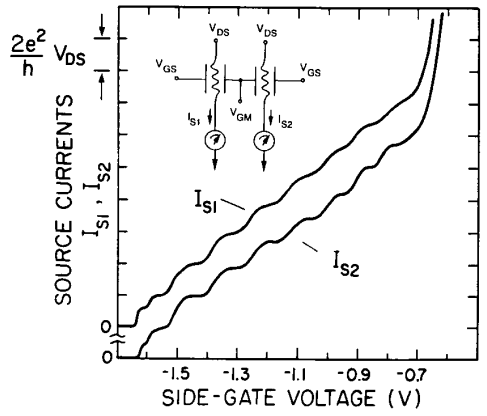

Fig. 4. *I–V* characteristics for the individual waveguides of a dual electron waveguide device. Device schematic shown in inset.

two separate conventional split-gate electron waveguides, the DWG device is a particularly efficient way to implement our scheme.

II. Analog-to-Digital Conversion Scheme

We obtain a single bit of the binary code by using a subtraction scheme in which the properly weighted staircase *I–V* characteristics of the two electron waveguides in a DWG device are subtrated from one another. The basic circuit which we propose to carry out such a technique is shown in Fig. 5. The curvy lines represent the two electron waveguides in our DWG device, as shown in the inset of Fig. 4.

The analog input voltage V_{in} is applied directly to the first side-gate and through a divide-by-two voltage divider to the second side-gate. Since the step width is roughly linear with gate bias, the staircase *I–V* characteristics will be twice as wide in gate voltage for the second waveguide than they are for the first waveguide. The middle-gate is kept at a fixed negative voltage V_{bias1} sufficiently below threshold in order to keep the two waveguides isolated from one another. An offset bias $V_{bias2} = V_{th}$ is needed to line up the staircase of the two waveguides so that they pinch off simultaneously with V_{in}. In addition, the drain-source bias across one of the waveguides is twice that across the other waveguide. The result of this is that the steps in the current for the second waveguide will be twice as high as those in the first waveguide. For the subtraction technique, the drain-source bias across the first waveguide is inverted with respect to the other waveguide. In this way, the combined current measured at the output of the two waveguides is a significant bit series. Fig. 6 schematically illustrates the resulting *I–V* characteristics for each electron waveguide as well as the measured bit series for a ramp voltage input to the circuit in Fig. 5. Each bit representing a 1 has a height in current of $(2e^2/h)V_{DS}$.

By cascading this basic stage into an arbitrary multiple number of stages, one can attain more significant bits.

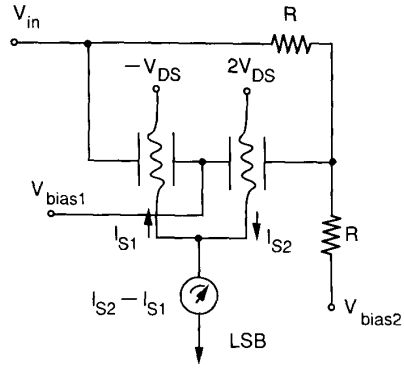

Fig. 5. Basic circuit for achieving one significant bit in proposed A/D conversion architecture.

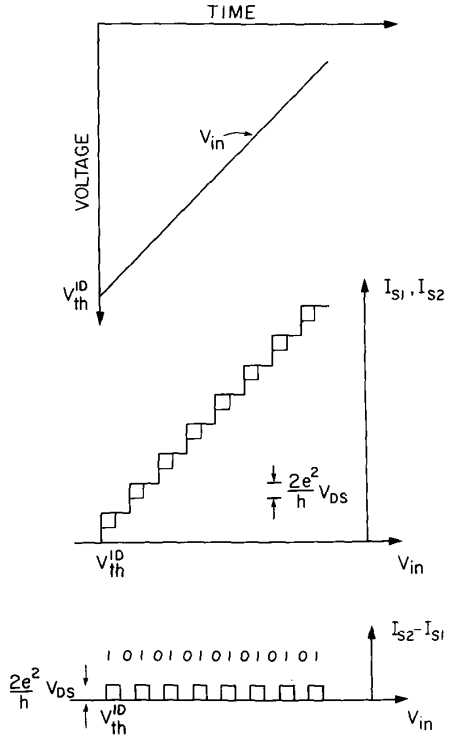

Fig. 6. Schematic illustration of input voltage ramp, *I–V* characteristics of each waveguide and binary bit series in response to analog input of circuit shown in Fig. 5.

Each stage will give one significant bit series. For example, the circuit required for a 4-bit A/D converter is shown in Fig. 7. The input is applied across a binary-ratioed resistor ladder so that the staircase characteristics are properly stretched out to achieve 4 significant bits, one for each stage. For example, for the second stage, the steps are two times and four times as wide as the steps in the first electron waveguide of the first stage. The properly weighted *I–V* characteristics as well as the resulting bit series are shown in Fig. 8. For this example, the largest value which the input can be encoded into is 1111 and the smallest value is 0000.

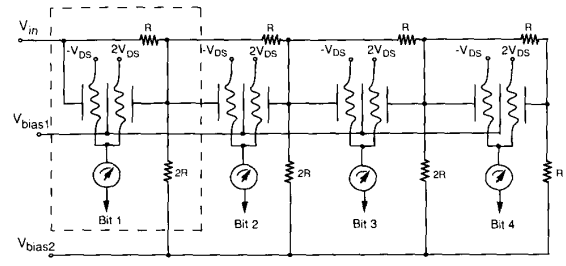

Fig. 7. Cascaded stage architecture to attain four significant bits. Each stage provides one significant bit of resolution.

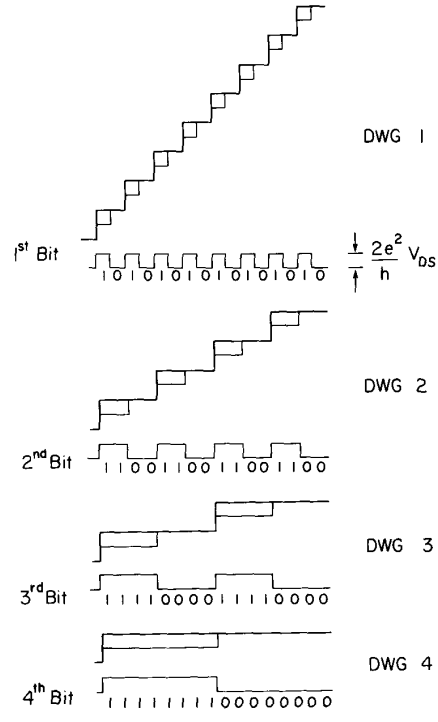

Fig. 8. Schematic illustration of *I–V* characteristics and binary bit series for each stage of circuit in Fig. 7.

Our scheme has the potential to scale to much higher significant bits of resolution with a relatively small number of devices. The limitation of the number of stages that can be assembled together will be the number of steps required in the *I–V* characteristics of the electron waveguides. Table I shows the number of quantized conductance steps as well as the number of DWG devices required to implement an A/D converter with a specified number of significant bits. For example, a 4-bit A/D converter requires 16 conductance steps and 4 DWG devices. This is close to the maximum number of conductance steps which have been observed using the split-gate scheme [7]. Therefore, the additional circuit techniques will be required to scale beyond 4 or 5 bits.

TABLE I
NUMBER OF QUANTIZED STEPS REQUIRED AND THE NUMBER OF DWG DEVICES REQUIRED FOR A SPECIFIED NUMBER OF SIGNIFICANT BITS OF RESOLUTION

No. of Bits	No. of Steps	No. of Devices
2 bits	4 steps	2 DWG's
3 bits	8 steps	3 DWG's
4 bits	16 steps	4 DWG's
5 bits	32 steps	5 DWG's
n bits	2^n steps	n DWG's

III. Device Fabrication and Experimental Results

We fabricated [10], [11] our devices using a high mobility AlGaAs/GaAs modulation-doped heterostructure. The mobility of the 2DEG is 1.2×10^6 cm^2/V − s and the carrier density is 4.2×10^{11} cm^{-2} at $T = 4$ K. The depth of the 2DEG is 890 Å from the surface. Mesa isolation, ohmic contacts and gate pads are defined using optical lithography. The actual split-gate configuration, shown in Fig. 9, is fabricated using electron-beam lithography. The lithographic device dimensions are defined as L representing the length of the confining split-gates and W as the distance between the side-gate and the middle-gate.

We use an $L = 0.5$ μm, $W = 0.4$ μm AlGaAs/GaAs dual electron waveguide device to demonstrate our A/D conversion scheme. We initially bias the device to show the properly weighted staircase characteristics for each waveguide. Following this measurement, the device is biased in a configuration to demonstrate a significant bit series. All measurements are carried out at $T = 1.6$ K.

The actual circuit used to demonstrate the feasibility of properly weighted staircase features for each waveguide is shown in Fig. 10. Two lockin amplifiers are used to measure the drain-source characteristics for the two individual electron waveguides. An ac voltage at 19 Hz of 100 mV is applied through a 1/1000 voltage divider onto the drain contact of the first waveguide. The source contact for that waveguide is tied to the virtual ground of a current-to-voltage preamplifier and then fed into one of the lockin amplifiers. We use the same technique for the second electron waveguide except the ac voltage is 200 mV at a frequency of 11 Hz (different frequency so that lockin measurements do not interfere with one another). The middle-gate voltage separating the two waveguides is fixed at $V_{GM} = -1.5$ V. The input voltage is a ramp function provided by an HP 4145B, beginning at 0 V and continuing onto −2 V. This input is directly applied to the side-gate of the first electron waveguide. In order to line up the thresholds with one another, the same input voltage shifted by −1.8 V, V'_{in}, is applied through the 1 kΩ voltage divider onto the side-gate of the second electron waveguide.

The source currents I_{S1} and I_{S2} as measured by the two lockin amplifiers are shown in Fig. 11. The current I_{S1} flowing out of the first electron waveguide has the familiar $(2e^2/h)V_{DS}$ steps. The current I_{S2} flowing out of the second electron waveguide also has the same staircase structure, except that each step is twice as high and twice as wide as those for the first waveguide. The thresholds of the two electron waveguides also line up very well. The results in Fig. 11 prove that we can engineer the staircase features of two electron waveguides in a manner consistent with our A/D conversion scheme.

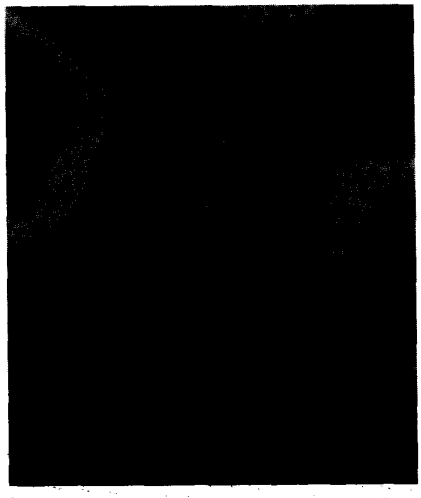

Fig. 9. Scanning electron micrograph of gates in $L = 0.5$ μm, $W = 0.2$ μm dual electron waveguide device.

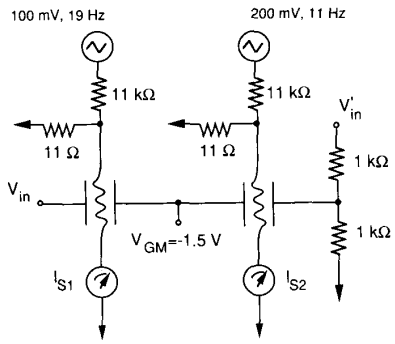

Fig. 10. Circuit used to demonstrate properly weighted I–V characteristics of each waveguide in a DWG device.

We now proceed onto the measurement carried out to show the first, or least, significant bit series. The actual circuit used in our experiment is shown in Fig. 12. Here we use only a single lockin amplifier to measure the difference current. A 100 mV ac bias at 19 Hz is applied through a 1/500 voltage divider onto the drain contact of the second waveguide. This same ac source is applied through an inverting stage, then through a 1/1000 voltage divider onto the drain contact of the first electron waveguide. In this way, we establish $-V_{DS}$ across the first waveguide and $2V_{DS}$ across the second ($V_{DS} = 100$ μV). The source contacts of both electron waveguides are tied together and fed into the preamplifier/lockin setup. The input ramp voltage is configured in the same manner as for the preceding measurement.

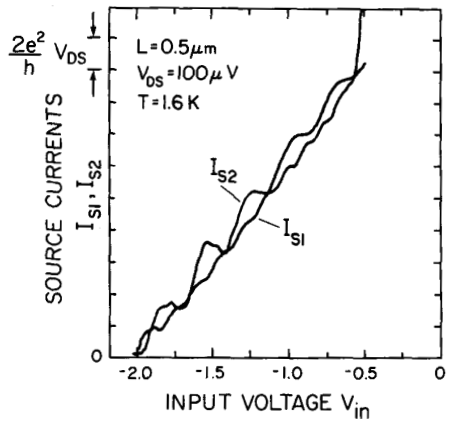

Fig. 11. Measured I–V characteristics of each waveguide in a DWG device to implement first (least) significant bit (T = 1.6 K).

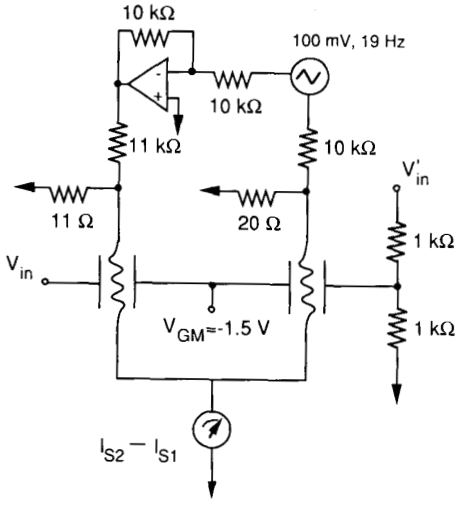

Fig. 12. Circuit used to demonstrate significant bit series.

The source current measured by the lockin amplifier is shown in Fig. 13. The bit series can be clearly seen and it is indeed the subtraction of the two staircase I–V characteristics shown in Fig. 11. The individual bits are less than their ideal height, $(2e^2/h)V_{DS}$, as a result of the less than ideal staircase structure. The bit series has the same 1010 $\cdots$ pattern which we outlined for the least significant bit in our proposal (Figs. 6 and 8).

By passing the input voltage through an additional voltage divider, we can establish the conditions necessary to achieve the second significant bit series. The properly weighted staircase features for each electron waveguide are shown in Fig. 14. The steps in Fig. 14 are twice as wide and four times as wide as they are for the first electron waveguide (Fig. 11). The staircase features still need to be shifted to match the threshold voltage of -2 V for the results in Fig. 11.

The second significant bit series is measured using the

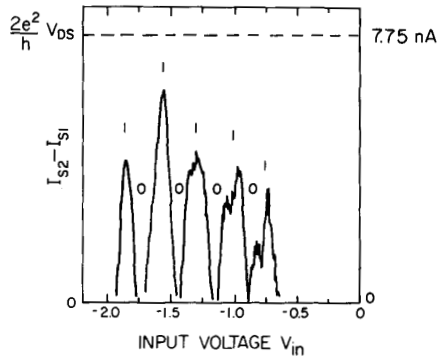

Fig. 13. Measured first (least) significant bit series at (T = 1.6 K).

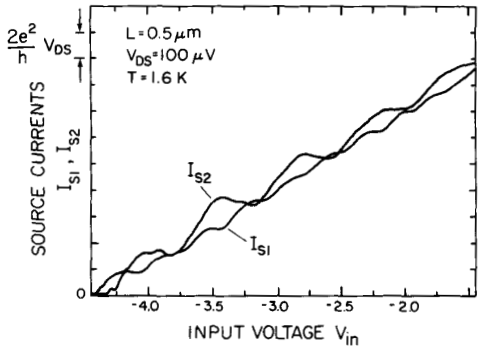

Fig. 14. Measured I–V characteristics of each waveguide in a DWG device to implement second significant bit (T = 1.6 K).

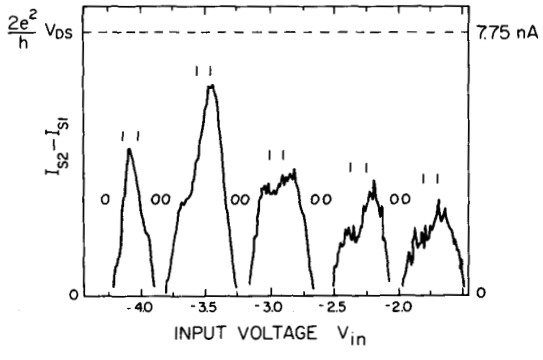

Fig. 15. Measured second significant bit series (T = 1.6 K).

subtraction circuit shown in Fig. 12. It is important to remember that the input voltages still pass through the additional voltage divider. The measured second bit series is shown in Fig. 15. The 110011 $\cdots$ pattern is the same as outlined in our initial proposal (Fig. 8). The bits deviate from their ideal heights due to the less than ideal step structure.

IV. Discussion

We have outlined and demonstrated a novel analog-to-digital conversion architecture based on the quantized

conductance in electron waveguides. By exploiting the functionality of the quantum devices, we have been able to implement efficient circuits with only a small number of active devices. In this section, we will discuss the limitations of our analog-to-digital conversion scheme.

The deviation from the expected $2e^2/h$ conductance value for the steps in our data is a result of finite scattering in the channel [12] for the particular device used in the experimental demonstration. A transmission coefficient can be associated with each mode which gives the probability of an electron reaching the output of the waveguide [13]. For an ideal electron waveguide in which scattering is completely absent, the transmission coefficient for the different modes are all unity. However, when scatterers exist in the channel, the transmission coefficient deviates from unity and in fact becomes energy dependent. The result is that the steps become rounded and smaller than their ideal $2e^2/h$ value [14][16]. Previous work has shown that even a single scatterer can strongly affect the sharpness of the conductance steps [17]–[19]. This of course is a serious concern for the practical implementation of our A/D conversion scheme.

Another problem for our A/D conversion scheme is the low temperatures and small drain-source biases required to observe the quantized conductance. The main reason for these strict conditions is the small energy subband separations in our channels. The energy spacing is typically around 1 meV for split-gate induced channels [20]. In order to resolve the individual levels (quantized conductance), thermal and voltage smearing of the electron distribution around the Fermi level must be kept smaller than the energy level spacings. Therefore, the spacing (1 meV) must be larger than 3.5 kT and eV_{DS} which are the respective smearing functions [21]. This limits the measurement temperature to below 4 K and the drain-source bias to below 1 mV.

The reason for the narrowly spaced subbands is the soft lateral confining potential induced by the fringing fields of the split-gate bias. In order to have high mobility samples, a large spacer region is needed between the dopants and the heterointerface. This results in a deep 2DEG, far removed from the split-gates on the surface, which in turn gives rise to the soft parabolic confining potential. The solution to this problem is to increase the subband spacing through sharper confining schemes [22] and novel material systems [23]–[25].

V. Conclusions

We have proposed and demonstrated a novel analog-to-digital conversion architecture based on the quantized conductance of electron waveguides. Our scheme shows that it is possible to exploit the unique features observed in electron devices to implement efficient circuits. This work represents the first electronic circuit ever realized that utilizes electron waveguide devices.

Acknowledgment

We would like to acknowledge M. R. Melloch (Purdue University) for sample growth and M. J. Rooks (NNF, Cornell University) for electron-beam lithography.

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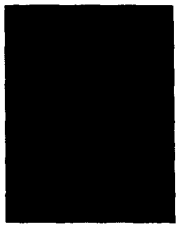

Cristopher C. Eugster (S'91–M'92) was born in San Antonio, TX, on October 11, 1965. He received the B.S. degree in electrical engineering from Texas A & M University, College Station, in 1987, and the M.S. and Ph.D. degrees in electrical engineering from the Massachusetts Institute of Technology, Cambridge, in 1989 and 1993, respectively. His Ph.D. thesis investigated the physics and technology behind novel quantum-effect devices and circuits. His Ph.D. work was partly funded by an IBM Fellowship.

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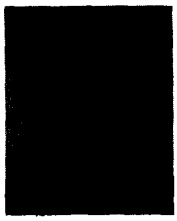

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Mr. Nuytkens was awarded the National Strategic Defense Initiative Distinguished Performance Award in 1988. In 1990, he was awarded the Charles Stark Draper Laboratory Distinguished Performance Award. He served on the 1991–1992 IEDM integrated circuit committee. He is currently the 1993 IEDM integrated circuit committee chairman.

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Dr. del Alamo is the current holder of the ITT Career Development Professorship at MIT. In 1991, he was awarded the Presidential Young Investigator Award by NSF. In 1993 he received the Harold E. Edgerton Award given to a junior faculty every year at MIT. He is a member of the American Physical Society and the Japanese Society of Applied Physics.