Presence of deep-level states may have serious effects in the performance of devices based on diamond. For example, in the case of p-n junction devices, the reverse leakage current, the switching speed, and on-state conduction characteristics are dependent on the lifetimes of the carriers, which in turn are controlled by the position, density, and capture cross sections of the traps. Also, deep-level impurities lead to compensation effects, resulting in changes in the background resistivity. Changes in resistivity affect the breakdown voltage and current conduction in power Schottky rectifiers and p-n junction devices.

IV. Conclusions

Current–voltage characteristics of P-doped polycrystalline Si, Au, and Pt contacts on natural diamond crystals have been investigated. These contacts show excellent rectification with low reverse leakage current densities. Although the *I–V* and *C–V* characteristics indicate the presence of a barrier, the *I–V* characteristics are apparently dominated by bulk effects rather than by thermionic emission over the barrier. Logarithmic plots of the *I–V* characteristics in the forward direction indicate space-charge-limited current conduction through the active volume of the devices. The natural diamond crystals investigated show the presence of deep levels in the energy range 0.5–0.8 eV above the valence band.

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A New Drain-Current Injection Technique for the Measurement of Off-State Breakdown Voltage in FET's

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***Abstract*—We present a new simple three-terminal technique to measure the off-state breakdown voltage of FET's. With the source grounded, current is injected into the drain of the on-state device. The gate is then ramped down to shut the device off. In this process, the drain–source voltage rises to a peak and then drops. This peak represents an unambiguous definition of three-terminal breakdown voltage. In the same scan, we additionally obtain a measurement of the two-terminal gate–drain breakdown voltage. The proposed method offers potential for use in a manufacturing environment, as it is fully automatable. It also enables easy measurement of breakdown voltage in unstable and fragile devices.**

Precise knowledge of the off-state breakdown voltages of a device is essential for its application in a circuit environment. Off-state breakdown limits the voltage swing of logic circuits and the power density of amplifiers [1]. In the FET literature, however, the characterization of this important parameter is clouded by the use of many different measurement and extraction techniques.

A "two-terminal" technique is used to measure gate breakdown with the following variations: a) Drain grounded and source floating [2]–[7]; this gives the drain–gate breakdown voltage BV_{DG}. b) Source grounded and drain floating [2], [8]; this gives the source–gate breakdown voltage BV_{SG}. c) Both source and drain grounded [7], [9], [10]; this gives approximately the lower voltage of a) and b). A "three-terminal" technique is used to obtain the drain–source breakdown voltage [3]–[5], [8], [10]–[14] and also BV_{DG} [4], [10], [15].

A variety of criteria are used in extracting values from the above techniques. Breakdown voltages are extracted either visually from the shape of the breakdown characteristic [4], [5], [8], [12]–[14] or at a given current criteria—commonly but not always 1 mA/mm of gate width [2]–[4], [6], [7], [9]–[11], [15]. For the three-terminal measurement, the gate bias offers an additional degree of freedom. The channel can either be off [3], [4], [8], [12], [13] (off-state breakdown), or on [12] (on-state breakdown).

For many applications, the off-state drain–source breakdown

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voltage BV_{DS} is an important parameter. BV_{DS} is typically defined as the drain voltage of the turned-off device (with respect to the grounded source), where a sharp rise in I_D occurs on the output I–V characteristics. It does not necessarily imply that breakdown occurs in the channel; it could equally occur between drain and gate [1]. BV_{DS} cannot be a precisely defined value because of the following two reasons. First is the difficulty in defining the threshold voltage V_T, especially for short-channel devices. Second is the dependence of BV_{DS} on V_{GS} [4]. There is, however, a particular value of BV_{DS} which is uniquely defined [4], [16]. This is the maximum drain-source voltage the device can attain for a given drain-current criteria. At this bias point, as shown later, V_{DS} is limited by gate breakdown. We have therefore labeled this point as BV_{DS}^{G}. A typical procedure of measuring this parameter consists of displaying the output I–V characteristics till breakdown on a curve tracer, and then adjusting the gate-voltage *offset amplitude* knob to maximize V_{DS} at a certain drain-current criteria, most commonly 1 mA/mm [16]. This procedure, however, is tedious and unsuited for a manufacturing environment. It is repetitive and will therefore give ambiguous results with unstable devices [9], i.e., which show a large breakdown drift with repetitive scanning. Additionally, for fragile devices, great care must be taken to limit the current and prevent device destruction.

We present a new *Drain-current Injection technique* to unambiguously measure both BV_{DS} and BV_{DG}, which overcomes the above difficulties. The schematic is shown in Fig. 1. We have implemented it using an HP 4145B semiconductor parameter analyzer. To characterize breakdown, a fixed predefined current is injected into the drain, the gate–source voltage is ramped down from a strong forward bias to below threshold, and V_{DS} and I_G are monitored. The technique traces the locus of V_{DS}, V_{DG}, and I_G versus V_{GS} at fixed I_D on the output I–V characteristics. BV_{DS}^{G} is unambiguously defined as the maximum V_{DS} attained, irrespective of V_{GS}. BV_{DG} is defined at $I_D = -I_G$, i.e., $I_S = 0$. Additionally, the onset of channel breakdown can also be observed in some cases. We denote this point as BV_{DS}^{Ch}.

Fig. 2 shows *Drain-current Injection* scans obtained on three commercial FET's: a) GaAs MESFET (NEC NE-9000), b) AlGaAs/GaAs HEMT (Fujitsu FHX04LG), and c) Si JFET (National Semiconductor 2N5459). The I_D criteria used were 1 mA/mm for the MESFET and HEMT and 1 μA for the JFET. 1 μA was the value used in the JFET data sheet (W_G was not given). The devices were stabilized by biasing them at BV_{DS}^{G} for 5 min.

Consider the NE-9000 GaAs MESFET. This has $L_G = 0.5$ μm, $W_G = 400$ μm, and $V_T = -2.7$ V. Fig. 2(a) is the plot of V_{DS}, V_{DG}, and I_G versus V_{GS}. Above V_T, both V_{DS} and V_{DG} are relatively small. At $V_{GS} \approx -3$ V, both V_{DS} and V_{DG} rise sharply. As V_{GS} is further lowered, I_G starts becoming significant. V_{DS} then peaks at 11.8 V and starts decreasing linearly while V_{DG} plateaus at approximately 17 V. At this point, $I_D \approx -I_G$. Similar characteristics are observed for the HEMT and JFET (Fig. 2(b) and (c)). BV_{DS}^{G} is unambiguously defined as the peak V_{DS} and BV_{DG} is defined at $I_S = 0$. The extraction of these values may be easily automated.

The drain-current injection technique, in addition, provides insight into the physics of breakdown. The scans in Fig. 2 can display four regions, best exemplified by the NE-9000 MESFET. These can be interpreted with reference to the output I–V characteristics in Fig. 3. Region I: Linear: $V_{GS} > -3.0$ V. V_{DS} is low because the channel is conducting. Region II: Saturation: $-3.0 > V_{GS} > -3.4$ V. V_{DS} rises rapidly with a slope determined by the finite output conductance of the device. Region III: Channel breakdown: $-3.4 > V_{GS} > -5.2$ V. The onset of this region is defined by an abrupt decrease in the slope of V_{DS} versus V_{GS} in Fig. 2(a). If the V_{DS} curve is mapped onto the device output I–V characteristics of Fig. 3, it is seen that the facet of Fig. 2(a) is due to the sudden *increase* in slope of I_D with V_{DS}, characteristic of breakdown phenomena. One can also conclude that this is channel breakdown, since I_G is negligible at this point. For this reason, we have labeled V_{DS} at the onset of the facet as BV_{DS}^{Ch}. As V_{GS} is further

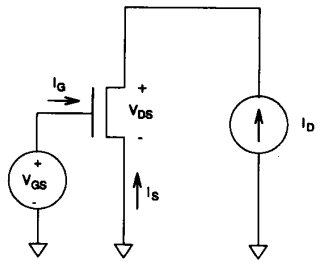

Fig. 1. Schematic circuit diagram for *Drain-current Injection* technique.

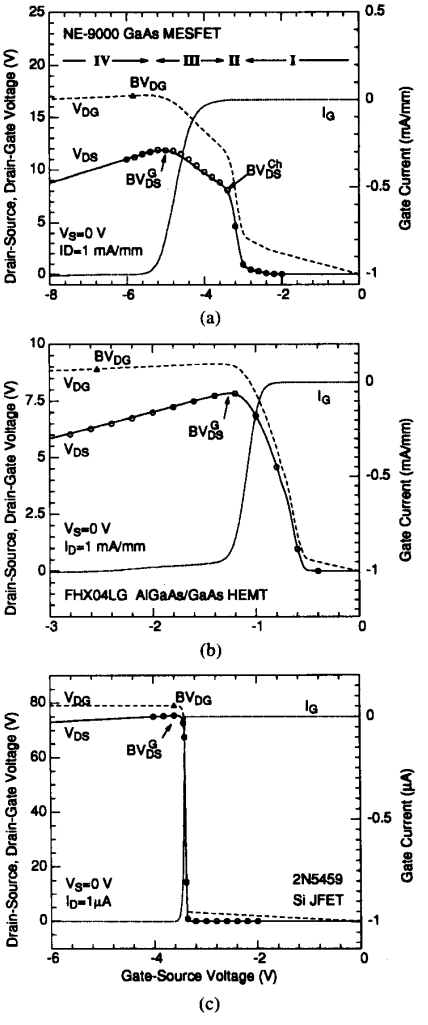

Fig. 2. Illustration of *Drain-current Injection technique* on (a) GaAs MESFET, (b) AlGaAs/GaAs HEMT, and (c) Si JFET. For comparison, BV_{DG} (triangle) was measured between gate and drain (source floating) at $I_D = 1$ mA/mm. The circles (V_{DS}) were measured from the output I–V characteristics at $I_D = 1$ mA/mm. For a discussion of the four regimes marked in Fig. 2(a), see text.

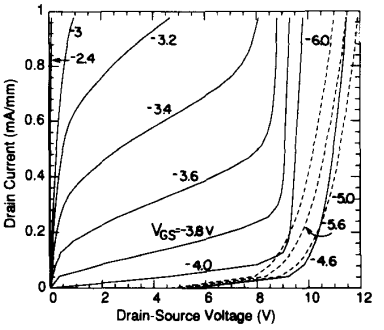

Fig. 3. The output I–V characteristics on the NE-9000 GaAs MESFET till I_D = 1 mA/mm for V_{GS} from −2.4 to −6 V. In the drain-gate breakdown regime, the characteristics have been drawn with dashed lines.

lowered in region III, V_{DS} rises gradually as the device is further shut off and channel breakdown is suppressed. Towards the end of region III, drain–gate breakdown starts occurring (I_G starts becoming significant in comparison to I_D), as V_{DG} becomes larger. The end of region III is defined by the peak V_{DS} value, which occurs when V_{DS} becomes limited by drain–gate breakdown. Region IV: Drain–gate breakdown: $V_{GS} < -5.2$ V. The drain–gate voltage becomes independent of V_{GS} and all the drain current comes out of the gate (Fig. 2(a)). On the output I–V characteristics, the sharp rise in I_D (Fig. 3—dashed lines) shifts to lower V_{DS}. This behavior is the signature of drain–gate breakdown. Breakdown also becomes gentler, indicating a changeover to another mechanism.

An important fact shown in Fig. 2 is the ability of the technique to resolve the channel- and gate-dominated regions of device breakdown. The breakdown mechanisms differ between devices. The Si JFET exhibits a sharp turn-off characteristic (Fig. 2(c)), going straight into gate breakdown. The III–V devices have a softer characteristic in which channel breakdown tends to occur first, and V_{DS} ultimately becomes limited by gate breakdown [4].

The drain-current injection technique has enabled a study of the physics of breakdown in InAlAs/n^+-InGaAs HFET's [17]. These devices were fragile and unstable, probably because they were unpassivated [9]. By using this technique, we avoided repetitive scanning, and also reduced the risk of burnout from current runaway.

In conclusion, a new method of measuring BV_{DS} and BV_{DG} in FET's is presented. The technique measures BV_{DS} and BV_{DG} in a single scan, and improves existing techniques by enabling an unambiguous measurement of BV_{DS} without the need for precisely determining V_T. Extraction of breakdown voltages is simple and automatable, making this technique valuable for a manufacturing environment.

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A Simple Two-Dimensional Model for Subthreshold Channel-Length Modulation in Short-Channel MOSFET's

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***Abstract*—A physical yet simple model that describes subthreshold channel-length modulation and its complex relationship with DIBL in short-channel MOSFET's is derived. The underlying quasi-two-dimensional analysis produces a V_{DS}-independent value for the modulated**

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