Doubly Strained $In_{0.41}Al_{0.59}As/n^+$-$In_{0.65}Ga_{0.35}As$ HFET with High Breakdown Voltage

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***Abstract*—An $In_{0.41}Al_{0.59}As$ / n^+-$In_{0.65}Ga_{0.35}As$ HFET on InP was designed and fabricated, using the following methodology to enhance device breakdown: 1) a quantum-well channel to introduce electron quantization and increase the effective channel bandgap, 2) a strained $In_{0.41}Al_{0.59}As$ insulator, and 3) the elimination of parasitic mesa-sidewall gate leakage. The $In_{0.65}Ga_{0.35}As$ channel is optimally doped to $N_D = 6 \times 10^{18}$ cm^{-3}. The resulting device ($L_g = 1.9$ μm, $W_g = 200$ μm) has $f_t = 14.9$ GHz, f_{max} in the range of 85 to 101 GHz, MSG = 17.6 dB at 12 GHz, $V_B = 12.8$ V, and $I_{D(max)} = 302$ mA / mm. This structure offers the promise of high-voltage applications at high frequencies on InP.**

InAlAs/InGaAs heterostructure FET's (HFET's) on InP have recently emerged as an optimum choice for a variety of microwave and photonics applications. Increasing the InAs mole fraction in InGaAs improves its electron transport properties [1]–[3]; InAs-rich ($x > 0.53$) channels have recently attained world-record current gain cutoff frequencies [3]. Unfortunately, the low breakdown voltage V_B of InAlAs/InGaAs MODFET's on InP (typically less than 5 V [2]) severely restricts their use in many applications. This is the case of power amplification at high frequencies. It is also the case of InP photonics receivers, where it forces the use of a separate low-voltage supply, since optimum MSM photodetector operation requires voltages beyond those supported by the MODFET's [2], [4].

InGaAs channels on InP, by consequence of their narrow bandgap, cannot compete with GaAs or InP channels in terms of power handling at moderate frequencies. However, an approach that succeeds in raising the breakdown voltage of InGaAs channels will enable a new realm of applications: medium power at frequencies unattainable by GaAs or InP channels, and also the possibility of monolithic long-wavelength photonics receivers with a single power supply.

A device with great potential for power handling is the InAlAs/n^+-InGaAs metal insulator doped-channel FET (MIDFET), by virtue of its undoped insulator and thin, heavily doped channel. In this structure, the breakdown voltage V_B is not only large but we have previously shown that it can be engineered using pseudomorphic insulators [5] and channel quantization [6]. Drain current I_D, transconductance g_m, and cutoff frequency f_t can also be increased with InAs-rich channels [1], [3], [7], however at the cost of severely reduced V_B. This is due to the reduced bandgap of the material [8] and to severe gate leakage at the sidewall of the mesa [7], [9].

In this work, we apply breakdown voltage engineering to an InAs-rich InGaAs channel ($x = 0.65$) and obtain a high breakdown voltage coupled with excellent microwave performance. The device is a doubly-strained $In_{0.41}Al_{0.59}As/n^+$-$In_{0.65}Ga_{0.35}As$ HFET. The high InAs-mole fraction in the channel provides a boost to f_t and $I_{D(max)}$. The high-AlAs $In_{0.41}Al_{0.59}As$ insulator forms part of a methodology to enhance the breakdown voltage. The two other components of this methodology consist of a thin subchannel to introduce electron quantization in the channel and increase its effective bandgap [6], and a novel fabrication technique to eliminate mesa-sidewall gate leakage [10]. These separate enhancements are put together here for the first time. In MIDFET's, we find that breakdown occurs from drain to gate. This process involves both the insulator and channel, and as a result, breakdown voltage engineering must consider both layers.

The heterostructure, with the cross section shown in Fig. 1, was grown on semi-insulating InP by MBE. It consists of (bottom to top) a 1000-Å $In_{0.52}Al_{0.48}As$ buffer, a 75-Å $In_{0.53}Ga_{0.47}As$ undoped subchannel, a 100-Å strained n^+-$In_{0.65}Ga_{0.35}As$ Si-doped ($N_d = 6 \times 10^{18}$ cm^{-3}) channel, a 300-Å $In_{0.41}Al_{0.59}As$ strained insulator, and a 50-Å undoped $In_{0.53}Ga_{0.47}As$ cap. The channel doping of 6×10^{18} cm^{-3} is an optimized value, obtained experimentally [11].

The insulator composition was chosen to avoid misfit dislocations while providing maximum conduction band discontinuity [5], [12], [13]. The subchannel thickness was minimized without significantly degrading current driving capability [6]. The InAs mole fraction in the channel ($x = 0.65$) was chosen just below the Matthews–Blakeslee critical-layer limit [12]. Double-crystal X-ray diffraction was performed to investigate the crystalline quality of the material and determine the insulator composition. Even though the insulator exceeds its critical layer thickness, we deduced that the heterostructure is coherent because the

Manuscript received August 21, 1992. This work was supported by the Joint Services Electronics Program under the Research Laboratory of Electronics (DAAL-03-92-C-0001), the C. S. Draper Laboratory (DL-H-441638), Texas Instruments, and Nippon Telegraph and Telephone. B. R. Bennett was supported by an AFOSR graduate fellowship.

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IEEE Log Number 9205884.

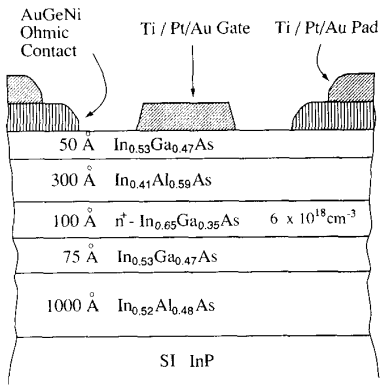

Fig. 1. Cross section of device structure.

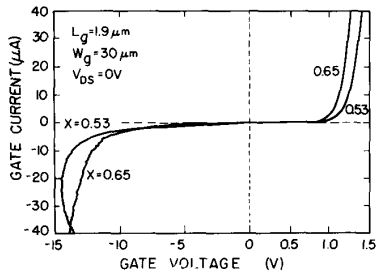

Fig. 2. Forward and reverse gate-diode I–V characteristics for HFET's with $x = 0.53$ and 0.65.

full width at half-maximum of the measured $In_{0.41}Al_{0.59}As$ peak (520 arc-seconds) is very close to its simulated value of 500 arc-seconds, and there are prominent Pendellosung fringes in the X-ray diffraction spectra [11], [12]. The absence of misfit dislocations was further confirmed by the lack of surface ridges on the unprocessed sample under dark-field optical microscopy [13].

Devices were fabricated by first chemically etching a mesa down to the InP substrate. Then, before removing the mesa-level photoresist mask, the wafer was dipped for 40 s into a SA:H_2O_2 6:1 solution [10] to selectively etch the exposed portion of the InGaAs channel at the mesa edge. For the ohmic contacts, 600-Å Ge, 1200-Å Au, and 300 Å of Ni were evaporated, lifted off, and alloyed at 385°C for 10 s. For the gate, 300 Å of Ti, 300 Å of Pt, and 2500 Å of Au were e-beam evaporated and lifted off. This metal scheme, with a Au thickness of 3500 Å, was then used for the pads.

Measurements are reported for HFET's with optically measured 1.9-μm gate length L_g and gate widths W_g of 30 μm (dc devices) and 200 μm (microwave devices). Statistical values of $I_{D(\max)}$, $g_{m(\text{peak})}$, and V_T were obtained by averaging over ten dc devices. V_B for the dc devices was measured from the gate Schottky I–V characteristics at $V_{DS} = 0$ V, and was averaged over five dc devices. These device parameters were: $I_{D(\max)} = 271 \pm 30$ mA/mm, $g_{m(\text{peak})} = 202 \pm 12$ mS/mm, $V_T = -1.19 \pm 0.11$ V, and $V_B = 12.8 \pm 3.1$ V. The contact and sheet resistance were measured using the transmission-line method (TLM). Values averaged over three structures were $0.61 \pm 0.01\ \Omega \cdot$ mm and $747 \pm 7.9\ \Omega/\square$ respectively, allowing us to estimate a source resistance ($L_{GS} = 1.2$ μm) of $1.51 \pm 0.01\ \Omega \cdot$ mm. Room temperature measurements on a Hall bar fabricated alongside the HFET's gave $n_s = 2.06 \times 10^{12}$ cm^{-2} and $\mu = 3664$ cm^2/V · s.

Fig. 2 shows typical gate ($V_{DS} = 0$ V) I–V characteristics of the HFET's. Also superimposed are the gate characteristics of an otherwise identical device, except for the channel composition of $x = 0.53$ (lattice matched to the substrate). Both heterostructures were grown on the same day and were processed together. The V_B of both devices are almost identical, in contrast with our earlier studies which showed that a high InAs mole fraction in the channel drastically degrades V_B [7]. This demonstrates the successful application of our breakdown enhancement methodology. The forward-gate characteristics exhibit high turn-on voltages (≈ 1.2 V). This is a benefit of the increased ΔE_c offered by the AlAs-enriched insulator [5], which is apparent only in the absence of mesa-sidewall gate leakage.

The microwave HFET ($W_g = 200$ μm) on which the high-frequency measurements were performed (see below) had $I_{D(\max)} = 302$ mA/mm, $g_{m(\text{peak})} = 190$ mS/mm, $V_T = -1.24$ V, and $V_B = 12.8$ V. V_B here is defined as the drain-to-source breakdown voltage of the output I–V characteristic at 5% of $I_{D(\max)}$. A power density, $W = 0.40$ W/mm, was calculated as in [14] by multiplying $1/8 \cdot I_{D(\max)} \cdot [V_B - V_{DS(\text{sat})}]$. $V_{DS(\text{sat})}$ was taken as the drain–source voltage at which I_D falls to 90% of its maximum value. The output I–V characteristics (on an identical device on the next die, since this device was destroyed during the measurement) are shown in Fig. 3. V_B for this adjacent device was 14 V.

Fig. 4 is a plot of the forward current gain (H_{21}) and the maximum stable gain (MSG) versus frequency for the $W_g = 200$ μm HFET at $V_{DS} = 4.5$ V and $V_{GS} = 0.4$ V. We used the MSG since the device was conditionally stable ($k < 1$) over the measured frequency range of 1–26 GHz. We obtain $f_t = 14.9$ GHz and $f_{\max}$ as high as 101 GHz. This value was obtained by extrapolating the average MSG over 22–26 GHz at −20 dB/decade. A more conservative extrapolation of $f_{\max} = 85$ GHz was obtained by a logarithmic regression of MSG between 24 and 26 GHz, since the falloff seems to take place at −23 dB/decade. Values of MSG at 12, 18, and 26 GHz were 17.6, 14.8, and 11.8 dB, respectively. The high $f_{\max}$ is a consequence of low g_d (dc value of 0.9 mS/mm at the peak f_t bias point of $V_{DS} = 4.5$ V and $V_{GS} = 0.4$ V) as this device is probably entering accumulation at $V_{GS} \geq 0$ V [15]. This is inferred by the sudden rise in both f_t and $f_{\max}$ at $V_{GS} \approx 0$ V (not shown). The dc voltage gain when biased for peak f_t is 150. For this device, we calculate an effective electron velocity of 1.8×10^7 cm/s and an $f_t \times L_g$ product of 28.3 GHz · μm.

The $f_t \times L_g$ product is comparable to that obtained on

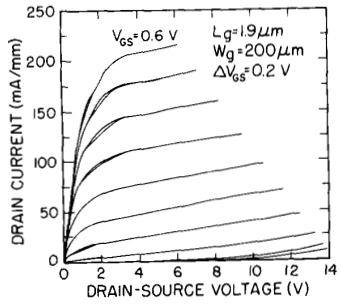

Fig. 3. Output I–V characteristics of L_g = 1.9 μm, W_g = 200-μm HFET.

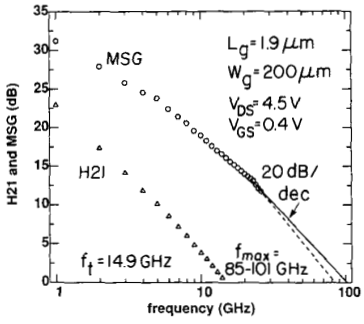

Fig. 4. H_{21} and MSG versus frequency for the HFET with L_g = 1.9 μm and W_g = 200 μm.

lattice-matched MODFET's of similar L_g [16]. This is in accordance with studies showing that saturation velocities are not significantly degraded for doped channels [17]. However, the power density and breakdown voltage are higher [2], [16]. High electron confinement and reduced gate leakage in our HFET's are instrumental in obtaining high f_t and $f_{\max}$, and in obtaining high V_B for an enriched InAs mole fraction in the channel.

In conclusion, in the pursuit of enabling power handling with InGaAs channels, we have combined for the first time in an InAlAs/n$^+$-InGaAs HFET, an AlAs enriched insulator, an InAs enriched channel, channel quantization, optimized channel doping, and mesa-sidewall leakage elimination. This device has a high breakdown voltage and shows excellent microwave characteristics. Scaled-down versions should extend the availability of power to frequencies unattainable by GaAs or InP channels. These devices are also very promising for photonics applications.

ACKNOWLEDGMENT

The authors thank Prof. C. G. Fonstad for the use of his MBE, and Dr. W. P. Hong at Bellcore for the use of his microwave characterization facility.

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