Physics of breakdown in InAlAs/n$^+$–InGaAs Heterostructure Field-Effect Transistors

Sandeep R. Bahl and Jesús A. del Alamo
Massachusetts Institute of Technology, Cambridge, MA 02139

Abstract: InAlAs/n$^+$–InGaAs HFET's have demonstrated a high breakdown voltage in spite of their narrow channel bandgap. In order to understand this unique feature, we have carried out a systematic study in a range of temperatures around room-temperature. We find that for HFET's with L_G=1.9 μm, breakdown is drain-gate limited and is a two-step process. First, electrons are emitted from the gate to the insulator. Second, as a consequence of the large ΔE_C, they enter the channel hot, into the high-field drain-gate region, and immediately relax their energy, causing impact-ionization. This combined mechanism explains all our observations to date regarding off-state breakdown phenomena in InAlAs/n$^+$–InGaAs HFET's.

Introduction

InAlAs/InGaAs Heterostructure Field-Effect Transistors (HFET's) have emerged as promising candidates for applications in microwave and lightwave communication systems. MODFET's from this material system have achieved world-record frequency and low-noise performance [1]. There is, however, one fundamental weakness of InAlAs/InGaAs HFET's when compared to GaAs-based FET's. $In_{0.53}Ga_{0.47}As$ has a bandgap (E_G) of 0.73 eV [2], about half the bandgap of GaAs (E_G=1.42 eV) [3]. This fundamentally limits their off-state breakdown voltage, V_B. It is for this reason that, although the advantages of InAlAs/InGaAs HFET's for power microwave applications have been recognized [4], they have yet to be exploited [1]. It is also for this reason that InP photonics receivers based on InAlAs/InGaAs HFET's need a separate low-voltage supply, since the HFET's cannot support the voltages required for optimum MSM photodetector operation [5].

A device structure that might alleviate this problem is the InAlAs/n$^+$–InGaAs HFET. This HFET has shown significantly improved V_B. Furthermore, in previous work we have shown that V_B can be increased by using insulators and channels with lower InAs-mole fractions, and channels with lower thickness and doping (see references in [6]). An understanding of the physics of breakdown will enable the ability not only of *engineering* the breakdown voltage of this device, but also will provide ideas for increasing the breakdown voltage of the MODFET.

In this paper, we present the first comprehensive study of off-state (channel turned-off) breakdown in InAlAs/n$^+$–InGaAs HFET's. V_B is an important figure of merit for many applications. For example, it limits the power density of class-A amplifiers [1]. In our study, we used a new *Drain-current Injection technique* to characterize three-terminal off-state breakdown.

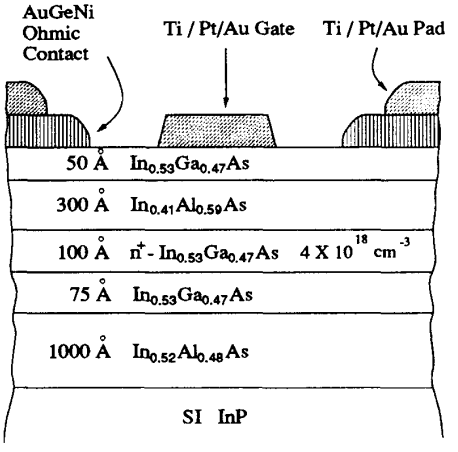

Figure 1: Cross-section of device structure.

Experimental

The device structure used in this study is shown in Fig. 1. It was grown by MBE on S.I. InP and has a 300 Å thick undoped $In_{0.41}Al_{0.59}As$ *pseudo*-insulator, and a 100 Å thick n$^+$(Si-doped to 4×10^{18} cm^{-3})–$In_{0.53}Ga_{0.47}As$ channel [7]. The device fabrication sequence is described in ref [6].

The following devices were used in this study. First, an HFET with (optically measured) L_G=1.9 μm and W_G=30 μm. Second, a sidegate structure with (nominal) L_G=2 μm and W_G=30 μm. The sidegate contact is formed by ohmic metallization, has dimensions of 15 μm by 40 μm, and lies parallel to the HFET mesa with a separation of 15 μm. It is isolated from the main FET by etching the mesa down to the substrate. A sketch is shown in the inset of Fig. 8. Third, a gated Hall-bar structure. This is essentially a long-gate FET (L_G=34 μm and W_G=20 μm) with three voltage taps directly into the gated channel (see inset in Fig. 4). The outer taps are placed 3 μm away from the gate edge and the inner tap is centered with the gate-edges.

Both drain-source breakdown voltage, $V_{B(D-S)}$, and drain-gate breakdown voltage, $V_{B(D-G)}$, were measured. In our terminology, "drain-source breakdown voltage" refers to the breakdown of the drain with respect to the grounded source, *i.e.* the sharp rise of I_D on the output I-V characteristic [1]. It does not necessarily imply that breakdown occurs in the drain-source path.

To carry out this study, we have formulated a new Drain-

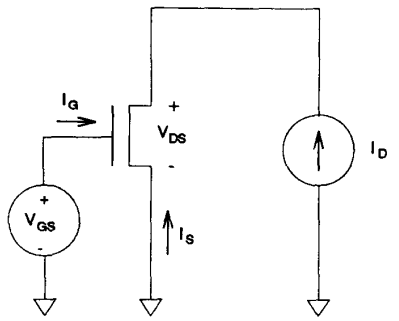

Figure 2: Schematic circuit diagram for the *Drain-current Injection technique*.

current Injection technique. The schematic is shown in Fig. 2. A typical scan is shown in Fig. 5. To measure breakdown, a fixed current (typically 1 mA/mm of gate-width) is injected into the drain of the on-state device. The gate-source voltage is then ramped down from a strong forward bias to below threshold, and V_{DS} and I_G are monitored. In this manner, the device goes from the linear regime, through the saturation region and into the breakdown regime. $V_{B(D-S)}$ is unambiguously defined as the maximum V_{DS} attained, irrespective of V_{GS}. $V_{B(D-G)}$ is defined at I_D=-I_G, *i.e.* I_S=0. This technique essentially traces the locus of V_{DS}, V_{DG} and I_G vs. V_{GS} at I_D=1 mA/mm on the output I-V characteristics.

The Breakdown Mechanism

The InAlAs/n^+–InGaAs HFET consists of a thin undoped wide-bandgap *pseudo*-insulator and a thin heavily-doped narrow-bandgap channel, with substantial ΔE_C between both layers. There can be several potential breakdown mechanisms in such a structure. The experiments which we present below convincingly show that, at around room-temperature, both thermionic-emission and Auger generation [8] (impact-ionization at a potential step [9]) play a key role in breakdown.

The combined thermionic-emission/Auger-generation process, shown schematically in Fig. 3, is a two step process. First, electrons are injected from the gate into the insulator by thermionic, thermionic-field, or field emission. Second, because of the large conduction-band offset and the electric-field in the insulator, they enter the channel hot, into the high-field gate-drain region, and immediately relax their energy, causing impact-ionization. The electrons flow towards the drain, and the holes can either be extracted by the gate or flow towards the source, where they recombine with electrons.

The proof of this hypothesis requires the verification of the following facts:

(a) the high-field region is in the drain-gate gap;

(b) breakdown occurs from drain to gate, *i.e.* drain-gate breakdown limits the maximum drain-source voltage of the device;

(c) I_G is thermally activated approaching breakdown;

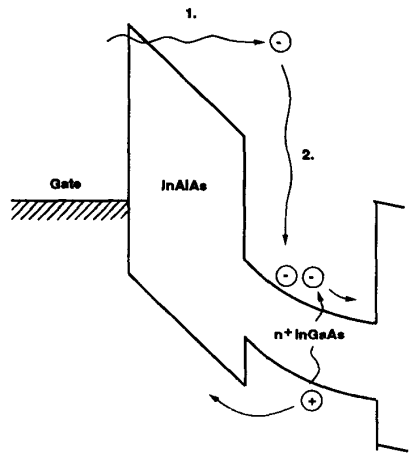

Figure 3: A schematic showing the combined effect of electron emission and Auger generation.

(d) electron-hole pairs are generated in the channel during breakdown; and

(e) breakdown is not triggered by the source current, I_S.

In the next section, we present a series of experiments which confirm the above requirements.

Results

(a) High-field regions:
We used the gated Hall-bar structure (inset of Fig. 4) to determine the location of the high-field regions. A measurement of the gate breakdown voltage, with V_{DS}=0 V, was carried out till I_G=-2 mA/mm. The data is presented in Fig. 4. As V_G is lowered, the tap voltages track the drain/source potential (0 V) until $V_G = V_T$. (- 0.75 V for this device). At this point the channel becomes totally depleted, and the voltage taps are cut off from the drain and source. From this point on, they track the gate voltage with a slope of 1.00. All three tap voltages were approximately equal for the entire measurement.

From this data the following two conclusions may be made: (a) there is no lateral electric field underneath the gated channel, and (b) most of the gate-drain voltage is dropped in the gate-drain gap, *i.e.* a high field region exists at the gate edge of the drain-gate gap. We found that these conclusions were consistent with 2-D simulations using PISCES-2b.

(b) Breakdown occurs from drain to gate:
Fig. 5 shows the Drain-current injection scan at T=300 K for a typical HFET. The plot shows V_{DG}, V_{DS} and I_G vs. V_{GS} at I_D=1 mA/mm. Above threshold, the channel is on, $V_{DS}\approx$0 V, and $I_G\approx$0. At around threshold (V_T=-0.8 V), the channel shuts off and both V_{DS} and V_{GS} rise sharply. Breakdown starts in the drain-gate path, and I_G starts rising. At V_{GS}=-1.2 V, V_{DS} peaks at 17 V and V_{DG} plateaus to $\approx$ 18.3 V. Upon decreasing V_{GS} further, V_{DS} decreases linearly with V_{GS}, showing a slope of $\approx$1, while V_{DG} remains constant at $\approx$19 V. At this point, all the injected drain-current comes out of the gate, and

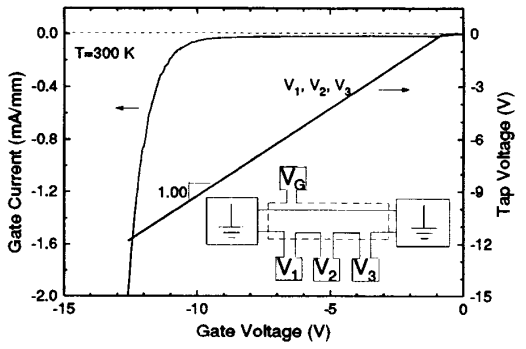

Figure 4: The reverse gate-characteristic of a gated-Hall-bar structure (inset). The data shows that the high-field region is in the gate-drain gap.

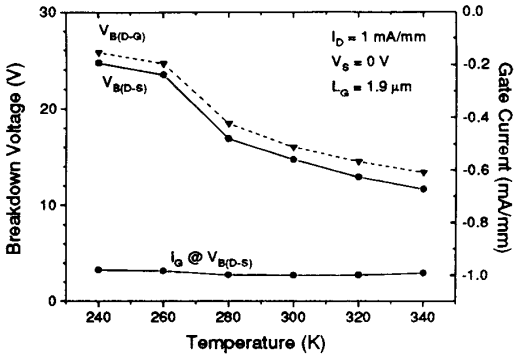

Figure 6: A plot of $V_{B(D-S)}$ and $V_{B(D-G)}$ vs. temperature. I_G@$V_{B(D-S)}$ is also plotted, and shows that breakdown occurs from drain to gate.

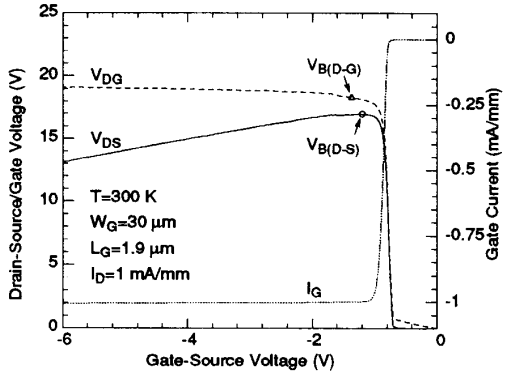

Figure 5: A Drain-current injection scan at I_D=1 mA/mm for the HFET at 300 K. V_{DS} is limited by drain-gate breakdown. V_{DG} becomes independent of V_{GS}. This behavior is a clear signature of drain-gate breakdown, and convincingly shows that drain-gate breakdown limits the maximum drain-source voltage of the device.

(c) I_G is thermally activated approaching breakdown:
The temperature-dependence of $V_{B(D-S)}$ and $V_{B(D-G)}$ was studied by use of the Drain-current Injection technique at 1 mA/mm between T=340 K – 240 K, with ΔT=20 K. Fig. 6 is a plot of $V_{B(D-S)}$, $V_{B(D-G)}$, and I_G@$V_{B(D-S)}$ for this temperature range. V_B shows a negative temperature coefficient, with $V_{B(D-G)}$ increasing from 13.4 V at 340 K to 25.8 V at 240 K. $V_{B(D-S)}$ tracks $V_{B(D-G)}$ with a difference of about V_T (-0.8 V). I_G@$V_{B(D-S)}$ is also ≈-1 mA/mm at all temperatures. This shows that drain-gate breakdown is limiting $V_{B(D-S)}$ in this temperature range.

An Arrhenius plot of I_G/T^2 was generated for several values of V_{DG}. Data from the locus of the drain-current injection technique (I_D=1 mA/mm) was used. The plot is shown in Fig. 7. The gate current was found to be thermally activated with an activation energy of 0.41-0.46 eV, regardless of V_{DG}. This value is consistent with electron thermionic-field emission over the barrier being the breakdown limiting mechanism.

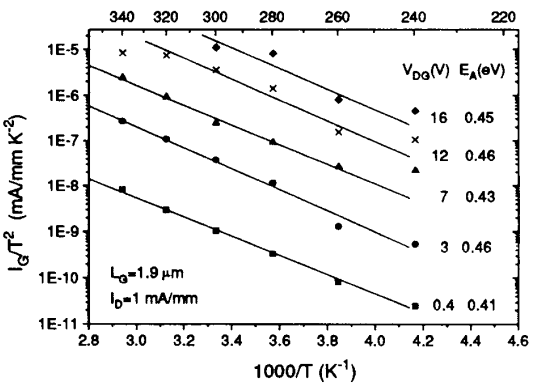

Figure 7: An Arrhenius plot of I_G/T^2 for V_{DG} steps from 0.4 V to 16 V. I_G is thermally activated in the breakdown regime.

(d) Holes are generated in the channel:
To investigate whether electron-hole pairs are generated in the channel during breakdown, we carried out a Drain-current Injection scan at I_D=1 mA/mm on a sidegate structure (inset of Fig. 8). Sidegating structures have previously been used for detecting holes generated by impact-ionization in the channels of GaAs-based devices [10].

Fig. 8 is a plot of V_{DG}, I_G and I_{SG} vs. V_{GS} at T=300 K. To extract holes, the sidegate was biased at -15 V with respect to the grounded source. As the device is turned-off, V_{DS} rises, and a simultaneous increase in both I_G and I_{SG} takes place. The increase in I_{SG} is not due to a parasitic drain-sidegate path, as one might think could arise, since the drain-sidegate voltage, V_{D-SG} also increases in this process. We verified this (not shown) by carrying out (a) a two-terminal drain-sidegate measurement (I_S=I_G=0), and (b) drain-current injection scans at 1 mA/mm, 1.5 mA/mm, and 2 mA/mm. We found that there was no sharp increase in I_{SG} for the two-terminal measurement. For the drain-current injection scans, I_{SG} behaved as shown in Fig. 8, and its peak value increased approximately linearly with I_D. These measurements convincingly show that hole generation occurs in the channel during breakdown.

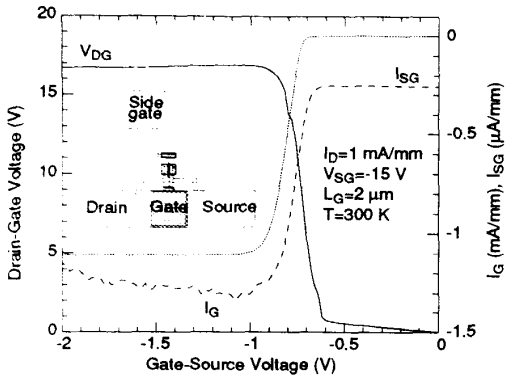

Figure 8: A Drain-current injection scan on a sidegate structure, showing electron-hole pair generation in the channel.

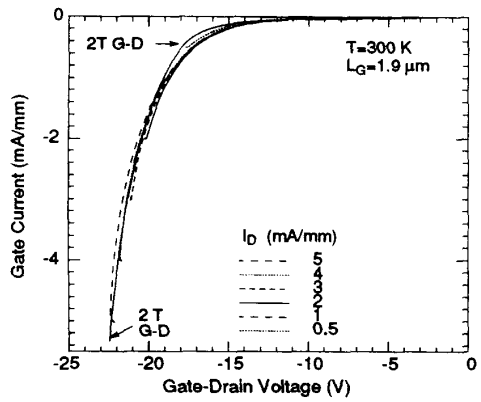

Figure 9: Two- and three-terminal gate-drain characteristics showing that breakdown is independent of I_S. The *2T G-D* characteristic is taken with the source floating.

(e) Breakdown is not triggered by the source current

We have carried out measurements of I_G vs. V_{GD} with different values of I_S. A measurement for I_S=0 was carried out with the source floating. Measurements for other values of I_S were carried out by use of the Drain-current Injection technique with I_D from 0.5 mA/mm to 5 mA/mm. In this case, the I_D vs. V_{GD} characteristics were generated from the locus of the Drain-current Injection scan. The data is plotted in Fig. 9. The two- and all the three-terminal characteristics overlap closely, showing that the (drain-gate) breakdown characteristic is independent of I_S. This shows that the mechanism for off-state breakdown is different from that of on-state (channel turned-on) breakdown in which the source current causes impact-ionization [11]. The difference arises because electrons from the source enter the channel cold, whereas electrons from the gate enter hot.

Discussion

The hypothesis presented above explains all our experimental observations to date on the off-state breakdown of the InAlAs/n$^+$–InGaAs HFET [6]. We have previously found that V_B increases with (a) lower InAs mole fraction in the insulator and (b) a decrease in channel thickness. The lower-InAs insulator has a larger Schottky barrier height [12], and in our hypothesis, enhances breakdown by suppressing hot-electron injection into the channel. A thinner channel has a larger effective bandgap due to quantum-size effects, and increases breakdown by suppressing impact-ionization [6]. We have also found that V_B decreases with (a) higher InAs-mole fractions in the channel, and (b) higher channel doping. We attribute this reduction to respectively, (a) enhanced impact ionization in the lower bandgap [3] channel, and (b) higher electron injection into the channel from a reduced effective Schottky-barrier height, because of the increased electric-field in the cap and insulator at high doping.

This combined thermionic-emission/Auger-generation process is also likely to limit V_B in InAlAs/InGaAs MODFET's, since in these devices, doping the insulator results in a reduced effective barrier to electron emission.

Conclusion:

We present an understanding of the physics of off-state breakdown at around room-temperature in InAlAs/n$^+$–InGaAs HFET's. Breakdown is found to be drain-gate limited and is a two step process. First, electrons are emitted from the gate to the insulator. Second, as a consequence of the large ΔE_C, they enter the channel hot, into the high-field drain-gate region, and immediately relax their energy, causing impact-ionization. This combined mechanism explains all our observations to date on breakdown phenomena in InAlAs/n$^+$–InGaAs HFET's.

Acknowledgements

This work was funded by The Joint Services Electronics Program (DAAL-03-92-C-0001), the C. S. Draper Laboratory (DL-H-441694), Texas Instruments, and Nippon Telegraph and Telephone Corporation.

References

[1] L. D. Nguyen, L. E. Larson, and U. K. Mishra, *Proc. IEEE*, **80**, 494 (1992).
[2] D. K. Gaskill and N. Bottka, *Appl. Phys. Lett.*, **56**, 1269 (1990).
[3] S. Adachi, *J. Appl. Phys.*, **53**, 8775 (1982).
[4] P. M. Smith *et al. This conference*, p. 39 (1990).
[5] J. H. Burroughes and M. Hargis, *IEEE Photonics Tech. Lett.*, **3**, 532 (1991).
[6] S. R. Bahl, B. R. Bennett, and J. A. del Alamo, *IEEE Elec. Dev. Lett.*, **14**, 22 (1993).
[7] S. R. Bahl, B. R. Bennett, and J. A. del Alamo, *This conference*, p. 222 (1992).
[8] S. Tiwari, *Compound Semiconductor Device Physics*, Academic Press (1992).
[9] K. Brennan, T. Wang, and K. Hess, *IEEE Elec. Dev. Lett.*, **6**, 199 (1985).
[10] T. Yokoyama and A. Tamura, *Inst. Phys. Conf. Series*, **120**, 239 (1991).
[11] G. G. Zhou *et al.*, *IEDM Tech. Dig.*, p. 247 (1991).
[12] C. L. Lin *et al.*, *Appl. Phys. Lett.*, **49**, 1593 (1986).