Mesa-Sidewall Gate Leakage in InAlAs/InGaAs Heterostructure Field-Effect Transistors

Sandeep R. Bahl, *Student Member, IEEE*, Michael H. Leary, and Jesús A. del Alamo, *Member, IEEE*

Abstract—**InAlAs/InGaAs HFET's fabricated by conventional mesa isolation have a potential parasitic gate-leakage path where the gate metallization overlaps the exposed channel edge at the mesa sidewall. We have unmistakably proven the existence of this path by fabricating special heterojunction diodes with different mesa-sidewall gate-metal overlap lengths. We find that sidewall leakage is a function of the crystallographic orientation of the sidewall, and increases with channel thickness, sidewall overlap area, and InAs mole fraction in the channel. In HFET's fabricated alongside the diodes, sidewall leakage increased the subthreshold and forward gate leakage currents, and reduced the breakdown voltage.**

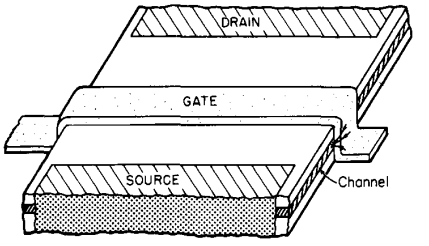

Fig. 1. Perspective of HFET, showing the sidewall-leakage path at the gate-metal/mesa-sidewall overlap.

HETEROSTRUCTURE Field-Effect Transistors (HFET's) from the InAlAs/InGaAs/InP material systems are of great interest for long-wavelength optical and ultra-high-frequency microwave telecommunication applications. Both Modulation-Doped FET's (MODFET's) and Metal–Insulator Doped-channel FET's (MIDFET's) have shown excellent high-frequency performance [1], [2]. MIDFET's have, in addition, shown excellent high-voltage potential [3]. Enriching the InAs mole fraction in the InGaAs channel of these HFET's has resulted in substantial device improvement [2], [4]. This is due to the enhanced electron transport properties of InAs-enriched InGaAs [5].

Fabrication of these HFET's by conventional mesa isolation, however, results in sidewalls where the InGaAs channel is exposed and comes in contact with the gate metallization running up the mesa (Fig. 1). Even though the sidewall contact area can easily be several orders of magnitude smaller than the gate area, the low Schottky-barrier height of metals with $In_{0.53}Ga_{0.47}As$ (0.2 eV) [6] potentially results in a significant leakage path from the gate to the channel. In AlGaAs/GaAs HFET's, mesa-sidewall gate leakage, or *sidewall leakage* for short, should be insignificant due to the higher Schottky-barrier height of GaAs with metals (~ 0.75 eV) [7]. For typical InAlAs/InGaAs HFET's, however, researchers have acknowledged that sidewall leakage causes excessive gate-leakage current [4], [8]–[10] and severely degraded breakdown voltage [4], [9].

To study the effect of sidewall leakage in our MIDFET's, we have fabricated, alongside them, specially designed test structures with varying lengths L_s of mesa-sidewall/gate-metal overlap or *sidewall overlap*. Since the heavy doping in the channel of these test structures enhances tunneling through the barrier, they make good tools to study sidewall leakage. Here, we present what we believe is the first comprehensive study of mesa-sidewall gate leakage in InAlAs/InGaAs HFET's fabricated using conventional mesa isolation. We provide unequivocal evidence of sidewall leakage and show its impact on device characteristics.

II. Experimental

A cross section of the device structure considered in this work is shown in Fig. 2. Six wafers were grown by MBE in MIT's Riber 2300 system, comprising two separate experiments with a common reference wafer. The starting material was semi-insulating Fe-doped InP. Surface preparation of the InP wafer was carried out using a $3:1:1$ $H_2SO_4:H_2O_2:H_2O$ etch followed by a $1:20$ bromine-methanol etch. The reference device structure consists (from bottom to top) of a 1000-Å undoped $In_{0.52}Al_{0.48}As$ buffer layer, an $In_{0.53}Ga_{0.47}As$ channel consisting of a 100-Å undoped subchannel, and a 100-Å heavily Si doped ($N_D = 4 \times 10^{18}$ cm^{-3}) active channel, a 300-Å undoped $In_{0.52}Al_{0.48}As$ gate insulator layer, and an undoped 50-Å $In_{0.53}Ga_{0.47}As$ cap. In one experiment

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S. R. Bahl and J. A. del Alamo are with the Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA 02139.

M. H. Leary was with the Department of Electrical Engineering and Computer Science, Massachusetts Institute of Technology, Cambridge, MA 02139. He is now with Cornell University, Ithaca, NY 14853.

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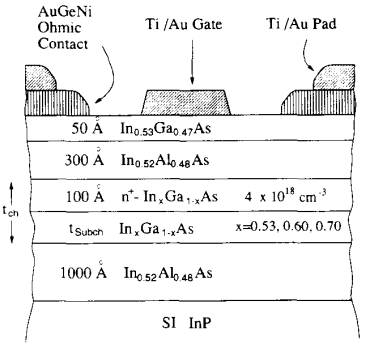

Fig. 2. Schematic cross section of the fabricated $In_{0.52}Al_{0.48}As/n^+$-$In_xGa_{1-x}As$ HFET's.

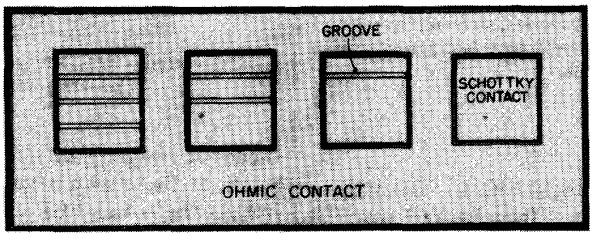

Fig. 3. Photograph of fabricated heterojunction diode test structures with Schottky area of 10 000 μm^2 and sidewall-overlap length L_s of (left to right) 600, 400, 200, and 0 μm.

[4], the InAs mole fraction x in the channel (active channel and subchannel) was increased from lattice matching. Wafers with $x = 0.53$, 0.60, and 0.70 were grown. Due to the varying growth rates of the different $In_xGa_{1-x}As$ compositions, the channel doping is slightly different, since the Si cell was maintained at a constant temperature. The doping levels deduced from MBE calibrations for the $x = 0.53$, 0.60, and 0.70 devices are 4×10^{18}, 4.5×10^{18}, and 5.3×10^{18} cm^{-3}, respectively. In the other experiment [11], the InAs mole fraction of the channel x was fixed at 0.53 and the thickness of the subchannel was varied. Wafers with subchannel thickness of 0, 50, 100, and 250 Å (total channel thicknesses t_{ch} of 100, 150, 200, and 350 Å) were grown. The subchannel separates the active channel from the reverse InGaAs/InAlAs interface and improves transport characteristics [11].

Device fabrication is similar to that used in [3]. In summary, isolation was performed by chemically etching a mesa down to the InP substrate using a $H_2SO_4 : H_2O_2 : H_2O$ 1 : 10 : 220 etch. For the ohmic contacts, 1500 Å of AuGe followed by 300 Å of Ni were evaporated, lifted off, and alloyed at 350°C for 1 min. For the gate and pad, 300 Å of Ti and 2000 Å of Au were electron-beam evaporated and lifted off.

To convincingly identify the existence of sidewall leakage and study its impact on HFET characteristics, we have fabricated alongside the HFET's special heterojunction diodes with an active Schottky area of 10 000 μm^2. The Schottky metallization is the same as that used for the HFET gates. Gate-metal/mesa-sidewall overlaps were created by etching grooves through the active diode during mesa formation, and then depositing the Schottky metal on top. Each groove is 100 μm long and 5 μm wide, and creates two sidewall-overlap edges. SEM photographs have confirmed that these grooves are completely etched down till the InP substrate. Twelve diodes were fabricated with L_s = 0, 200, 400, and 600 μm, running in each of [011], [001], and [0$\bar{1}$1] crystallographic directions. Fig. 3 shows a labeled photograph of the diode test structure along one crystallographic orientation. The ohmic contact surrounds the Schottky region. Forward and reverse I–V characteristics were measured on these diodes.

The HFET drain subthreshold current $I_{D(sub)}$ is a very important parameter for circuit applications, since it limits the transistor off-state current. $I_{D(sub)}$ was measured for HFET's with nominal gate length $L_g = 1.5$ μm (gate width = 30 μm), for all wafers. We have found a strong correlation between the behavior of $I_{D(sub)}$ and the sidewall leakage current as measured by the diodes. The I–V characteristics of the HFET gate were also measured at V_{ds} = 0 V. Detailed measurements on all other figures of merit of these HFET's are presented in [4], [11].

III. Results

A. Heterojunction Diodes

Extensive characterization was carried out on the specially designed diodes. Typical forward and reverse I–V

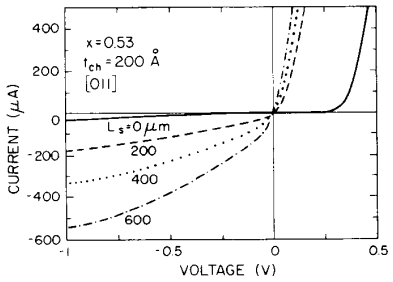

Fig. 4. A plot of forward and reverse currents for heterojunction diodes with $x = 0.53$ and $t_{ch} = 200$ Å, showing the increase in both forward and reverse currents with sidewall-overlap length in the [011] direction.

characteristics of diodes with $L_s = 0$, 200, 400, and 600 μm, running along the [011] direction for our baseline device ($x = 0.53$, total channel thickness = 200 Å) are shown in Fig. 4. Both forward and reverse currents increase with L_s. This is unmistakable evidence of the existence of a sidewall-leakage path. For the diode with $L_s = 0$, the diode forward turn-on is at approximately 0.4 V. With increasing L_s, the diode turn-on voltage drops drastically to about 0.03 V, as would be expected of a low Schottky barrier. This is deleterious to device operation, as it essentially short-circuits the large (0.5 eV) [12] $In_{0.52}Al_{0.48}As/n^+$-$In_{0.53}Ga_{0.47}As$ conduction-band discontinuity of the intrinsic gate structure. The reverse current also increases with L_s in an approximately linear manner. We have found that sidewall leakage in forward and reverse bias increases with L_s not only for sidewall overlaps along the [011] direction, but also along [001] and [0$\bar{1}$1]. Fig. 5 is a plot of the diode current at $V_g = -2$ V (Fig. 5(a)) and $V_g = 0.5$ V (Fig. 5(b)) with $x = 0.53$ in the channel, as a function of L_s in each of the [011], [001], and [0$\bar{1}$1] crystallographic directions. Depending upon the number of working diodes available, each point represents an average over 8–15 devices. The error bars represent two standard deviations. These statistical plots show that both forward and reverse currents increase with L_s and also show a dependence on crystallographic orientation with I [0$\bar{1}$1] > I [001] > I [011]. This could arise from the slightly anisotropic action of our mesa etchant ($H_2SO_4 : H_2O_2 : H_2O$ 1 : 10 : 220), resulting in differently sloped [011] and [0$\bar{1}$1] sidewall profiles [13]. We could not, however, distinguish the difference within the resolution of our SEM photographs. This could also arise from a slight dissimilarity in the Schottky-barrier height for the two crystal planes, as has been reported for different crystal planes in GaAs [14]. The diode without sidewall overlap does not show any dependence on crystallographic orientation, confirming that the orientation dependence arises from the mesa-sidewall leakage path. The large error bars probably indicate the large sensitivity of the leakage current to small differences in sidewall morphology caused by process variations.

We have also studied the effect of channel thickness on sidewall leakage for diodes with $x = 0.53$. Fig. 6 is a plot at −2 V of the current versus channel thickness for diodes

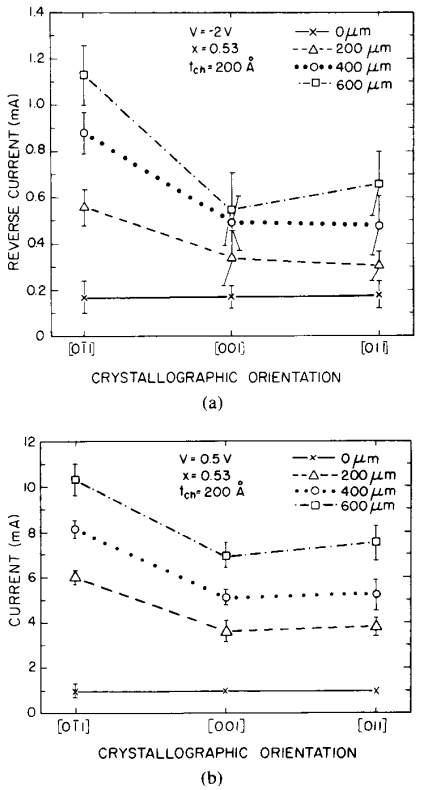

Fig. 5. A statistically averaged plot of diode currents in the [011], [001], and [0$\bar{1}$1] directions for (a) reverse (−2 V) and (b) forward (0.5 V) operation. Sidewall leakage shows dependence on crystallographic orientation and sidewall-overlap length.

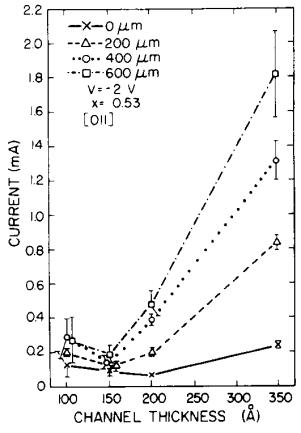

Fig. 6. A statistically averaged plot of diode currents at −2 V, showing that diodes with thicker channels are more sensitive to sidewall leakage.

along the [011] direction. The data have been averaged over four devices and clearly shows that an increase in channel thickness results in a larger sidewall-leakage current. The same is observed in forward bias. This means that a thicker channel results in a larger sidewall-contact area, as would be expected. For the 150-Å channel, the currents are close to the baseline area-leakage component.

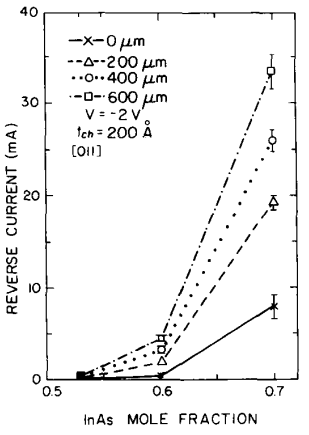

Fig. 7. A statistically averaged plot of diode currents −2 V, showing the enormous increase in sidewall-leakage current with InAs mole fraction in the channel.

In decreasing t_{ch} from 150 to 100 Å the currents increase, contrary to what is expected from the reduced sidewall contact area. We think this is due to channel quantization, which reduces the effective barrier height for both the sidewall- and area-related leakage components [11].

Increasing the InAs mole fraction x in the channel results in a drastic enhancement in sidewall leakage. This is because the Schottky-barrier height of metals on $In_xGa_{1-x}As$ decreases with x [6], [15]. Fig. 7 is a plot of reverse currents versus x at −2 V for [011] diodes with 200-Å channels. The data show that there is a phenomenal increase in the reverse sidewall-leakage current component (total current minus the baseline component) with x. Increasing x also drastically increases the forward-bias sidewall-leakage current, enough to significantly compromise the increase in ΔE_c between the $In_{0.52}Al_{0.48}As/n^+$-$In_xGa_{1-x}As$ heterojunction [16]. Fig. 8 shows the characteristics of typical diodes with t_{ch} = 200 Å and x = 0.53, 0.60, and 0.70, and L_s = 0 and 600 μm. Without sidewall overlap, the currents decrease with x, consistent with the larger ΔE_c. With sidewall overlap, however, the currents increase drastically for all x, more so for higher x.

The increased reverse currents from sidewall leakage result in increased currents at breakdown. Our results show that the sidewall-leakage path does not appear to result in premature breakdown in itself, however. Fig. 9 shows the reverse characteristics of diodes as a function of L_s for x = 0.53 and t_{ch} = 350 Å. Three regions are seen in order of increasingly negative voltage: (I) pre-threshold, (II) plateau, and (III) breakdown. The pre-threshold region is very sensitive to sidewall leakage. Beyond the device threshold voltage, the channel is pinched off and the sidewall-leakage current saturates. Sidewall leakage does not cause any further incremental increase in current. The characteristics for increasing L_s are just shifted down by the amount of pre-threshold leakage current, and the breakdown region begins at approximately

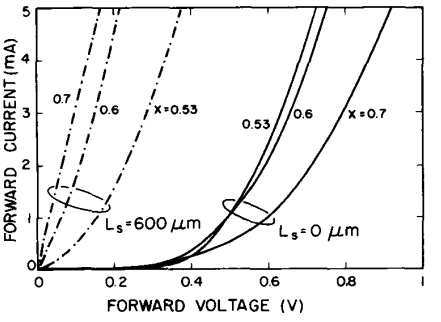

Fig. 8. Forward I–V characteristics of diodes with t_{ch} = 200 Å, x = 0.53, 0.60, and 0.70, and L_s = 0 and 600 μm along [011]. Sidewall overlap results in greatly increased leakage with x.

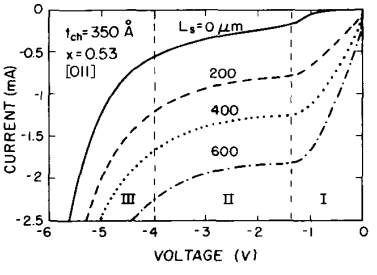

Fig. 9. Reverse I–V characteristics for diodes with x = 0.53 and t_{ch} = 350 Å. The pre-threshold regime (I) is particularly sensitive to sidewall leakage.

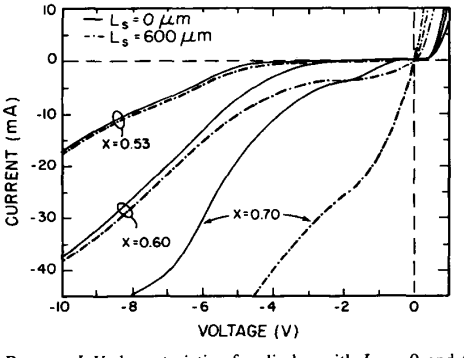

Fig. 10. Reverse I–V characteristics for diodes with L_s = 0 and 600 μm along [011], for t_{ch} = 200 Å and x = 0.53, 0.60, and 0.70. Sidewall leakage has a greater effect on breakdown for higher x.

the same voltage for all L_s. We have observed this effect for all our wafers.

If the breakdown voltage is defined at a certain value of reverse gate current, then sidewall leakage will degrade the breakdown voltage rating of the device. This degradation becomes particularly severe with increasing x, and is shown in Fig. 10. Fig. 10 shows the reverse I–V characteristics of diodes with W_{ch} = 200 Å and x = 0.53, 0.60, and 0.70, for L_s = 0 and 600 Å. The forward I–V characteristics of these diodes were shown in Fig. 8. With increasing x, the pre-threshold leakage current forms a greater portion of total reverse-leakage current. If we ar-

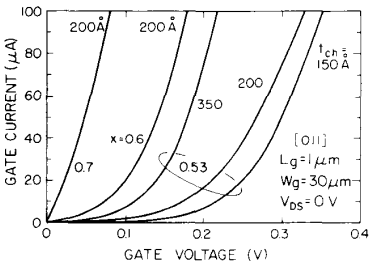

Fig. 11. Forward gate characteristics of HFET's with nominal $L_g = 1$ μm at $V_{ds} = 0$ V. The current increases with x and with t_{ch}.

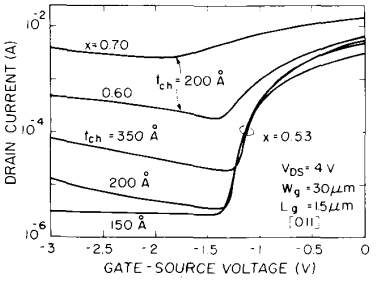

Fig. 12. A semilogarithmic plot of I_d versus V_{gs} for typical HFET's with a nominal L_g of 1.5 μm, at $V_{ds} = 4$ V. $I_{D(sub)}$ increases both with x and t_{ch}.

bitrarily define the breakdown voltage at a reverse current of 30 mA, at $x = 0.70$, sidewall leakage results in a significant degradation from −6 to −2.9 V.

B. HFET's

If the HFET's are affected by sidewall leakage, their gate characteristics should show the same dependences as the heterostructure diodes, i.e., gate-leakage current should increase with channel thickness, and drastically increase with x. Fig. 11 shows the forward gate characteristics of typical HFET's with $L_g = 1$ μm and $V_{ds} = 0$ V fabricated on the same wafers as the diodes presented above. With the exception of $t_{ch} = 100$ Å (not shown), the forward gate leakage increases with x and t_{ch}. This is precisely the behavior observed in the diodes with sidewall overlap (Figs. 6 and 8). From this dependence, we conclude that the HFET forward gate current is dominated by the sidewall-leakage path. This means that sidewall leakage degrades the gate isolation, reducing the forward gate drive that can be applied to the transistors. The 100-Å wafer has a higher leakage, probably due to channel quantization [11] (see Fig. 6).

When the transistor is turned off, reverse sidewall leakage might degrade HFET subthreshold characteristics, since both the drain and source are reverse-biased with respect to the gate. Excessive reverse sidewall leakage would result in a device unable to shut off. Fig. 12 is a semilogarithmic plot of the drain current I_d versus the gate–source voltage V_{gs} for typical HFET's with a nominal L_g of 1.5 μm, at $V_{ds} = 4$ V. Again, the 100-Å HFET has been left out due to its anomalous behavior. For $x = 0.53$, $I_{D(sub)}$ increases with channel thickness, consistent with our findings on diodes (Fig. 6). Enhancing x in the channel, while keeping t_{ch} constant at 200 Å results in a drastic increase in $I_{D(sub)}$, consistent with the observations for the diodes in Fig. 7. The drastic increase in $I_{D(sub)}$ with x is particularly disturbing, since devices with an enhanced InAs mole fraction in the channel have shown excellent transport properties, but have severely degraded reverse breakdown, subthreshold, and forward gate characteristics [4].

IV. Discussion

In order to confirm the physical origin of the sidewall-leakage current, we have extracted effective barrier heights ϕ_b from the diode I–V characteristics by extrapolating the forward I–V curve to 0 V using the method described in Yang [17]. The I–V characteristic for the metal–semiconductor junction is given by

$$I = I_0(e^{qV/nkT} - 1) \tag{1}$$

where I is the current, V the voltage, q the electron charge, n the ideality factor, T the temperature, and k the Boltzmann constant. I_0 may be extracted by plotting the I–V characteristic on a semilogarithmic scale and extrapolating the current to zero volts. I_0 is given by

$$I_0 = AR^*T^2e^{-\phi_b/kT} \tag{2}$$

where A is the diode area, R^* the effective Richardson constant, and ϕ_b the Schottky-barrier height. R^* is given by

$$R^* = \frac{4\pi q m_e^* k^2}{h^3} \tag{3}$$

where h is Planck's constant, and m_e^* the effective electron mass.

Using (1) and (2), barrier height extraction has been carried out at 300 K. The sidewall-leakage area was calculated by multiplying L_s by t_{ch} for each diode groove. This is an upper limit to the active contact area because of channel depletion. Depletion at the top and bottom of the channel could be caused by Fermi-level pinning at the InGaAs cap [7], and a degraded InAlAs/InGaAs reverse interface [18] between the buffer and channel. For diodes with $L_s = 0$ μm, the area used was 10 000 μm^2, the area-related component. The effective masses used to calculate R^* from (3) for the different InAs mole fractions were obtained by interpolating among $m_e^* = 0.067$ for $x = 0$, $m_e^* = 0.041$ for $x = 0.53$, and $m_e^* = 0.026$ for $x = 1$ [19]. We obtained $m_e^* = 0.038$ and 0.035 for $x = 0.60$ and 0.70, respectively.

These diodes are not ideal for extracting barrier heights and conduction band discontinuities due to voltage-dependent ideality factors, significant process-dependent parasitic resistances at the sidewall-overlap region, and heavy doping in a portion of the channel that might cause

tunneling. In addition, a change in channel depletion width caused by a change in gate-bias affects the effective sidewall-leakage area and the parasitic resistance of the channel. Our results should therefore be regarded as zeroth-order estimation of the effective barrier height. Diodes with sidewall-overlap should show ϕ_b closer to that of Au/InGaAs junctions (0.2 eV for $x = 0.53$ [15]) whereas diodes without sidewall overlap should show ϕ_b closer to the InAlAs/InGaAs conduction-band discontinuity (0.5 eV for $x = 0.53$ [12]).

Fig. 13 shows forward low-voltage I–V characteristics of typical diodes with 0 and 3 grooves, and channel thickness $t_{ch} = 200$ Å for $x = 0.53$, 0.60, and 0.70. The 3-groove diodes were chosen since they maximize the sidewall-overlap/diode-area ratio. We have used the low-voltage characteristics to minimize the effect of series resistance and to operate in a region where the area leakage does not contribute appreciably to the total leakage current in diodes with sidewall overlap.

The extracted barrier heights (ϕ_b) for diodes with $x = 0.53$ and varying t_{ch} are summarized in Table I. Table II shows ϕ_b with varying x for diodes with $t_{ch} = 200$ Å. Also shown in Table II are values of ϕ_b for $In_xGa_{1-x}As$ with $x = 0.53$, 0.60, and 0.70 from [15]. For $x = 0.53$, ϕ_b for $L_s = 0$ varies from 0.50 to 0.55 eV, regardless of the channel thickness (Table I). This is consistent with a ΔE_c of 0.5 eV for the $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ heterojunction [12]. With sidewall overlap ($L_s = 600$ μm), however, ϕ_b drops sharply to 0.11–0.13 eV. This is lower than the reported value of 0.2 eV [15], probably from tunneling due to the heavy channel doping. As x is increased, our extracted ϕ_b (for $L_s = 0$ μm) surprisingly decreases from 0.5 eV at $x = 0.53$ to 0.38 eV at $x = 0.70$ (Table II). This is contrary to reports in the literature [16], which indicate that ϕ_b should increase with x. Fig. 8 shows that our diodes with higher x have an increased forward-leakage current at low voltages. The increase in ΔE_c only becomes apparent once the diodes are fully turned-on. This increased low-voltage leakage current results in a lower extracted ϕ_b for higher x. The significant point, however, is that ϕ_b drops sharply to 0.13–0.064 eV with increasing x once sidewall overlap is introduced. The decrease in the barrier height of the metal–$In_xGa_{1-x}As$ junction with increasing x is consistent with values from the literature [15]. In all cases, the drastic reduction in ϕ_b with sidewall overlap is in agreement with the presence of a sidewall-leakage path.

To eliminate sidewall leakage from their HFET's, researchers use air bridging [8], [20], [21] or ion implantation [9], [22]. Air bridging is complex and ion implantation requires capital-intensive tools. The results from this work motivated us to recently develop a simple self-aligned method of eliminating sidewall leakage [23]. This method utilizes a succinic-acid-based selective etchant to selectively recess the exposed channel edge into the mesa sidewall. The subsequently electron-beam-evaporated metal does not enter the sidewall cavity, and remains isolated from the channel edge [23].

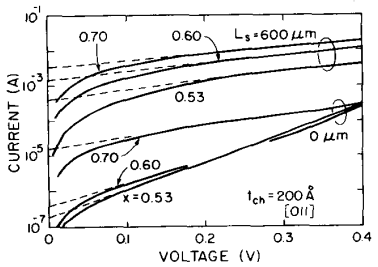

Fig. 13. A semilog plot of forward I–V characteristics of diodes with $L_s = 0$ and 600 μm, $t_{ch} = 200$ Å, and $x = 0.53$, 0.60, and 0.70. The calculated barrier heights drastically decrease in the presence of sidewall overlap.

TABLE I
EXTRACTED SCHOTTKY BARRIER HEIGHTS FOR DIODES WITHOUT ($L_s = 0$ μm) AND WITH ($L_s = 600$ μm) MESA SIDEWALL-GATE OVERLAP FOR WAFERS WITH $x = 0.53$ AND VARYING t_{ch}

	ϕ_b (Experimental)	
t_{ch} (Å)	$L_s = 0$ μm	$L_s = 600$ μm
100	0.55 eV	0.11 eV
150	0.52 eV	0.13 eV
200	0.50 eV	0.13 eV
350	0.52 eV	0.12 eV

TABLE II
SCHOTTKY BARRIER HEIGHTS ϕ_b FOR DIODES WITHOUT ($L_s = 0$ μm) AND WITH ($L_s = 600$ μm) MESA SIDEWALL-GATE OVERLAP FOR WAFERS WITH $t_{ch} = 200$ Å AND VARYING x AS WELL AS VALUES OF ϕ_b FOR $In_xGa_{1-x}As$ FROM THE LITERATURE [15]

	ϕ_b(Experimental)		Literature [15]
x	$L_s = 0$ μm	$L_s = 600$ μm	$\phi_b(In_xGa_{1-x}As)$
0.53	0.50 eV	0.13 eV	0.20 eV
0.60	0.48 eV	0.090 eV	0.13 eV
0.70	0.38 eV	0.064 eV	0.061 eV

V. CONCLUSION

At the mesa sidewall of InAlAs/InGaAs HFET's fabricated by conventional mesa isolation, there exists a parasitic gate-leakage path. This path is formed by the low Schottky contact of the exposed channel edge with the gate metallization. Using special diode test structures, we have shown that this sidewall-leakage current increases with sidewall-overlap length, channel thickness, and InAs mole fraction x in the channel, and shows a dependence on the crystallographic orientation of the sidewall. While barrier heights extracted from heterostructure diodes without sidewall overlap approach the InAlAs/InGaAs conduction-band discontinuity, barrier heights extracted from diodes with sidewall overlap are closer to those of Schottky barriers on $In_xGa_{1-x}As$. Sidewall leakage in HFET's results in increased forward and reverse gate-leakage currents, increased subthreshold currents, and a reduced breakdown voltage.

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Sandeep R. Bahl (S'84) was born in Delhi, India, on March 26, 1964. He was awarded the RPI International Scholarship to attend the Rensselaer Polytechic Institute, Troy, NY, and received the S.B. degree (summa cum laude) in electrical engineering in 1985. For his Bachelors project, he worked under Prof. S. K. Ghandhi on the characterization of OMVPE CdTe layers on GaAs. In 1988, he received the S.M. degree in electrical engineering from the Massachusetts Institute of Technology, Cambridge, MA. His research area was power electronics. For his thesis project, he designed and fabricated a silicon power MOSFET for use in a 10-MHz dc-dc converter.

He has now completed most of the requirements for the Ph.D. degree under Prof. J. A. del Alamo in the Electrical Engineering and Computer Science Department at MIT. His current research interests include device physics, modeling, and simulation; the growth and fabrication of InAlAs/InGaAs HFET's on InP, and their use in high-performance circuits.

Mr. Bahl is a member of Tau Beta Pi and Eta Kappa Nu.

Michael H. Leary was born in Newark, NJ, in 1969. He received the B.S. degree in electrical engineering, and the B.S. degree in physics from the Massachusetts Institute of Technology, Cambridge, in 1991.

He is currently pursuing the Ph.D. degree at Cornell University, Ithaca, NY. His current research is in the field of high-speed optoelectronics.

Jesús A. del Alamo (S'79–M'85) received the degree of Telecommunications Engineer from the Polytechnic University of Madrid, Madrid, Spain, in 1980, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1983 and 1985, respectively.

From 1977 to 1981 he was a research assistant at the Institute of Solar Energy of the Polytechnic University of Madrid, working on silicon solar cells. At Stanford University he carried out research for the Ph.D. dissertation on minority-carrier transport in heavily doped silicon and its relevance to bipolar transistors and solar cells.

From 1985 to 1988 he was research engineer with NTT LSI Laboratories in Atsugi (Japan) where he conducted research on heterostructure field-effect transistors (HFET's) based on InP, InAlAs, and InGaAs. Since 1988 he has been with the Department of Electrical Engineering and Computer Science of Massachusetts Institute of Technology as Assistant Professor, and from 1991, as Associate Professor. His current interests include high-performance HFET's based on compound semiconductors that contain In and novel quantum-effect devices with one-dimensional carrier confinement. He is the current holder of the ITT Career Development Professorship at MIT. In 1991, he was awarded the Presidential Young Investigator Award by NSF.

Dr. Del Alamo is a member of the American Physical Society and the Japanese Society of Applied Physics.