A Novel Analog-to-Digital Conversion Architecture Using Electron Waveguides

Cristopher C. Eugster, Peter R. Nuytkens and Jesús A. del Alamo

Department of Electrical Engineering and Computer Science
Massachusetts Institute of Technology, Room 13-3018, Cambridge, MA 02139

Abstract

We have demonstrated a novel analog-to-digital (A:D) conversion architecture based on the quantized conductance of electron waveguides. In our scheme, a dual electron waveguide (DWG) device implements a binary quantizer and encoder for one significant bit. The conductance values of the on and off states are $2e^2/h$ and zero, respectively. By cascading multiple DWG devices, higher order bits can be attained. In this paper, we demonstrate the first significant bit and the second significant bit for a 2-bit analog-to-digital converter using a DWG device fabricated in an AlGaAs/GaAs modulation-doped heterostructure.

Introduction

The recent excitement behind quantum-effect devices stems from their unique and prominent transport characteristics [1]. Such characteristics could potentially lead to more functional devices which would reduce the number of components necessary for today's complex circuits. In our work, we exploit the quantized conductance phenomena in electron waveguides to demonstrate a novel analog-to-digital (A:D) conversion scheme.

The most common way for implementing an electron waveguide is by using a split-gate field-effect transistor. In such a scheme, split-gates are patterned on top of a normally-on modulation-doped heterostructure. A negative gate voltage depletes the two-dimensional electron gas (2DEG) underneath the gates but leaves a narrow conducting channel in between. If the channel width is comparable to the electron wavelength ($\approx$ 500 Å), then electrons in the channel are only allowed to move in one dimension (1D). In addition, if the electrons travel through the channel without scattering, then the channel can be considered to be an electron waveguide [2].

In an electron waveguide, the 1D electronic subbands correspond to the transverse modes of the waveguide. The split-gate bias can modulate the electron population in the channel and thereby control the number of occupied 1D subbands or transverse modes. With the application of a drain-source bias, the resulting current through the waveguide increases in discrete steps as the subbands sweep below the Fermi level. Each step, when normalized by the drain-source bias, is a fundamental constant equal to $2e^2/h$ ($\approx 7.75\times10^{-5}S$) [3,4].

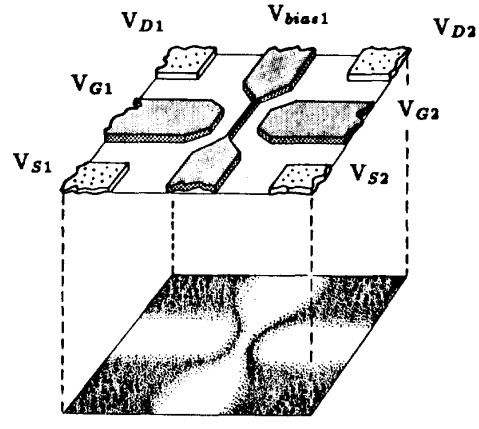

Fig. 1. A dual electron waveguide (DWG) device. Shaded regions represent electron concentration at the heterointerface of an AlGaAs/GaAs modulation-doped heterostructure.

The split-gate approach can be extended to implement a dual electron waveguide (DWG) device, shown in Fig. 1, in which two electron waveguides are formed in close proximity to each other using a three-gate configuration [5]. The two side-gates are used to independently modulate the electron concentration in the respective waveguides and the middle-gate is used to provide isolation between the two waveguides. The conductance for each waveguide in an actual DWG device is shown in Fig. 2 [5].

In this paper, we use the unique double staircase I-V characteristics of a DWG device to implement both a quantizer and binary encoder for an analog signal.

0-7803-0817-4/92 $3.00 © 1992 IEEE

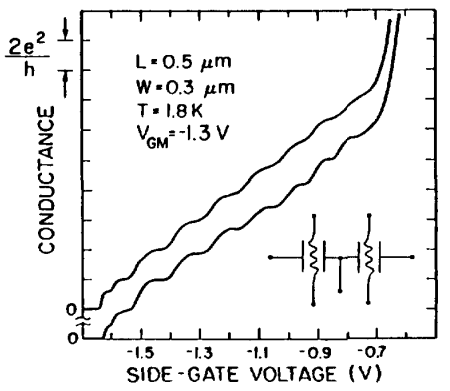

Fig. 2. I-V characteristics of a dual electron waveguide device. Device schematic shown in inset.

Analog-to-Digital Conversion Scheme

We obtain a single bit of the binary code by using a subtraction scheme in which properly weighted staircase I-V characteristics of two electron waveguides in a DWG device are subtracted from one another. The circuit necessary to implement this single stage is shown in Fig. 3.

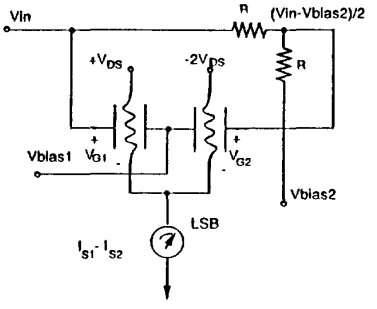

Fig. 3. Circuit for one significant bit.

As seen in Fig. 3, the input signal voltage V_{in} is applied directly to the first side-gate and through a divide-by-two voltage divider to the second side-gate. The middle-gate is kept at a fixed negative voltage V_{bias1} below threshold in order to keep the two waveguides isolated from one another. Since there is a linear relation between the width of the channel and the gate voltage, the staircase I-V characteristics will be twice as long in gate voltage for the second waveguide. An offset bias V_{bias2} is needed to line up the staircases of the two waveguides. In addition, the drain-source bias of the slower varying second waveguide is twice that of the first waveguide. One of the drain-source biases is inverted with respect to the other so as to achieve a subtraction of the two staircases. In this way, the combined current measured at the output of the two waveguides is the single bit for that stage.

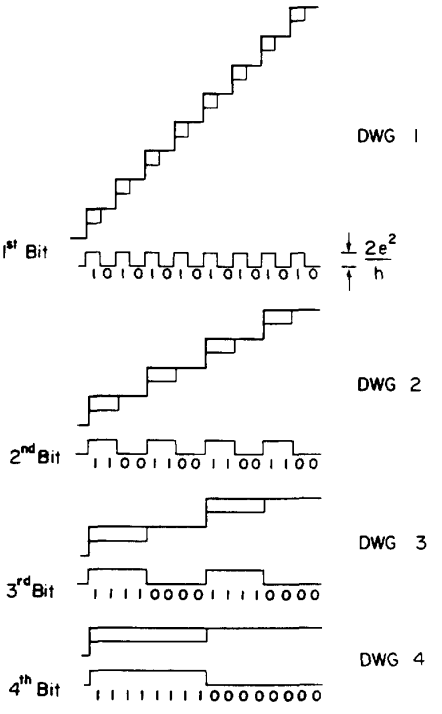

Fig. 4. Illustration of subtraction scheme of I-V characteristics for first, second, third, and fourth bit of a 4-bit A:D converter.

Fig. 4 illustrates the subtraction scheme of the staircase I-V characteristics in the implementation of a 4-bit A:D converter. The weighted staircases necessary for the first bit are shown in the first pair of overlapping staircases in Fig. 4. With the addition of two more waveguides, or one more DWG device, in which the side gate-voltages are again divided, we can implement the second pair of staircase I-V characteristics in Fig. 4 to obtain the next

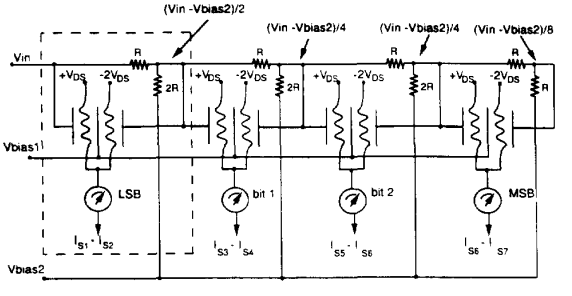

Fig. 5. Extention to a 4-bit A:D converter.

significant bit. As seen by the rest of Fig. 4, with additional DWG device stages we can attain higher order bits. Each bit representing the on-state has a conductance value of $2e^2/h$. The circuit in Fig. 5 shows how cascading the single stage in Fig. 3 results in a 4-bit A:D converter.

Our scheme has the potential to scale to higher order bits utilising a relatively small number of devices. The limitation to cascading arbitrary number of stages will be the number of steps in the I-V characteristics of the waveguides. Table 1 shows the number of steps as well as the number of DWG devices required to implement an A:D converter with arbitrary number of bits. For example, a 4-bit A:D converter requires 16 conductance steps and 4 DWG devices. This is close to the maximum number of conductance steps which have been observed using the split-gate scheme [3]. Therefore, additional circuit techniques are required to scale beyond 4 or 5 bits.

Table 1

No. of Bits	No. of Steps	No. of Devices
2 bits	4 steps	2 DWGs
3 bits	8 steps	3 DWGs
4 bits	16 steps	4 DWGs
5 bits	32 steps	5 DWGs
.	.	.
n bits	2^n steps	n DWGs

Fabrication

We fabricated [5,6] our devices using a high mobility AlGaAs/GaAs modulation-doped heterostructure. The mobility of the sample of the 2DEG is $1.2 \times 10^6 \frac{cm^2}{V-sec}$ and the carrier density is 4.2×10^{11} cm^{-2} at T=4 K. Mesa isolation, ohmic contacts and gate pads are done using optical lithography. The actual split-gate configuration, shown in Fig. 6, is fabricated using electron-beam lithography. The lithographic device dimensions are defined as L representing the length of the confining split-gates and W as the distance between the side-gate and the middle-gate.

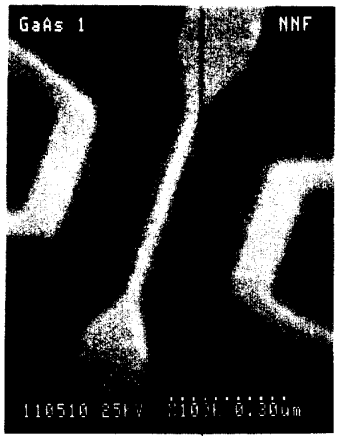

Fig. 6. Scanning electron micrograph of confining split-gates.

Results

We use an L=0.5 μm, W=0.4 μm AlGaAs/GaAs dual electron waveguide device to demonstrate our A:D conversion scheme. The device is initially biased to show the staircase characteristics necessary for the first significant bit as well as the second significant bit. We then implement the circuit in Fig. 3 to measure the individual bits. The input signal applied to the gates is a negatively sweeping bias. All measurements are carried out using lockin amplifiers at T=1.6 K.

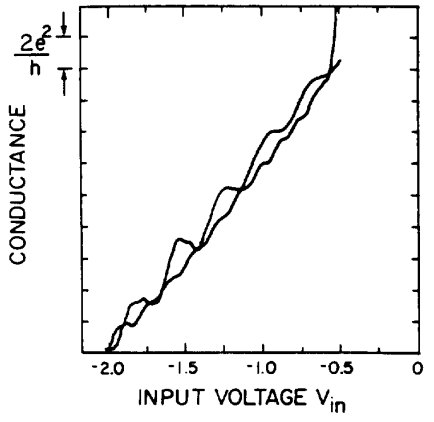

Fig. 7a. Measured I-V characteristics to implement first bit.

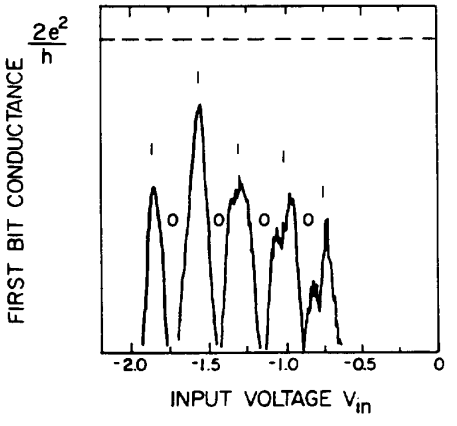

Fig. 7b. Measured first bit series using Fig. 3 circuit.

The ramp input signal is applied to the side-gates through the binary-ratioed resistor ladder discussed in the previous section (R is equal to 1 kΩ for the divider in Fig. 3). The drain-source bias (200 μV) across the slower varying waveguide is twice that of the other waveguide (100 μV). In this way, we are able to engineer the conductance steps for the two waveguides to give the I-V characteristics shown in Fig. 7a. By implementing the circuit in Fig. 3 and inverting one of the drain-source biases, we measure the subtraction of the two staircase characteristics in Fig. 7a. The resulting first bit series is shown in Fig. 7b.

By sending the input signal through an additional divide-by-two voltage divider (R is equal to 130 Ω for this divider) before the above 1 kΩ divider, we achieve the properly weighted staircase features for the second bit, shown in Fig. 8a. The measured second bit series is shown in Fig. 8b.

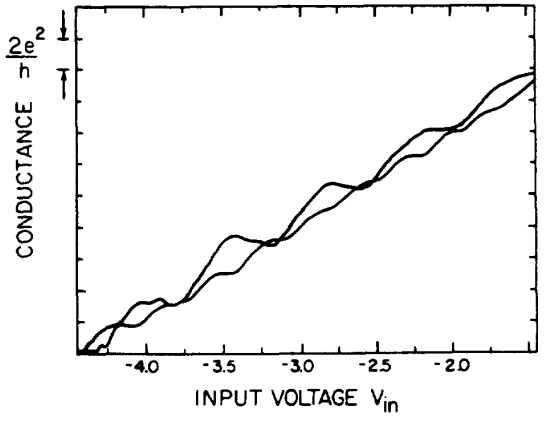

Fig. 8a. Measured I-V characteristics to implement second bit.

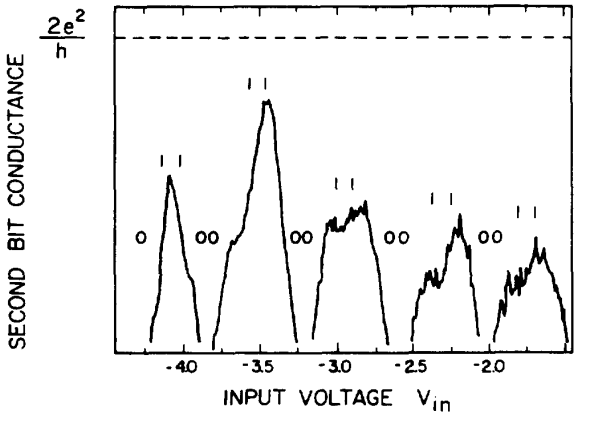

Fig. 8b. Measured second bit series using Fig. 3 circuit.

Fig. 7b and 8b show clearly distinguishable bits. However, the bits deviate from the ideal $2e^2/h$ values due to the lack of perfect conductance quantisation of the electron waveguides. This arises from finite scattering in the electron waveguides which causes the transmission coefficient for the different modes to deviate from unity [7].

The lack of robustness in quantum-effect features does raise serious questions on the practicality of such devices. Impurities and nonidealities have very strong effects on electron waveguides. It has been shown that even a single scatterer can severely degrade the conductance quantisation [7]. Our A:D conversion scheme might be somewhat immune to this problem since only a small number of devices is required. This makes it more likely to have impurity-free circuits.

Conclusion

We have demonstrated a novel analog-to-digital conversion architecture based on the quantised conductance of electron waveguides. This is the first electronic circuit ever demonstrated that utilises electron waveguide devices.

Acknowledgments

We would like to acknowledge M. R. Melloch for the sample growth and M. J. Rooks (NNF) for the electron-beam lithography. This work has been funded by NSF contracts 87-19217-DMR, DMR-9022933 and by NSF PYI Award 9157305-ECS.

References

[1] C. W. J. Beenakker and H. van Houten, Solid State Physics, eds. Ehrenreich and Turnbull (Academic Press, 1991), p. 1.

[2] G. Timp, R. Behringer, S. Sampere, J. E. Cunningham, and R. E. Howard, *Nanostructure Physics and Fabrication*, eds. M. A. Reed and W. P. Kirk, (Academic Press, 1989), p. 331.

[3] B. J. van Wees, H. van Houten, C. W. J. Beenakker, J. G. Williamson, L. P. Kouwenhoven, D. van der Marel and C. T. Foxon, *Phys. Rev. Lett.* **60**, p. 848, 1988.

[4] D. A. Wharam, T. J. Thornton, R. Newbury, M. Pepper, H. Ahmed, J. E. F. Frost, D. G. Hasko, D. C. Peacock, D. A. Ritchie and G. A. C. Jones, *J. Phys. C* **21**, L209, 1988.

[5] C. C. Eugster, J. A. del Alamo, M. J. Rooks and M. R. Melloch, *Appl. Phys. Lett.* **60**, p. 642, 1992.

[6] M. J. Rooks, C. C. Eugster, J. A. del Alamo, G. L. Snider and E. L. Hu, *J. Vac. Sci. Tech. B* **9**, p. 2856, 1991.

[7] C. C. Eugster, J. A. del Alamo, M. R. Melloch and M. J. Rooks, *to appear in Phys. Rev. B*, October 1992.