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A HIGH-VOLTAGE, DOUBLY-STRAINED $In_{0.41}Al_{0.59}As/n^+$–$In_{0.65}Ga_{0.35}As$ HFET

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Abstract: An InAlAs/n^+-InGaAs HFET on InP, suitable for power microwave applications, was designed and fabricated. A strained $In_{0.65}Ga_{0.35}As$ channel is optimally doped to $N_D=6\times10^{18}$ cm^{-3}. The heterostructure employs the following methodology to enhance device breakdown: 1) an ultrathin subchannel to introduce quantization and increase the effective channel bandgap, 2) a strained $In_{0.41}Al_{0.59}As$ insulator, and 3) the elimination of parasitic mesa-sidewall gate-leakage. The resulting device (L_g=1.9 μm, W_g=200 μm) has f_t=14.9 GHz, f_{max}=*101 GHz*, V_B=12.8 V, and $I_{D(max)}$=302 mA/mm.

Introduction

InAlAs/InGaAs HFET's (Heterostructure FET's) on InP have recently emerged as an optimum choice for a variety of microwave and photonics applications. Unfortunately, the low breakdown voltage of InAlAs/InGaAs MODFET's on InP (typically less than 5 V [1]) severely restricts their use in high-power applications, such as large-signal microwave amplification and laser driving. It also forces the use of a separate high voltage supply to operate MSM photodetectors in InP photonics receivers.

A device with great potential for power handling is the InAlAs/n^+-InGaAs MIDFET (Metal Insulator Doped-channel FET), by virtue of its undoped insulator and thin, heavily-doped channel. In this structure, the breakdown voltage, V_B, is not only large but we have previously shown that it can be engineered using pseudomorphic insulators [2] and channel quantization [3]. Drain current, I_D, transconductance, g_m, and cutoff frequency, f_t, can also be increased with InAs-rich channels [4, 5]. The attainment of high power, however, demands a large $I_D \times V_B$ product. InAs-rich channel devices unfortunately suffer from a low breakdown due to the reduced bandgap of the material [6] and severe gate leakage at the sidewall of the mesa, where the gate comes in contact with the heavily-doped channel [4].

To maximize I_D and f_t, while maintaining a high V_B, we designed a doubly-strained $In_{0.41}Al_{0.59}As/n^+$-$In_{0.65}Ga_{0.35}As$ HFET. The high InAs-mole fraction in the channel provides a boost to f_t and $I_{D(max)}$, while the $In_{0.41}Al_{0.59}As$ insulator forms part of a methodology to enhance the breakdown voltage. The remaining methodology features a thin subchannel to introduce electron quantization in the channel and increase its effective bandgap [3], and a novel fabrication technique to eliminate mesa-sidewall gate leakage [7].

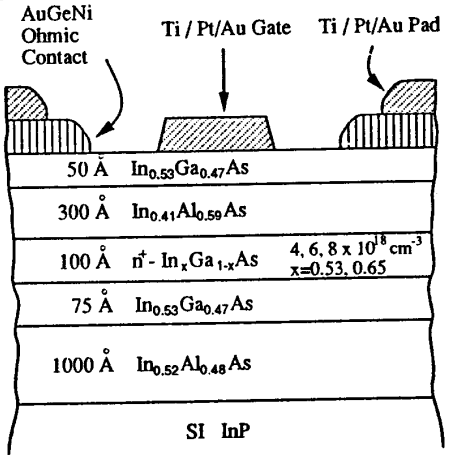

Figure 1: Cross-section of device structure.

Experimental

Four wafers were grown on S.I. InP by MBE with the cross section shown in Fig. 1. The first three had channels lattice-matched to InP (x=0.53), and comprised a doping optimization experiment. The fourth had an InAs-enriched (x=0.65) channel (hereafter called the Hi-In wafer). The heterostructure consists of (bottom to top), a 1000 Å $In_{0.52}Al_{0.48}As$ buffer, a 75 Å $In_{0.53}Ga_{0.47}As$ subchannel, a 100 Å n^+-$In_xGa_{1-x}As$ Si-doped channel, a 300 Å $In_{0.41}Al_{0.59}As$ strained insulator, and a 50 Å $In_{0.53}Ga_{0.47}As$ cap. The channels for the doping experiment were nominally doped to 4, 6, and 8×10^{18} cm^{-3}. From these wafers an optimized doping of 6×10^{18} cm^{-3} was determined. The Hi-In wafer was grown at this channel doping. During this growth, the Si-cell temperature was reduced to compensate for the lower $In_{0.65}Ga_{0.35}As$ growth rate.

The insulator composition was chosen to avoid misfit dislocations while providing maximum conduction band discontinuity [2, 8, 9]. The subchannel thickness was minimized without significantly degrading current driving capability [3]. For the Hi-In device, the InAs mole fraction of x=0.65 was chosen just below the Matthews-Blakeslee critical-layer limit [8]. Double-crystal X-ray diffraction was performed to investigate the crystalline quality of the material and determine the insulator composition. Fig. 2 shows the experimental and simulated rocking curves for

Table 1: Figures of merit for DC (W_g=30 μm) devices

x	N_D (cm^{-3})	$I_{D(max)}$ (mA/mm)	$g_{m(peak)}$ (mS/mm)	V_T (V)	V_B (V)	R_s ($\Omega \cdot mm$)	n_s (cm^{-2})	μ ($cm^2/V \cdot s$)
0.53	4×10^{18}	122±16	122±7	-0.78±0.07	21.1±2.5	3.47±0.31	1.23×10^{12}	4032
	6×10^{18}	215±13	200±9	-0.77±0.04	15.6±3.5	2.49±0.01	1.32×10^{12}	4447
	8×10^{18}	362±47	182±8	-1.47±0.12	5.3±0.5	1.18±0.10	3.12×10^{12}	3528
0.65	6×10^{18}	271±30	202±12	-1.19±0.11	12.8±3.1	2.10±0.02	2.06×10^{12}	3664

the Hi-In heterostructure. Even though the insulator exceeds its critical layer thickness, we deduce that the heterostructure is coherent because the full-width half-maximum of the $In_{0.41}Al_{0.59}As$ peak (520 arc-seconds) is very close to its simulated value of 500 arc-seconds, and there are prominent Pandellosung fringes [8]. The absence of misfit dislocations was further confirmed by the absence of surface ridges on the unprocessed sample under dark-field optical microscopy [9].

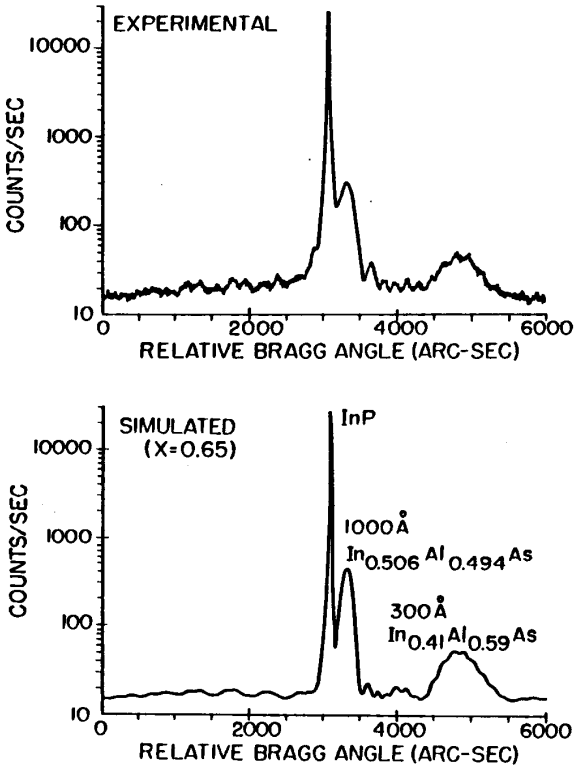

Figure 2: (a) Double-crystal x-ray rocking curve for the Hi-In heterostructure and (b) simulated fit with an $In_{0.41}Al_{0.59}As$ insulator and $In_{0.65}Ga_{0.35}As$ channel.

Devices were fabricated by first chemically etching a mesa down to the InP substrate. Then, before removing the mesa-level photoresist mask, the wafer was dipped for 40 sec. into a SA:H_2O_2 6:1 solution [7, 10] to selectively etch the exposed portion of the InGaAs channel. The SA solution was prepared by adding 1 liter H_2O to 200 g. succinic acid with the addition of ammonium hydroxide until the pH was 5.5. A planar selectivity of 23:1 was measured, with the $In_{0.52}Al_{0.48}As$ etching at 25 Å/min. We have confirmed that this technique completely eliminates sidewall-leakage in all crystallographic directions on the (100) surface [7]. For the ohmic contacts, 600 Å Ge, 1200 Å Au, and 300Å of Ni were evaporated, lifted off, and RTA alloyed at 385°C for 10 sec. For the gate, 300Å of Ti, 300 Å of Pt, and 2500 Å of Au were e-beam evaporated and lifted off. This metal scheme, with a Au thickness of 3500 Å, was then used for the pads.

Results and Discussion

Measurements are reported for HFET's with (optically measured) 1.9 μm gate length (L_g) and gate widths (W_g) of 30 μm (DC devices) and 200 μm (microwave devices). The sheet carrier concentration, n_s, and mobility, μ, were measured on a Hall-bar fabricated alongside the HFET's. Statistical values of $I_{D(max)}$, $g_{m(peak)}$, and V_T were obtained by averaging over 10 DC devices. V_B for the DC devices was measured from the gate I-V characteristics at V_{DS}=0 V. Table 1 shows V_B values averaged over 5 DC devices. The values of $I_{D(max)}$, $g_{m(peak)}$, threshold voltage V_T, source resistance R_s, n_s, and μ are also shown.

Fig. 3 shows the I_D vs V_{GS} characteristics of typical devices from each wafer. $I_{D(max)}$ increases with both doping and InAs mole fraction in the channel. A benefit of the AlAs–rich insulator is the expanded range over which I_D increases with V_{GS} [2]. We find that (not shown) the drop in I_D is due to real-space transfer of electrons from the channel to the gate. Increasing the AlAs mole fraction of the insulator delays the onset of real-space transfer to higher V_{GS}, thereby increasing $I_{D(max)}$ [2].

Fig. 4 shows the g_m vs. V_{GS} characteristics for these HFET's. For x=0.53, $g_{m(peak)}$ is maximized for a nominal doping of 6×10^{18} cm^{-3}. This value of $g_{m(peak)}\approx$200 mS/mm does not show any change with x. Hall measurements showed that for x=0.53, increasing the nominal doping from 4 to 6×10^{18} cm^{-3} increases the sheet charge density only slightly, from 1.23 to 1.32 $\times10^{12}$ cm^{-3}. This is consistent with these devices having the same V_T.

Although higher channel doping results in higher $I_{D(max)}$, it also results in lower V_B. Fig. 5 shows typical gate-diode (V_{DS}=0 V) I-V characteristics of HFET's

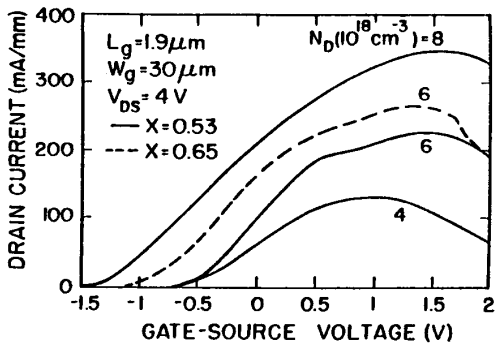

Figure 3: I_D vs. V_{GS} for V_{DS}=4 V.

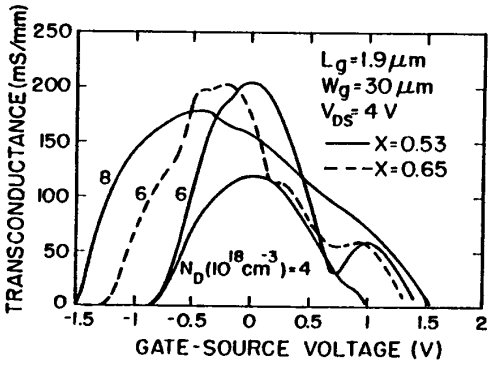

Figure 4: g_m vs V_{GS} at V_{DS}=4 V.

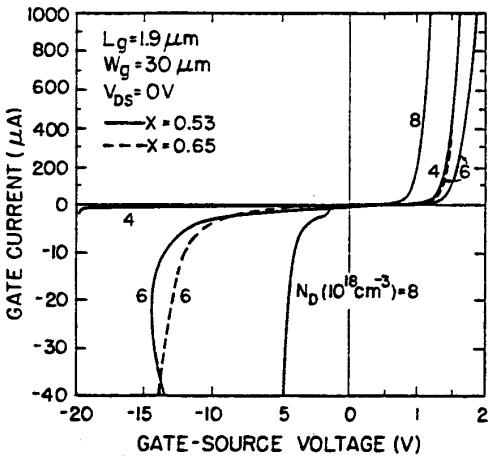

Figure 5: Forward and reverse gate-diode I-V characteristics for V_{DS}=0 V.

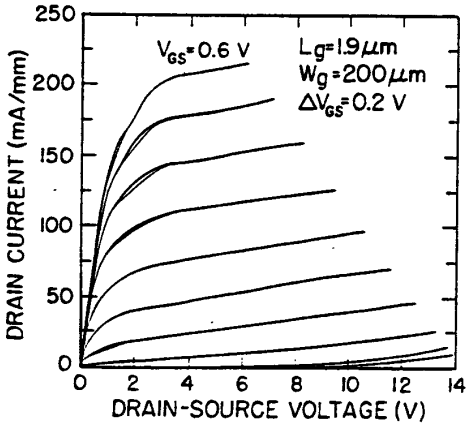

Figure 6: Output I-V characteristics of Hi-In HFET (x=0.65). This device broke down at V_{DS}=14 V.

from the four wafers. We find that V_B decreases rapidly with channel doping (Table 1). The optimal doping of 6×10^{18} cm^{-3} was chosen to maximize current, while retaining high breakdown. With increasing x, however, V_B decreases only slightly. This result is in contrast with our earlier studies [4] and signifies the successful application of our breakdown enhancement methodology.

The forward-gate characteristics exhibit high turn-on voltages (0.8–1.4 V). This is a benefit of the increased ΔE_c offered by the AlAs–enriched insulator [2], which is apparent only in the absence of sidewall-leakage. Sidewall-leakage is especially severe for Hi-In channels [4], and would mask the high ΔE_c because this parasitic path turns on near zero volts [2].

Results for individual microwave devices from each wafer (W_g=200 μm) are tabulated in Table 2. V_B here is defined as the drain-to-source breakdown voltage of the output I-V characteristic at 5% of $I_{D(max)}$. The power density, W, is calculated by multiplying $1/8\cdot I_{D(max)}\cdot[V_B - V_{DS(sat)}]$, where $V_{DS(sat)}$ is the drain-source voltage at which I_D falls to 90% of its maximum value. The results show that higher doping results in a lower W, but better RF performance. With increased x, however, we find an improvement in both W and RF performance. The Hi-In device has a breakdown voltage of 12.8 V, a power density of 0.4 W/mm, f_t of 14.9 GHz and f_{max} of *101 GHz*. The output I-V characteristics (on an identical device on the next die, since this device was destroyed during the measurement) are shown in Fig. 6. Fig. 7 is a graph of H_{21} and MAG of the Hi-In device listed in Table 2. The high f_{max} is a consequence of low g_d (DC value of 0.9 mS/mm at the peak f_t bias point of V_{DS}=4.5 V, V_{GS}=0.4 V) as this device is probably entering accumulation at $V_{GS} \geq$ 0 V [11]. This is shown by the sudden rise in both f_t and f_{max} at $V_{GS}\approx$0 V (Fig. 8). The DC voltage gain when biased for peak f_t is 150. For this device, we calculate an electron velocity of 1.8 $\times10^7$ cm/sec and an $f_t\times L_g$ product of 28.3 GHz·μm. These values are comparable to those obtained on lattice-matched MODFET's of similar L_g [12]; however, the power density and breakdown voltage are 2-3 times better [12]. High electron confinement and reduced gate leakage in our HFET's are instrumental in obtaining high f_t and f_{max}, and in mitigating the degradation in V_B from enriching the InAs mole fraction in the channel.

Table 2: Figures of merit for microwave (W_g=200 μm) devices

x	N_D (cm^{-3})	$I_{D(max)}$ (mA/mm)	$g_{m(peak)}$ (mS/mm)	V_T (V)	V_B (V)	W (W/mm)	f_t (GHz)	f_{max} (GHz)
0.53	4×10^{18}	159	131	-0.85	19.3	0.37	9.2	34
	6×10^{18}	194	172	-0.72	14.3	0.30	11.3	42
	8×10^{18}	413	196	-1.60	4.8	0.14	12.8	68
0.65	6×10^{18}	302	190	-1.24	12.8	0.40	14.9	101

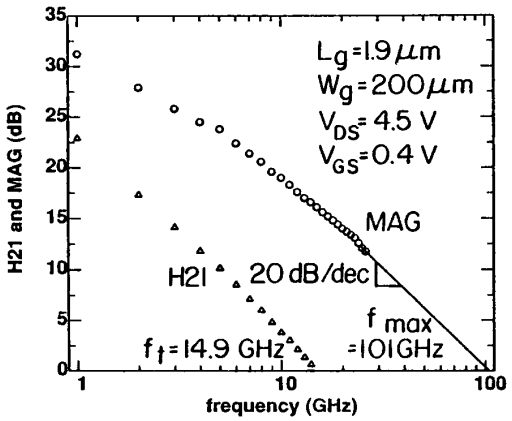

Figure 7: H_{21} and MAG vs. frequency for Hi-In (x=0.65) HFET with L_g=1.9 μm and W_g=200 μm.

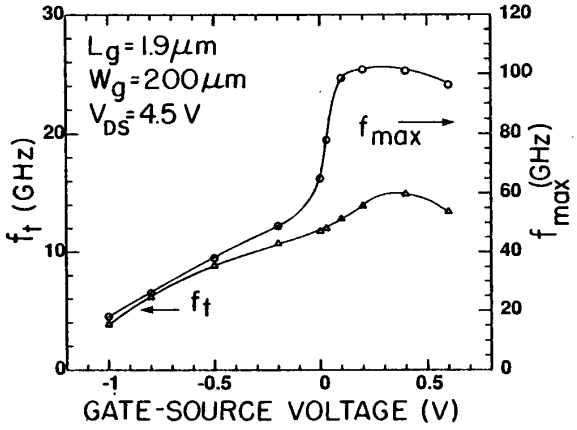

Figure 8: f_t and f_{max} vs. V_{GS} for Hi-In (x=0.65) HFET. The rise in f_t and f_{max} indicates that the HFET is entering accumulation at $V_{GS}\geq0$ V.

Conclusion

In conclusion, in the pursuit of high-power InAlAs/InGaAs HFET's, we have combined for the first time in a single device, an optimized heavily-doped channel, an AlAs enriched insulator, an InAs enriched channel, channel quantization, and mesa-sidewall leakage elimination. We have thereby been able to fabricate a high-voltage device with excellent microwave characteristics. Scaled down versions of this device are very promising for high-power microwave and photonics applications.

Acknowledgements

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