A Process Control Methodology Applied to Manufacturing GaAs MMIC's

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***Abstract*—A methodology for guiding process-driven manufacturing organizations in instituting process control on a facility-wide basis is proposed. The methodology begins with a definition of the customer's expectations and of the manufacturing process used to meet these expectations. The output, of a given process or subprocess must reach four progressive levels of control. When the output can be reliably measured, it is considered *measureable*. The second level is reached when this output, viewed in aggregate and over time, is found to be *predictable*. When the distribution of outputs is centered within the spec limits and a "sufficient" fraction of the output lies within the spec limits, the process is considered *acceptable*. Finally, when the process, as it is currently operated, is fully documented and operator technique is passed on through training, the process reaches the fourth and final level of control, *recoverable*. An application of this methodology to the control of submicron gate lithography on a GaAs monolithic microwave integrated circuits (MMIC) process at Hewlett-Packard's Microwave Technology Division is discussed.**

I. Introduction

WELL-controlled processes have been shown to be economically and stategically beneficial to the long-term competitive abilities of a firm, yet many firms—particularly American ones—have made little progress in improving the level of control of their manufacturing processes [1]. While process control is a primary goal in some of these organizations and many useful tools are available to assist in accomplishing process control, many organizations still fail to realize substantive improvement. Experience at Hewlett-Packard suggests that a significant barrier to further progress is the lack of a clear conceptual guide for managing the introduction and integration of process control techniques to an organization. The many false starts made by organizations in pursuing process control suggests the need for a clearer conceptual guide for managing this organizational change.

Prior work on the control of manufacturing processes is quite extensive. Most of this work has focused on tools, such as control charts, histograms, and pareto charts, that play a specific, but limited role in achieving process control. More recently, researchers such as Taguchi have added new tools to the field with improved experimental techniques and more explicit evaluations of the "quality loss" [2]. While many such tools are useful in achieving process control, they emphasize localized optimization of some aspect of a single process, to the possible detriment of an organization wide process control optimum. Furthermore, none of them consider the broader question of how a manufacturing organization, set in a pattern of operation that has not emphasized process control in the past, goes about defining what it means by process control and incorporating available tools into its daily operations to achieve such control. Meanwhile, a few management researchers, most notably Bohn [3], have demonstrated the value of process control by identifying a link between environmental noise (which is a function of the degree of process control) and the speed of organizational learning. However, little has been written on how to guide an organization in adopting available tools and managing the pursuit of process control, despite the indication that the selection of a guiding strategy may be one of the most critical aspects in successfully attaining process control.

Efforts to define and use such an organizational guide have been undertaken by a joint industry/academia team at Hewlett-Packard's Microwave Technology Division (MWTD). The Division supplies a wide variety of leading edge, solid state components operating in the Radiowave, Microwave, and Lightwave frequency ranges to Hewlett-Packard's instrument divisions. The growing number of processes supported and the increasing volume of devices produced at MWTD has placed an increasing emphasis on process control as a necessary element in providing these devices reliably and at costs competitive with external sources. From MWTD's attempts to improve process control has grown the measureable, predictable, acceptable, and recoverable (MPAR) methodology that now guides the division's efforts to define,

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institute, and continually improve its level of process control.

This paper describes the MPAR methodology and its application to the control of submicron gate lithography for the production of GaAs monolithic microwave integrated circuits (MMIC's). The paper also includes a discussion of the impacts on the organization of using the MPAR process.

II. Overview of the MPAR Methodology

Experience at MWTD has suggested that efforts to utilize existing statistical and experimental tools to improve process control often suffer on three fronts:

1) Control of complex, multistep processes, well beyond the scope of a single individual, cannot be readily broken down into discrete pieces such that realistic responsibility for a process unit can be assigned to a single engineer.

2) While most engineers and operators are at least exposed to current statistical and experimental techniques, such techniques are used only sporadically and acceptance is slow.

3) Management, faced with an extremely broad array of processes, each in different stages of a life-cycle, cannot readily and with confidence manage process improvement.

The MPAR methodology addresses these three problems by providing, on a consistent basis throughout the organization:

- a definition of "process" and "process control,"
- a conceptual methodology to assure that process improvement follows an orderly procedure, and
- a simple, clear procedure to measure the level of control over several processes.

The MPAR methodology starts by identifying the customer's expectation for the product. It then focuses on a specific process that is desired to be brought under control. The customers expectations for the product need to be translated into process specifications. Control in meeting these expectations must reach four progressive levels. When the output can be reliably measured with known accuracy, it is considered *measureable*. The second level is reached when this output, viewed in aggregate and over time, is found to be *predictable*. When the distribution of outputs is centered within the spec limits and a "sufficient" fraction of the output lies within the spec limits, the process is considered *acceptable*. Finally, when the process, as it is currently operated, is fully documented and operator technique is passed on through training, the process reaches the fourth and final level of control, *recoverable*.

The next sections describe in detail the MPAR methodology and its applications to the critical gate manufacturing process of GaAs submicron metal-semiconductor field-effect transistors (MESFET's) at MWTD.

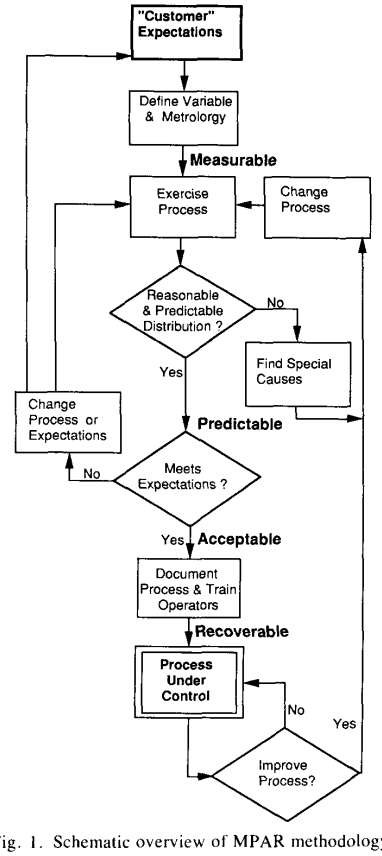

Fig. 1. Schematic overview of MPAR methodology.

III. Customer Expectations

The MPAR methodology, shown schematically in Fig. 1, begins with definition of who the "customer" is and definition of the customer's expectations. "Customer" is a figurative term that can represent the actual person receiving the finished product or, more often, the downstream process or coworker that is affected by the output of the process under consideration.

One relatively new and important fabrication process at MWTD is the MMIC-A process used to fabricate a variety of GaAs MMIC's. While MPAR is being gradually applied throughout the MWTD facility, an in-depth application was undertaken by examining the production of a primary electrical parameter of one part produced on the MMIC-A process [4].

Among the circuits produced on the MMIC-A process is a 2–26.5 GHz traveling-wave amplifier. One parameter of critical importance in Hewlett-Packard's microwave amplifier devices that require constant gain over a broad frequency range is the gain slope, defined as

$$\text{Gain Slope} = \frac{\text{Gain (max)} - \text{Gain (min)}}{\text{frequency range}} \quad (1)$$

where the frequency range is 24.5 GHz. Thus, an essential customer expectation of the traveling wave amplifier

is a small gain slope. Current devices demand a maximum to minimum range of no more than 0.9 dB over the entire frequency range.

While this expectation represents a suitable output of the MMIC-A process it has the distinct disadvantage that it can only be measured when the multistep fabrication process is completed. However, prior studies at MWTD of the circuit physics of this traveling wave amplifier demonstrated that gain slope is largely determined by the input capacitance of the MESFET's used to construct the amplifier circuit. In turn, MESFET device physics suggests that input capacitance is a strong function of gate length [5]. Using these relationships, the customer expectation for gain slope can be translated to a comparable expectation for a physical feature of the MESFET, the gate length with a target value of 0.42 μm. Control of gate fabrication processes then becomes central to control of gain slope.

IV. The Process

A "process" for these purposes is "a series of (repeated) actions used in manufacturing a desired product or product feature." Processes are hierarchical in nature in that they can be divided into a series of subprocesses, each of which can be considered a process unto itself. The methodology considers three types of processes that most directly affect the manufacture of saleable items:

1. Processes which add value to materials by either altering them, sorting them, or moving them closer to the customer application.
2. Processes which verify the product materials, processing equipment, or construction of the product; e.g., setting up a stepper for even field exposure.
3. Processes which alter data about the product materials, e.g., metrology, or metrology data storage and manipulation.

The application described in this paper has focused mainly on the first two types of processes; however, the MPAR methodology can be applied to all three types.

The MMIC-A process [6] requires the eleven masking levels outlined in Fig. 2. The critical gate region however, is fully formed after the fourth masking layer and changes little during subsequent processing. Initial processing begins by growing a doped GaAs active region on a semiinsulating GaAs substrate. Oxide is deposited by a chemical vapor deposition process to provide field passivation. Initial masking steps pattern the oxide deposition of ohmic contacts, proton isolation of active devices, and sputter deposition of a thin film resistor. At this point, wafers begin the critical processes that lead to gate formation (Figs. 3(a)–3(f) with final gate structure shown in Fig. 4).

Gate processing begins by spinning on a 0.6-μm polyimide layer to planarize the wafer surface (other surface features are about 0.2 μm off the active layer) and to provide a lifting medium for the transfer layer after the gate metal is deposited. After the polyimide is baked to provide stabilization, a 0.5-μm PMMA layer, is spun on to act as an imaging resist (see Fig. 3(a)). The PMMA is then baked, and the gate pattern is exposed with deep-

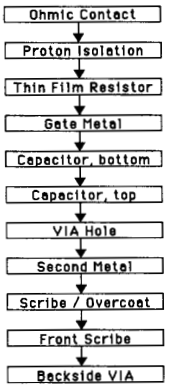

Fig. 2. MMIC-A process flow.

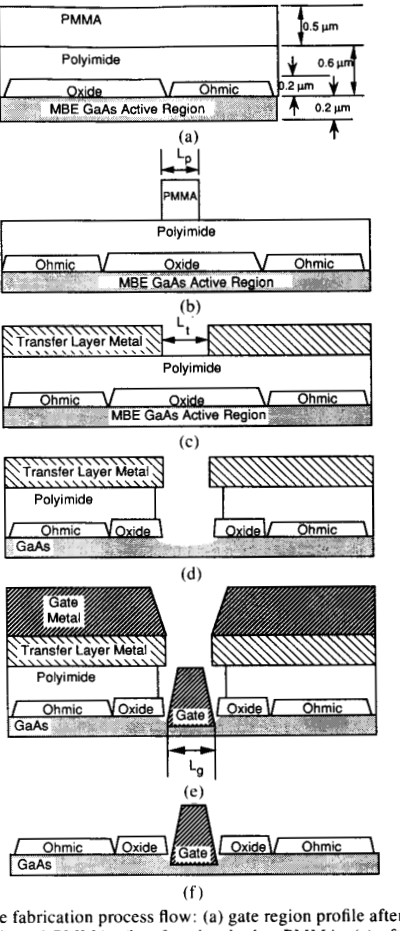

Fig. 3. Gate fabrication process flow: (a) gate region profile after spinning on Polyimide and PMMA, (b) after developing PMMA, (c) after evaporating transfer layer and lifting PMMA, (d) after etching polyimide, oxide, and active-GaAs, (e) after evaporating gate metal, (f) after lifting polyimide.

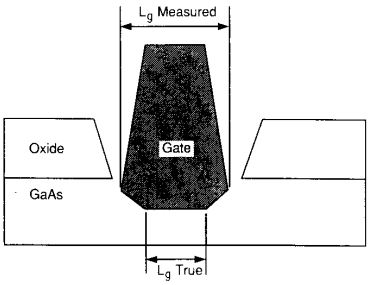

Fig. 4. Mushroom structure of MMIC-A process's gate.

ultra violet illumination on a contact lithography system. The process design attempts to keep exposure dose constant by calibrating the illumination level before every batch is run.

A standard developing solution is used to remove the exposed PMMA and leave a PMMA line. Batch-to-batch variation in developing is reduced by targeting the develop time before each new batch is processed using a silicon "dummy" wafer. Through successive develop cycles, PMMA line length on the dummy must be brought within the acceptable limits of 0.3 to 0.38 μm with a nominal target value of 0.35 μm. The cumulative develop time (nominal develop time is 120 s) seen by the dummy is then used to batch develop the actual product wafers (see Fig. 3(b)). It is assumed that this calibration corrects all batch-to-batch variability present in the develop process.

Subsequent processing seeks to transfer the current critical feature, the PMMA line, to an approximately equal line of gate metal. To accomplish this, a metal transfer layer is electron-beam evaporated, which since the PMMA is relatively thick and has a sharp profile, leaves a metal layer that is nonconformal after lifting the PMMA. A transfer layer opening remains (see Fig. 3(c)) and is the actual parameter selected as an in-process monitor of gate fabrication in this work, as discussed below. Reactive ion etching is used to transfer this pattern anisotropically through first the polymide and then the oxide. An isotropic wet etch process is used iteratively to etch the semiconductor and target the drain current, by controlling channel depth (see Fig. 3(d)). The gate metals are sequentially evaporated into this trench with the effective gate length controlled by the location of the transfer metal layer sidewalls, the steepness of the trench profile and the aperture in the evaporator (see Fig. 3(e)). Finally, the polyimide is lifted off to remove the transfer layer and the excess gate metal. This yields the final gate profile (see Figs. 3(f) and (4)).

Further details of this process can be obtained from [4].

V. The Four Levels of Process Control

When the process under study and the expectations of this process are defined, control of meeting these expectations is increased along four levels, as explained next (follow along with Fig. 1).

A. Measurable

The output(s) of concern to the customer must be defined precisely and a means for objectively and accurately assessing this output must be developed. Once done, the process or process step has reached the first level of process control, **measurable.**

This first level is often difficult to accomplish, particularly in semiconductor fabrication where the physics of working devices is not modeled with great accuracy and the physical features of interest increasingly range from submicron down to atomic scales. Measurement of relevant parameters is often difficult, inaccurate, unrepeatable, time consuming, and expensive.

With an expectation for the MMIC-A process comparable to the customer's, i.e., using transfer length as a proxy for gain slope, but measurable at a point in the process reasonably close to those subprocesses that actually determine the output of interest, attempts can now be made to make these subprocesses measurable. Unfortunately, due to the mushroom shape of the gate, gate length can only be measured accurately by scribing and breaking the wafer along the gate, a difficult and destructive process that forbids any further processing of the wafer. Since gate length is difficult to measure, it is useful to find an alternative process output that can be measured. A detailed study of the gate metal evaporation process suggests that gate length should be closely related to transfer layer length for this MMIC-A process, making transfer layer length a suitable output to measure to achieve control of gain slope (see Fig. 3(c)–3(e)). Current processing calls for five sites per wafer on each production wafer to be measured for transfer layer length using a scanning electron microscope that provides accuracy and repeatability better than 0.015 μm, which is within the allowable variability. Consequently, we can consider the gate formation process to be "measureable." Note that the method used to make this process measurable is not unique. One could use a variety of other metrology methods, from optical microscopy of transfer layer length to electrical probing of a test cell specifically designed to approximate the gate length [7].

B. Predictable

Once a particular process is measurable, it is exercised over a period of time during which data is collected to study the output. This repeated exercising allows observation of the natural variation of the process. Here prior research is useful in defining a "statistically significant sample" of measures of the output [8]. When a sufficient data set has been taken, one examines the data to see if the distribution is reasonable and expected. Here again many well-known tools, such as tests for normality, are available to assist in determining whether a distribution is reasonable [8]. Proper application of these tests requires the choice by the engineer or operator of a suitable physical or mathematical model of the process. Such models suggest a particular type of distribution, such as normal or bimodal, for which a statistical test can be applied.

When the distribution of a statistically significant sample of the measured output does not meet expectations for these types of processes, further exploration and experimentation must be done to find the causes of unexpected behavior and the process must be modified to eliminate those causes. Only when the distribution of measured outputs is reasonable and expected with a high statistical confidence has the process met the second level of process control, **predictable.**

Since transfer layer data are regularly acquired on all production wafers, they can be examined in aggregated form. Control charts and histograms are two useful representations of such aggregate data. Standard statistical tests are useful in suggesting whether these data are well-behaved. Fig. 5 shows a histogram of transfer layer lengths collected over a certain time period which can be tested for normality. If normality is shown to be statistically likely, other tools can be used such as control charts. When transfer layer length data are plotted on a control chart, as in Fig. 6, further tests of reasonableness can be made. For instance, the two runs of seven points on one side of the mean in the control chart (wafer #'s 7–17 and 34–40 in Fig. 6) are improbable events that should be more closely investigated. Using MPAR at MWTD highlighted that there are few tools to guide the engineer or operator in these investigations other than reviewing the details of the processing of specific wafers that diverge from expectations in the hopes of uncovering some bias to the process. Still, only when the distribution of transfer layer lengths is well behaved is the gate formation process considered to be predictable.

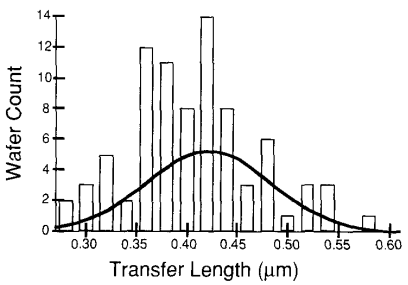

Fig. 5. Histogram of wafer mean transfer layer lengths over a certain time period. The solid line represents a normal distribution with the same mean (0.41 μm) and standard deviation (0.069 μm) as the data.

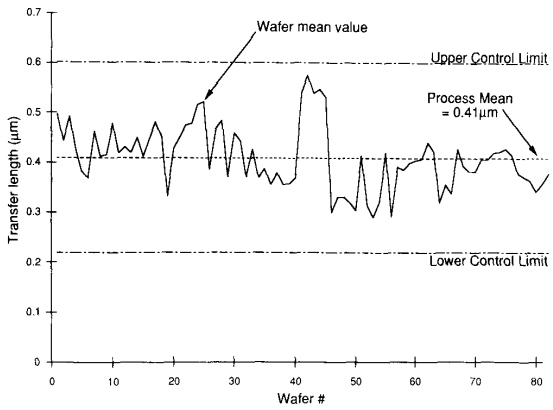

Fig. 6. Control chart of wafer mean transfer layer length with the same data as in Fig. 5.

C. *Acceptable*

When a process is behaving in a predictable manner, one can begin to ask the question of whether the observed distribution of the output meets the expectations of the "customer." Ideally the distribution should be centered about the target output value and the entire range of the distribution contained within the spec limits (Taguchi, in contrast, has argued that all divergences of an output from the target value are, by some measure, inferior [2]). Typically, however, some portion of the distribution lies beyond the spec limits. The question of how much of the distribution should be allowed to exist beyond the spec limits, requires a consideration of the economics involved. The cost of reworking or scraping out of spec parts must be traded off against the expense of improving the process to narrow the distribution of outputs. Because this economic analysis is not always easy to do, judgement and negotiation with the customer on the necessity of the spec limits may play a nonscientific, but unavoidable and important role in determining acceptability. Only when the distribution is centered and a "sufficient" portion of the output distribution lies within the spec limits has the process achieved the third level of process control.

Determining acceptability requires knowledge of the expectations for gate length. Prior work at MWTD demonstrated that the customers desire had demonstrated for gain slope requires a transfer layer length of 0.35–0.48 μm with a target of 0.42 μm. The data of Fig. 5 shows that the current gate formation is centered at 0.41 μm and has a standard deviation of 0.069 μm. This process then can achieve the required specification with a yield of only 65%. The acceptability of this yield must take into account two factors:

- the marginal cost of increasing yield,
- the marginal benefit of this increase.

In practice, neither of these values are straightforward to assess. The marginal cost of increasing yield requires understanding:

- the causes of yield loss,
- how such causes can be reduced or eliminated, and
- the expense involved in undertaking such process improvement projects.

Our research, to date, has spent considerable effort to obtain the first piece of information, the causes of yield loss, for just one critical parameter on HP's MMIC-A process [4]. It was found that variability in transfer layer length can be traced to the six process inputs listed as "causes of process variability" with their "resulting

TABLE I
SIX PROCESS INPUTS RESPONSIBLE FOR CURRENT TRANSFER LENGTH VARIABILITY (COLUMN 1), THE CURRENT VARIABILITY (COLUMN 2), PROPOSED SOLUTION (COLUMN 3), PREDICTED IMPROVED VARIABILITY (COLUMN 4), AND THE COST OF THE SOLUTION (COLUMN 5)

Cause of Process Variability	Resulting Variability-Today (Å)	Solution to Reduce Variability	Resulting Variability-Predicted (Å)	Cost of Solution ($)
Develop Control method	230	Revise control method	170	40,00
Developer exhaustion	213	Single wafer develop station	~0	170,000
Particles on wafer	112	Auto-spin system, better mask clean	56	180,000
Developer bath temperature	209	Buy new bath controller	42	40,000
Mask CD accuracy	214	Screen masks at vendor	44	35,000
Mask CD repeatability	123	Screen masks at vendor	51	15,000

variability'' in Table I, columns 1 and 2. Obtaining this single piece of information required three man-months effort in designing and running experiments to trace the effects of variability in various process inputs on the gain slope parameter under study. Yet once these causes were know, it was found that coming up with ways to reduce or eliminate these sources of yield loss was a straightforward task for experienced engineers (see Table I, column 3). Estimating the effects of these improvements on variability proceeds directly from the experimental work used to understand the causes of process variability (see Table I, column 4). For example, if a new bath temperature controller reduces the variability of bath temperature from one standard deviation of 0.5 to 0.1°C then the induced variability can be calculated to fall by a known amount, from 209 to 42 Å. Finally, estimating the expense involved in undertaking these process improvement projects is similar in challenge to estimating the costs of research and development with which this organization, like many others, has considerable experience (see Table I, column 5).

The marginal benefit of increased yield is considerably more opaque. Nominally, the marginal benefit is simply the reduction of rework and scrap costs. However, in a capacity-constrained fab that expects continued growth in demand and must shorten cycle times even as they are growing longer, this nominal estimate definitively understates the benefit of increased yield. While estimates have been made for this application, considerable improvements are still needed in the accounting and information reporting structures and in the proper application of economic and financial models to this situation. It is clear, however, that the marginal benefit of a process improvement project is an inverse function of the change in variability from undertaking that project. Ultimately, though, an accurate relationship between reduced variability and increased profitability must be identified.

Once known, the marginal cost can be compared against the marginal benefit to suggest which, if any, process improvement projects merit the investment of resources. One can construct a table, such as Table I, that summarizes the central data. It is important to remember that other alternatives to these projects are equally valid, prime among these are to replace the current process with a new one (e.g., use an electron-beam lithography process), or take no action at all. The predicted variability can be calculated by combining variabilities from the results in Table I, column 4 and is found to be 0.054 μm. This translates into an expected yield of 83%.

If resources are invested in some or all of these process improvement projects, a reduction in process variability can be expected (see Fig. 7). This change to the process should move the process closer to **acceptable.** However, explicitly trading off the value of reduced variability against the resource investment required is still difficult and inexact. In the end, defining what level of yield is acceptable and committing resources to meet this level was found to pose the greatest challenges in bringing a process under control.

D. Recoverable

Having reached the ''acceptable'' stage, a process is fully under control . . . for now. To provide a sense of security that this condition will remain or can be recovered if lost, the process should be fully documented to allow rebuilding the facilities, tooling, software, and operator techniques currently in use. Since many manufacturing processes, particularly in semiconductor fabrication, are still dependent on operator expertise, it is imperative that documentation be complete and that an active training program exists to pass on that part of expertise not captured in documentation. Only when this final requirement is met has the process reached the final level of process control, **recoverable.**

In exploring what was needed to make the gate length fabrication process recoverable, it was found that processing technique varied over time. Consequently, ''unit

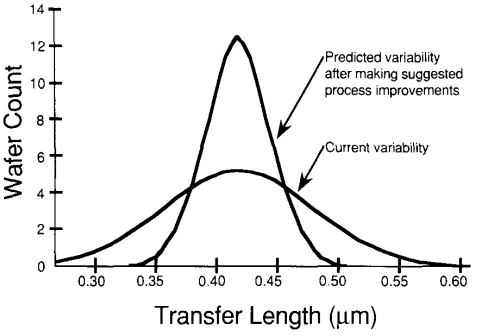

Fig. 7. Current and predicted (after suggested process improvements) normal distributions of transfer layer length.

processing specifications'' that define processing techniques and expected output values are being written for each subprocess involved with gate formation. Recoverability also requires writing specifications for auxiliary processes such as daily aligner calibration or aligner bulb replacement. Not surprisingly, these documents sometimes fail to capture all the details of the correct procedures and operators do not always read updated specifications. Consequently, training is used as an ongoing means of keeping processing techniques uniform across operators and over time. When the process is found to be acceptable and the training and documentation are current, the gate formation process will finally be considered to have reached the final level of control, **recoverable.**

Reaching the final level of recoverable does not imply that all dice produced will meet customer expectations, but that the process yields an acceptable number of products with an output measurement within the spec limits and can be expected to continue to do so with a low level of risk. This level of control does not excuse anyone from continuously improving the process over time as such improvement may be necessary to maintain competitive manufacturing capability in the future.

VI. Organizational Benefits of MPAR

The MPAR methodology was initially viewed as a means of creating a unified concept among engineers and managers of how to define, pursue and measure process control in a facility with a wide variety of processes. As this methodology gains increasing acceptance and use within MWTD, the resources committed to process improvements and the potential benefits of applying MPAR have increased considerably. While the implications of using the MPAR methodology cannot be fully separated from the effects of other changes underway at MWTD, the costs and benefits discussed here appear to be significantly dependent on the increasing use of MPAR.

The MPAR methodology has been developed and gradually utilized at MWTD over the past two years. As this methodology has become standard practice, it has sparked several changes in the way the manufacturing and, more recently, the design functions are managed. More than anything else, MPAR has helped to make the pursuit of process control a way of life at MWTD. Process control is becoming a never fully reached goal, quite in tune with the Hewlett-Packard's corporate philosophy of total quality control.

The successful use of MPAR is far from complete at MWTD. As was observed in the application of this methodology to the narrow problem of control of gain slope by control of the gate formation process, rigorous application of MPAR is a costly and major endeavor. The shear number of processes requiring control and the reliance on operator technique in GaAs IC fabrication necessitate that much of the burden of utilizing MPAR be shared by operators. This, however, has required MWTD to re-think what level of operator knowledge is needed in the fab. Consequently, MWTD upgraded all fab operator positions to a higher skill level and they have undertaken an exhaustive operator training program that includes both the MPAR methodology and the various tools, such as statistical process control, necessary to support MPAR. Along with this skills upgrade, MWTD is empowering line operators with the responsibility to evaluate and, in many cases, fix out of control processes. Furthermore, engineers are being further educated in the use of efficient design of experiments. All of this represents a large investment on the part of MWTD.

As was observed in the case of control of gate formation, it is difficult to definitely evaluate the benefits to be expected from such an investment. Current management must have the foresight to realize that high levels of process control can be a primary determinant of competitive advantage now and in the future as has been true in other industries.

While MPAR is being gradually implemented throughout the facility, few processes have yet to reach the recoverable stage; nonetheless, the implementation of MPAR is changing the way manufacturing and design engineering are practiced. Statistical process control is becoming de facto a part of these jobs. Manufacturing and design managers both have performance goals that now include the level of control reached by their processes. MPAR has become a tool for change at this division.

VII. Conclusion

A methodology for guiding the pursuit of process control at Hewlett-Packard's Microwave Technology Division has been presented. The MPAR methodology begins with defining a specific process and the customer's expectations of this process, then increases control over the process through four levels: measurable, predictable, acceptable, and recoverable. The use of this methodology to control the gate fabrication process for a GaAs traveling-wave amplifier was discussed.

Experience at MWTD suggests that the realization of process control is as much a managerial problem, as it is a technical one. This application suggests that MPAR

serves as a useful conceptual guideline for operators, engineers, and managers in uniformly applying a wide variety of process control tools previously in only sporadic use at MWTD. While a correct and complete use of MPAR encompasses a broad span of organizational undertakings and requires commitment of considerable resources, it appears to fill a critical gap in current efforts to realize process control.

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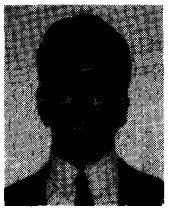

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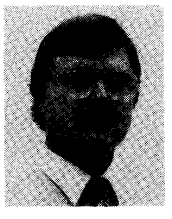
From 1985 to 1988, he worked as an engineer and technical supervisor at KLA Instruments in Santa Clara, CA. There he worked on the testing, reliability, and field support of automated optical inspection equipment used in the manufacture of semiconductors. During 1989, he worked at Hewlett-Packard's Microwave Technology Division, Santa Rosa, CA, doing research on the manufacture of GaAs IC's. Since August 1990, he has been an Associate with McKinsey & Company in San Francisco, CA. His current research focuses in the areas of overall manufacturing strategy, efficient resource allocation and process control, all in the manufacture of high technology products.



Scott S. Elliott (SM'80) received the B.S. and M.S. degrees in electrical engineering from the University of California at Berkeley in 1969 and 1971, respectively, and the Ph.D. degree in electrical engineers from the University of California at Santa Barbara in 1978.

In the mid-1970s, he developed novel Yttrium-Iron-Garnet (YIG) components, including limiters and filters. Since 1978, he has worked at the Hewlett-Packard Microwave Technology Center in Santa Rosa, CA. He has lead projects to develop Surface Acoustic Wave resonators and filters (including introducing the first SAW resonator to be sold commercially in an instrument) millimeter-wave diode integrated circuits on Gallium Arsenide and high-speed light-wave detectors and modulators. He is now the Fab Operations Manager for the HP Gallium Arsenide IC facility in Santa Rosa, where he is leading work on Process Control methodologies.

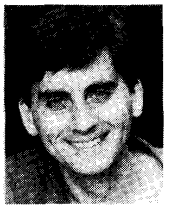
Dr. Elliott has authored or coauthored over 30 technical papers in the areas of microwave, acoustic, and optical devices and holds a patent on Surface Transverse Wave resonators.

Neil Wylie received the B.Eng. degree in 1980 in electronic engineering from the University of Sheffield, England.

He has been involved in semiconductor manufacturing for the past 11 years. He was employed at National Semiconductor in Scotland as a process engineer on the bipolar linear IC line until 1983. From 1983 to 1987 he worked for Fairchild Semiconductor, San Rafael CA, where he developed a manufacturing process for high voltage power mosfet devices. Since 1987 he has been involved with the manufacturing of GaAs IC's at the Microwave Technology Division of Hewlett Packard in Santa Rosa, CA, where he is currently the Process Engineering Manager in the wafer fab. He has authored several technical papers and holds a patent for a novel power mosfet device structure.

Rebecca M. Henderson holds a mechanical engineering degree from MIT and a doctorate in business economics from Harvard University, Cambridge, MA.

She became an Assistant Professor in the strategic management group at the MIT Sloan School of Management in 1988, where she teaches courses in corporate strategy, in the management of process and product development and in the economics of technological change. Her research focuses upon the problems established firms encounter in the face of radical technological change, particularly in the semiconductor capital equipment and pharmaceutical industries.



Jesús A. del Alamo (S'79-M'85) received the degree of Telecommunications Engineer from the Polytechnic University of Madrid in 1980, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1983 and 1985, respectively. From 1977 to 1981 he was Research Assistant at the Institute of Solar Energy of the Polytechnic University of Madrid, working on silicon solar cells. At Stanford University he carried out his Ph.D. dissertation on minority carrier transport in heavily doped silicon and its relevance to bipolar transistors and solar cells.

From 1985 to 1988 he was research engineer with NTT LSI Laboratories in Atsugi (Japan) where he conducted research on heterostructure field-effect transistors (HFET's) based on InP, InAlAs, and InGaAs. Since 1988 he has been with the Department of Electrical Engineering and Computer Science of Massachusetts Institute of Technology as Assistant Professor, and from 1991, as Associate Professor. His current interests include high performance HFET's based on compound semiconductors that contain In and novel quantum-effect devices with one-dimensional carrier confinement.

Dr. del Alamo is the current holder of the ITT Career Development Professorship at MIT. In 1991 he was awarded the Presidential Young Investigator Award by NSF. He is a member of the American Physical Society, and the Japanese Society of Applied Physics.