Strained-Insulator $In_xAl_{1-x}As/n^+-In_{0.53}Ga_{0.47}As$ Heterostructure Field-Effect Transistors

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***Abstract*—In an effort to enhance the conduction band discontinuity between channel and insulator, $In_xAl_{1-x}As/n^+-In_{0.53}Ga_{0.47}$ As HFET's have been fabricated with InAs mole fractions in the $In_xAl_{1-x}As$ gate insulator of $x = 0.52$ (lattice matching), 0.48, 0.40, and 0.30. We have experimentally found that decreasing the InAs mole fraction in the insulator results in reduced forward- and reverse-bias gate currents, increased reverse gate breakdown voltage, and reduced real-space transfer of hot electrons from channel to gate. We have found that down to $x = 0.40$, these improvements trade off with a slightly reduced transconductance, but the gain in gate bias swing results in an increase in maximum current drivability. From $x = 0.40$ to $x = 0.30$, there is a drastic decrease in transconductance, coincident with a high density of MISFIT dislocations. Wide-bandgap $In_xAl_{1-x}As$ insulator HFET's with $x \approx 0.40$ show promise for power microwave applications.**

I. Introduction

In long-wavelength optical and ultra-high-frequency microwave telecommunication applications $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ Heterostructure Field-Effect Transistors (HFET's) on InP are of great interest. The advantages of this material system are many. $In_{0.53}Ga_{0.47}As$ has a higher peak electron velocity, and a higher room-temperature mobility than GaAs [1]. In addition, it has a larger Γ-L separation and a lower effective mass [1]. $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ provides better electron confinement than AlGaAs/GaAs because of its large (0.5 eV [2], as compared to 0.3 eV [3] for AlGaAs/GaAs) conduction-band discontinuity.

Modulation-doped field-effect transistors (MODFET's) from this material system have shown excellent performance [4]. However, MODFET's suffer from the effects of DX centers [5]–[7], transconductance collapse at high gate–source bias [8], [9], and a reduced gate breakdown voltage due to the presence of doping impurities in the insulator. Metal–insulator doped-semiconductor FET's (MIDFET's), however, do not have any dopants in the gate insulator and therefore do not have the above drawbacks [10]. This leaves much greater freedom in the gate insulator design [11]. In addition, their excellent high-frequency performance, comparable with MODFET's of the same gate dimensions, has been recently shown [11]–[14].

In any HFET, it is desirable to get the highest possible conduction-band discontinuity ΔE_c. Doing so reduces the gate leakage current, allowing a larger maximum forward gate voltage. In the $In_xAl_{1-x}As/In_{0.53}Ga_{0.47}As$ system, this can be done by increasing the AlAs mole fraction, i.e., by decreasing the InAs mole fraction x in the $In_xAl_{1-x}As$ insulator layer. In a MIDFET this should result in improved drain current drivability. In a MODFET, this is not necessarily the case because the insulator is heavily doped and the maximum forward gate bias is limited by the formation of parasitic MESFET [8], [9]. In addition, changing the InAlAs composition from that at lattice-matching in the direction of increased AlAs introduces additional DX-like centers [15], which could have a negative impact on MODFET performance. The MIDFET is therefore very well suited for a strained $In_xAl_{1-x}As$ insulator.

Decreasing the InAs composition of InAlAs rapidly brings about an increase in the conduction-band discontinuity (ΔE_c) between the $In_xAl_{1-x}As$ insulator and the $In_{0.53}Ga_{0.47}As$ channel (Fig. 1). In fact, one gains rapidly till an InAs fraction of about 0.32, at which point the conduction-band minimum changes from the Γ to the X valley [16] and the rate of increase of ΔE_c becomes minimal. However, changing the InAs fraction of $In_{0.52}Al_{0.48}As$ also changes its lattice constant from that of InP, introducing strain. Therefore, for a given gate-insulator thickness, a critical value of InAs mole fraction is expected to exist beyond which dislocations are formed at the channel/insulator interface, possibly resulting in severely degraded device performance. The study of this fundamental trade-off from a device perspective is the purpose of this paper.

To explore the minimum tolerable $(InAs)_x$ composition in the insulator, we have fabricated $In_xAl_{1-x}As/n^+-In_{0.53}Ga_{0.47}As$ MIDFET's with $x = 0.52$, 0.48, 0.40, and 0.30. Extrapolating from the coefficients of InAs and AlAs using the method of Van de Walle [17] to include the effects of strain, ΔE_c is expected to increase from 0.49 eV

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Lg=1.0 μm

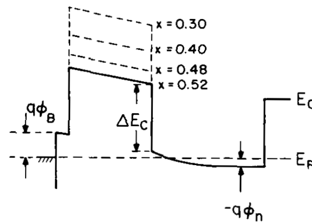

Fig. 1. Schematic energy band diagram of intrinsic FET structure as a function of InAs mole fraction x in the $In_xAl_{1-x}As$ barrier layer, showing the rapid increase in ΔE_c with decreasing x.

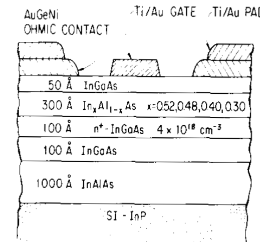

Fig. 2. Schematic cross section of the fabricated $In_xAl_{1-x}As/n^+$-$In_{0.53}Ga_{0.47}As$ MIDFET's.

at $x = 0.52$ to 0.56 eV at $x = 0.48$, 0.67 eV at $x = 0.40$, and 0.81 eV at $x = 0.30$. The Schottky-barrier height will be approximately 0.2 eV greater than these numbers, since the surface Fermi level of the $In_{0.53}Ga_{0.47}As$ cap is pinned 0.2 eV below its conduction band [18]. The following benefits have been experimentally confirmed in these MIDFET's: reduced gate leakage, improved gate breakdown voltage, and reduced real-space transfer of hot electrons from the channel to the gate. In addition, our results also show that decreasing the InAs fraction from 0.40 to 0.30 results in a sharp decrease in device transconductance. This has been found to be due to a large density of misfit dislocations, which restrict current flow [19].

II. Experimental

A cross section of the device structure is shown in Fig. 2. Four wafers were grown by MBE in MIT's Riber 2300 system. They were grown with InAs mole fractions in the $In_xAl_{1-x}As$ gate barrier layer of 0.52 (lattice matching), 0.48, 0.40, and 0.30. The starting material was semi-insulating Fe-doped InP. Surface preparation of the InP wafer was carried out using a 3 : 1 : 1 $H_2SO_4 : H_2O_2 : H_2O$ etch followed by a 1 : 20 bromine-methanol etch. The device structure consists (from bottom to top) of a 1000-Å undoped $In_{0.52}Al_{0.48}As$ buffer layer, a 100-Å undoped $In_{0.53}Ga_{0.47}As$ subchannel, a 100-Å heavily Si doped ($N_D = 4 \times 10^{18}$ cm^{-3}) $In_{0.53}Ga_{0.47}As$ channel, a 300-Å undoped $In_xAl_{1-x}As$ gate insulator layer, and an undoped 50-Å $In_{0.53}Ga_{0.47}As$ cap. The subchannel separates the channel from the reverse InGaAs/InAlAs interface, improving transport characteristics [20]. In the AlGaAs/GaAs system, impurity segregation towards the interface, as well as interface roughness, has been known to cause a poor reverse interface [21].

Device fabrication is similar to that used in [22]. In summary, isolation was performed by chemically etching a mesa down to the InP substrate using a $H_2SO_4 : H_2O_2 : H_2O$ 1 : 10 : 220 etch. For the ohmic contacts, 1500 Å of AuGe followed by 300 Å of Ni were evaporated, lifted off, and alloyed at 350°C for 1 min. For the gate, 300 Å of Ti, then 2000 Å of Au were e-beam evaporated and lifted off. This Ti/Au procedure was repeated to form the contact pads.

I–V characteristics were measured for devices with a nominal gate length of 1.5 μm and width of 30 μm. The actual gate lengths (measured by SEM) ranged from 1.4 to 2.1 μm, with an average of 1.8 μm. At these small gate lengths, the devices are velocity saturated at their operating points. The differences in the peak transconductances and drain currents should therefore be more representative of changes in the material, rather than due to changes in gate length. To show these trends, we have randomly selected ten devices from our one-eighths pieces of 2-in wafers, and have plotted our data with error bars representing two standard deviations. In all devices considered here, electron transport takes place along the $[0\bar{1}1]$ direction. The nominal gate–source spacing is 2 μm. Transmission-Line Model (TLM) measurements were used to obtain the contact resistance. The extrinsic channel sheet resistance and the source resistance were obtained by the all-electric Floating-Gate Transmission-Line Model (FGTLM) method [23], [24].

The gate *I–V* characteristics were measured with the drain and source contacts shorted to ground, and the gate terminal biased. For lack of a better definition, we defined the reverse breakdown voltage at a gate current of 0.3 mA, which corresponds to about 3.5% of the peak drain current of the reference device. All measurements were done using an HP4145A semiconductor parameter analyzer.

III. Results

Fig. 3 is a plot of the transconductance versus gate–source voltage of representative devices from each of the four wafers. These data were obtained for $V_{ds} = 4$ V. For the $x = 0.52$, 0.40, and 0.30 devices, two major trends are noticeable as x is decreased. First, the peak g_m decreases as x is decreased. This decrease is more pronounced between $x = 0.40$ and $x = 0.30$ than between $x = 0.52$ and $x = 0.40$. Values calculated by averaging over ten devices show a decrease in peak g_m from 218 mS/mm at $x = 0.52$ to 189 mS/mm at $x = 0.4$ to 127 mS/mm at $x = 0.30$. This is a drop of 13% for $x = 0.40$ and a drastic 42% for $x = 0.30$ from the reference device. As discussed later, this has been found to be due to the presence of a large density of misfit dislocations in the $x = 0.3$ sample [19]. Secondly, the g_m versus V_{gs} curve becomes flatter and remains positive for larger V_{gs} as x is

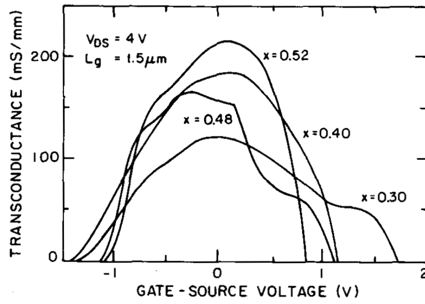

Fig. 3. A plot of transconductance versus gate-source voltage, showing transconductance degradation with decreasing InAs mole fraction in the $In_xAl_{1-x}As$ barrier layer.

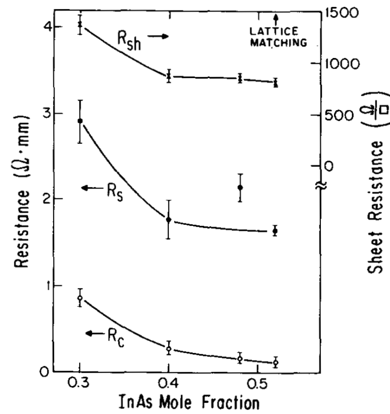

Fig. 4. A plot of statistically averaged contact resistance R_c, sheet resistance R_{sh}, and source resistance R_s as a function of InAs mole fraction in the $In_xAl_{1-x}As$ barrier layer. All three resistances decrease with increasing x.

decreased. This results in a more linear device which is able to handle a larger input voltage swing. The $x = 0.48$ device is anomalous in that its peak g_m is lower than that of the $x = 0.40$ device. The $x = 0.48$ devices were slightly misaligned, resulting in a larger source resistance, which could be responsible for this effect.

Fig. 4 shows the variation of the contact resistance R_c, the sheet resistance R_{sh}, and the source resistance R_s with x. The values of R_c are averages over five TLM structures, and the values of R_s and R_{sh} over five FGTLM structures. R_c monotonously increases with decreasing x. Auger electron spectroscopy on ohmic contacts to AlGaAs/GaAs MODFET's has shown that in a good ohmic contact, the Al migrates out of the barrier layer into the contact metal [25]. A larger Al fraction in the barrier, which results in a larger R_c, is consistent with a model involving the destruction of the barrier by Al outdiffusion in the process of forming the ohmic contact. R_{sh} is fairly constant from its value at lattice matching down to $x = 0.40$, but then increases for $x = 0.30$. A large density of misfit dislocations, partially depleting the channel, would increase R_{sh}. The value of R_s, directly measured from the FGTLM, is consistent with the value calculated from R_c and R_{sh}, i.e., $R_s = R_c + L_{gs} \times R_{sh}$, where L_{gs} represents the separation from source to gate. The $x = 0.48$ device, due to its larger gate-source gap (as indicated by SEM measurements), has a higher R_s than would be predicted by interpolation. This could explain its anomalous g_m result.

Fig. 5 shows the variation of g_m, g_{m0} and $I_{d(\max)}$ with x. These values are averages over ten devices, with the error bar representing two standard deviations. The intrinsic transconductance g_{m0} was calculated using the measured R_s values above. Both g_m and g_{m0} decrease with decreasing x while $I_{d(\max)}$ increases up to $x = 0.4$ from its value at $x = 0.52$ in spite of the decreased g_m. This is due to the gain in operating range into higher V_{gs} that the increase in ΔE_c has permitted.

Fig. 6 shows the variation of gate current with gate voltage for devices with $L_g = 1.5$ μm, and $W_g = 30$ μm at $V_{ds} = 0$ V. The forward gate current decreases for devices with lower x. This is expected because of the in-

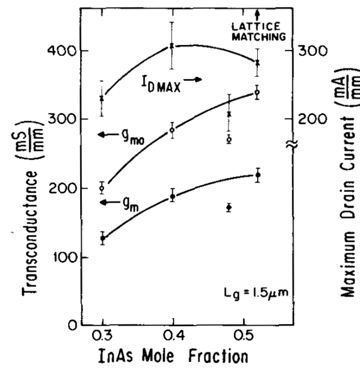

Fig. 5. A plot of statistically averaged peak intrinsic and extrinsic transconductances (g_m and g_{m0}), and maximum drain current $I_{d(\max)}$, as a function of x, over ten devices.

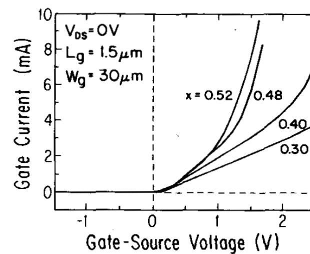

Fig. 6. A plot of gate current versus gate-source voltage as a function of x for the MIDFET, with $V_{ds} = 0$ V, $L_g = 1.5$ μm, and $W_g = 30$ μm.

crease in conduction band discontinuity between the $In_{0.53}Ga_{0.47}As$ channel and the $In_xAl_{1-x}As$ gate. As seen by the broader g_m versus V_{gs} curves (Fig. 3), this decrease has resulted in an increased operating range. This benefit, however, is not realized for low forward V_{gs}, as seen in Fig. 6, and is attributed to *gate-edge leakage*. The edge leakage path is the poor Schottky barrier formed between

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Lg=1.0 μm

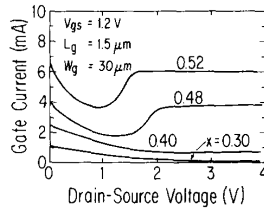

Fig. 7. A plot of gate current versus drain–source voltage as a function of x, showing the effects of RST. RST is eliminated for $x \leq 0.40$.

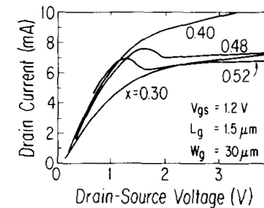

Fig. 8. Transistor drain current versus drain–source voltage characteristics as a function of x, displaying the deleterious effects of RST.

the mesa edge and the gate metal overlap where the gate metal comes in direct contact with the heavily doped channel. Edge leakage has been shown to significantly influence the forward characteristics of devices of this type [26]. On the scale of Fig. 6, the reverse current is negligible.

Fig. 7 shows the variation of the gate current with drain-source voltage for each of the four InAs compositions at $V_{gs} = 1.2$ V. The gate current initially decreases with increasing V_{ds} due to the reduction of the forward gate-channel bias on the drain half of the channel. For the InAs fractions of 0.52 and 0.48, an increase in I_g is observed at a certain threshold of V_{ds}, followed by subsequent saturation. Since similar effects have been reported for real-space transfer (RST) transistors [27], [28], we attribute this effect to the real space transfer of electrons from the channel to the gate. Note that the threshold V_{ds} for RST increases with an increase in ΔE_c, and in fact, RST is essentially nonexistent for $x \leq 0.40$. The RST V_{ds} threshold was also seen to increase with lower V_{gs}. These observations are consistent with the fact that a larger electric field in the channel is required to initiate RST over a higher barrier. Our results show that RST is reduced with increasing conduction-band discontinuity, and given a large enough ΔE_c, can actually be eliminated.

For our HFET's, real-space transfer of electrons is a deleterious mechanism since it decreases the drain current, as displayed in Fig. 8, which shows the drain current versus the drain–source voltage for each of the InAs fractions at a gate voltage of 1.2 V. On comparing Figs. 7 and 8, it is seen that for the devices with InAs fractions of 0.52 and 0.48, the increase in gate current is coincident with the decrease in drain current. This negative differential resistance region in insulating-gate HFET's has been observed by other authors [28], [29]. I_d is not degraded when RST is minimized. The increased I_d, the reduction in the operating point gate current, and the reduction of unstable negative resistance regions are the merits of reduced RST in these wide-bandgap insulator devices.

A final advantage of the strained-insulator MIDFET's is the enhanced gate–channel breakdown voltage. This reverse-bias gate–channel diode characteristics are shown in Fig. 9. As mentioned above, we have defined breakdown at a gate leakage current of 0.3 mA. Breakdown voltages of 13.7, 16.2, 22.7, and 28.8 V were measured for devices with InAs fractions of 0.52, 0.48, 0.40, and 0.30, respectively. The rapid increase of breakdown voltage with a reduction in InAs mole fraction makes wide-bandgap insulator MIDFET's attractive for power microwave applications.

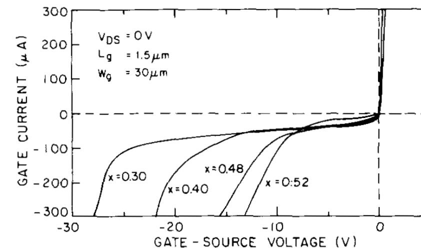

Fig. 9. Reverse-bias gate–channel diode characteristics at $V_{ds} = 0$ V for the MIDFET, with $L_g = 1.5$ μm and $W_g = 30$ μm. The plot shows the rapid increase in breakdown voltage with decreasing InAs mole fraction in the $In_xAl_{1-x}As$ barrier layer.

IV. Discussion

The gain in conduction-band discontinuity at lower InAs fractions is not fully evident in the low-voltage forward I_g–V_{gs} characteristics of the devices (Fig. 6). As mentioned previously, this is attributed to leakage at the gate metal–mesa edge overlap [26]. Heterostructure diodes without this edge leakage path were measured to separate out this effect. These diodes have an area of 10 000 μm^2, about 220 times the area of the device gate. Since the gate is fully contained inside the mesa, there is no gate–mesa edge overlap [26]. Fig. 10 shows their forward characteristics for each x at 300 and 100 K. The flatband voltage for these diodes is calculated to be 0.4 V. For the low $(InAs)_x$ diodes, turn-on does not occur till well beyond flatband (see Fig. 10), i.e., turn-on is directly limited by the conduction-band discontinuity [12]. However, it is possible that a large density of misfit dislocations could result in Fermi-level pinning at the interface, giving the effect of a larger ΔE_c [31] and artificially increasing the turn-on voltage of the $x = 0.30$ diode. For all x, cooling the diodes have resulted in a drastic reduction in forward diode current. This suggests that the dominant forward-gate current mechanism is thermionic emission, since thermionic emission is suppressed both with a reduction in temperature and an increase in ΔE_c. The promising forward current reduction of the low $(InAs)_x$ diodes show that edge isolation technology is necessary for a more effective reduction in forward I_g in these wide bandgap $In_xAl_{1-x}As$ HFET's.

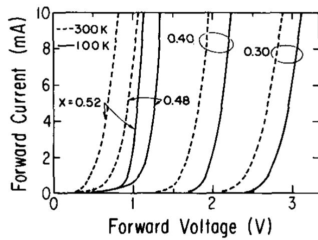

Fig. 10. Forward I–V characteristics of heterostructure diodes as a function of x at 300 and 100 K. Gate leakage is significantly reduced with decreasing InAs fraction in the $In_xAl_{1-x}As$ barrier layer and at lower temperature.

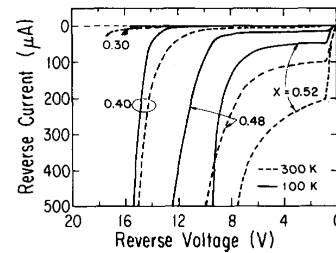

Fig. 11. Reverse I–V characteristics of heterostructure diodes as a function of x at 300 and 100 K.

The reverse diode characteristics are plotted in Fig. 11 for each x at 300 and 100 K. For reverse bias, the Schottky barrier limits the diode current. The presence of three distinct regions is noted in order of increasing reverse-bias: pre-threshold, plateau, and breakdown. The pre-threshold to plateau transition corresponds to the channel being pinched off, thereby saturating the area-related gate leakage component [26]. As x is decreased, this pre-threshold reverse leakage current sharply decreases, corresponding to a larger barrier height of the gate metal/$In_xAl_{1-x}As$ Schottky junction for smaller x. For $x = 0.3$, the enhancement in the Schottky barrier height has virtually eliminated the reverse leakage current. For smaller x, the plateau region becomes wider, and breakdown occurs at higher values of reverse bias. The $x = 0.30$ diodes broke down destructively, and with a lot of noise, at 25 to 50 μA, whereas the other diodes had a soft, nondestructive fairly smooth breakdown. The breakdown voltage of these diodes is lower than that of the FET's because the diodes have four sharp corners on the mesa, while the FET gates consist of parallel edges. While the mechanism for eventual breakdown is not clear, a reduction in temperature has reduced the reverse leakage resulting in a larger breakdown voltage. The reduction in reverse current both with a reduced InAs mole fraction (larger Schottky-barrier height), and a reduction in temperature points to thermionic emission. The destructive and noisy breakdown of the $x = 0.3$ device perhaps corresponds to the onset of another mechanism.

As x is reduced from lattice matching, strain builds up in the $In_xAl_{1-x}As$ layer. The $x = 0.52$ and $x = 0.48$ devices fall within the Matthews–Blakeslee critical layer limit of $x = 0.45$ for 300-Å thickness [30]. The $x = 0.40$ and $x = 0.30$ devices fall outside. We have, using a dark-field optical microscope, seen misfit dislocations in the $x = 0.4$ and $x = 0.3$ processed device samples. A more complete description is presented in [19]; the main conclusions are summarized here. The dislocations are unidirectional and run along $[0\bar{1}1]$. For the $x = 0.4$ and $x = 0.3$ samples, devices with current flow along $[0\bar{1}1]$ had a higher transconductance and lower sheet resistance than devices with current flow along [011], i.e, perpendicular to the dislocation. Devices on the $x = 0.52$ and $x = 0.48$ samples showed no such orientation dependence. From

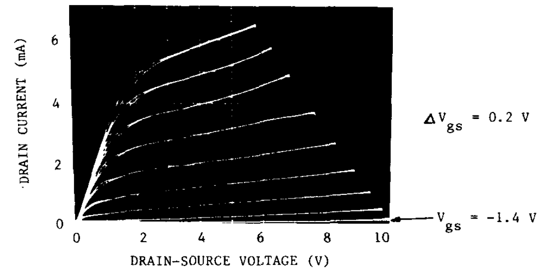

Fig. 12. I–V characteristics of MIDFET with $x = 0.4$ and V_{ds} up to 10 V, showing its suitability for power microwave applications. The device also has good pinchoff.

these data and other data supporting Fermi-level pinning at the misfit dislocation [31], we deduce that misfit dislocations partially deplete the portion of the channel in their proximity. The orientation dependence arises because these (cylindrical) depletion regions provide more of a bottleneck to current flow perpendicular, rather than parallel to them. For a low dislocation density ($x = 0.4$), devices with current flow along the dislocations, $[0\bar{1}1]$, are only slightly degraded, whereas devices with current flow perpendicular to the dislocations, [011], are considerably degraded. For a high dislocation density ($x = 0.3$), however, even devices with current flow along $[0\bar{1}1]$ are significantly degraded. These dislocations, however, do not contribute to increasing forward or reverse leakage currents, and the effects of increased ΔE_c and Schottky barrier heights are clear from Figs. 10 and 11. Our results show that the benefits of decreasing the InAs mole fraction of the $In_xAl_{1-x}As$ insulator continue beyond the critical layer limit, as long as the dislocations are sufficiently sparse and the current is oriented along the dislocation.

The characteristics obtained for reduced $(InAs)_x$ devices make them promising for power microwave applications. Fig. 12 shows the I–V characteristics up to $V_{ds} = 10$ V of the $x = 0.4$ device. In this photograph, the power has been restricted, as devices were not mounted on a heat sink, and burnt out at higher power. Well-behaved characteristics have been obtained.

V. Conclusions

$In_xAl_{1-x}As/n^+$-$In_{0.53}Ga_{0.47}As$ HFET's have been fabricated with a decreased InAs fraction in the $In_xAl_{1-x}As$

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Lg=1.0 μm

insulating layer. Reduced InAs (or enhanced AlAs) mole fractions in the insulator result in increased gate Schottky-barrier height and an increased ΔE_c between the channel and the insulator. This has important benefits for the device, such as reduced gate leakage current, increased reverse breakdown, and reduced real space transfer. The tradeoff in decreasing the InAs mole fraction, however, is a decrease in the peak transconductance from the introduction of misfit dislocations. However, $I_{d(max)}$ actually increases for a certain range of decreasing $(InAs)_x$ due to the greater voltage range applicable to the gate. The $x = 0.40$ and $x = 0.30$ devices are over the Matthews–Blakeslees limit of $x = 0.45$ for the 300-Å-thick layer, and have a unidirectional array of misfit dislocations in the $[0\bar{1}1]$ direction. For current flow in $[01\bar{1}]$, the transconductance of the $x = 0.30$ device was drastically degraded, but the $x = 0.40$ device showed only slightly degraded transconductance. For our device design, our results at $x = 0.4$ show this to be close to the optimal composition of the $In_xAl_{1-x}As$ insulator. Our results show that the benefits of decreasing the InAs mole fraction of the $In_xAl_{1-x}As$ insulator are available slightly beyond the Matthews–Blakeslee critical layer thickness, despite the presence of misfit dislocations, for current flow in the direction of the dislocation. Wide-bandgap $In_xAl_{1-x}As$ devices show promise for power microwave applications.

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References

[1] T. P. Pearsall, Ed., *GaInAsP Alloy Semiconductors*. New York: Wiley, 1982.

[2] R. People, K. W. Wecht, K. Alavi, and A. Y. Cho, "Measurement of the conduction-band discontinuity of molecular beam epitaxial grown $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$, N-n heterojunction by C-V profiling," *Appl. Phys. Lett.*, vol. 43, no. 1, p. 118, 1983.

[3] S. Adachi, "GaAs, AlAs, and $Al_xGa_{1-x}As$: Material parameters for use in research and device applications," *J. Appl. Phys.*, vol. 58, no. 3, p. R1, 1985.

[4] U. K. Mishra, A. S. Brown, S. E. Rosenbaum, C. E. Hooper, M. W. Pierce, M. J. Delaney, S. Vaughn, and K. White, "Microwave performance of AlInAs-GaInAs HEMT's with 0.2- and 0.1-μm Gate Length," *IEEE Electron Device Lett.*, vol. 9, no. 12, p. 647, 1988.

[5] T. J. Drummond, W. T. Masselink, and H. Morkoç, "Modulation-doped GaAs/(Al, Ga)As heterojunction field-effect transistors: MODFET's," *Proc. IEEE*, vol. 74, no. 6, p. 773, 1986.

[6] P. M. Solomon and D. J. Frank, "Device physics and new development of heterostructure FETs," in *Int. Workshop on Future Electron Devices—Superlattice Devices* (Tokyo, Feb. 9-11, 1987), p. 67.

[7] K. Nakashima, S. Nojima, Y. Kawamura, and H. Asahi, "Deep electron trapping centers in Si-doped InAlAs grown by molecular beam epitaxy," *Phys. Status Solidi.* (a), vol. 103, p. 511, 1987.

[8] K. Lee, M. S. Shur, T. J. Drummond, and H. Morkoç, "Parasitic MESFET in (Al, Ga)As/GaAs modulation doped FET's and MODFET characterization," *IEEE Trans. Electron Devices*, vol. ED-31, no. 1, p. 29, 1984.

[9] K. Hirakawa, H. Sakaki, and J. Yoshino, "Concentration of electrons in selectively doped GaAlAs/GaAs heterojunction and its dependence on spacer-layer thickness and gate electric field," *Appl. Phys. Lett.*, vol. 45, no. 3, p. 253, 1984.

[10] H. Hida, A. Okamoto, H. Toyoshima, and K. Ohata, "A high-current drivability i-AlGaAs/n-GaAs doped-channel MIS-like FET (DMT)," *IEEE Electron Device Lett.*, vol. EDL-7, no. 11, p. 625, 1986.

[11] J. A. del Alamo and T. Mizutani, "A recessed-gate $In_{0.52}Al_{0.48}As/n^+$-$In_{0.53}Ga_{0.47}As$ MIS type FET," *IEEE Trans. Electron Devices*, vol. 36, no. 4, p. 646, 1989.

[12] —, "Bias dependence of f_t and f_{max} in an $In_{0.52}Al_{0.48}As/n^+$-$In_{0.53}Ga_{0.47}As$ MISFET," *IEEE Electron Device Lett.*, vol. 9, no. 12, p. 654, 1988.

[13] J. B. Kuang, P. J. Tasker, S. Ratanaphanyarat, W. J. Schaff, L. F. Eastman, G. W. Wang, Y. K. Chen, O. A. Aina, H. Hier, and A. Fathimulla, "Low frequency and microwave characterization of submicron-gate $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ heterojunction metal-semiconductor field-effect transistors grown by molecular-beam epitaxy," *J. Appl. Phys.*, vol. 66, no. 12, p. 6168, 1989.

[14] A. Fathimulla, H. Hier, and J. Abrahams, "Microwave performance of pulse-doped-heterostructure GaInAs MESFETs," *Electron. Lett.*, vol. 24, no. 2, p. 93, 1988.

[15] W-P. Hong, S. Dhar, P. K. Bhattacharya, and A. Chin, "Deep levels and a possible D-X-like center in molecular beam epitaxial $In_xAl_{1-x}As$," *J. Elec. Mat.*, vol. 16, no. 4, p. 271, 1987.

[16] H. Kressel and J. K. Butler, *Semiconductor Lasers and Heterojunction LEDs*. New York: Academic Press, 1977.

[17] C. G. Van de Walle, "Band lineups and deformation potentials in the model-solid theory," *Phys. Rev. B*, vol. 39, p. 1871, 1989.

[18] H. H. Wieder, "Fermi level and surface barrier of $Ga_xIn_{1-x}As$ alloys," *Appl. Phys. Lett.*, vol. 38, no. 3, p. 170, 1981.

[19] S. R. Bahl, W. J. Azzam, and J. A. del Alamo, "Orientation dependence of mismatched $In_xAl_{1-x}As/In_{0.53}Ga_{0.47}As$ HFET's," presented at the 6th Int. Conf. on MBE, Aug. 1990, San Diego, CA; to be published in *J. Crystal Growth*, 1991.

[20] S. R. Bahl and J. A. Del Alamo, "A quantized-channel $In_{0.52}Al_{0.48}As/n^+$-$In_{0.53}Ga_{0.47}As$ HFET with high breakdown voltage," presented at the 1990 MRS Fall Meeting, Symp. B; Also in *Mat. Res. Soc. Extended Abstracts*, abstract EA-21, p. 117, 1990.

[21] T. Sajoto, M. Santos, J. J. Heremans, M. Shayegan, M. Heiblum, M. V. Weckwerth, and U. Meirav, "Use of superlattices to realize inverted GaAs/AlGaAs heterojunctions with low-temperature mobility of 2×10^{16} cm^2/V s," *Appl. Phys. Lett.*, vol. 54, no. 9, p. 840, 1989.

[22] J. A. del Alamo and T. Mizutani, "An $In_{0.52}Al_{0.48}As/n^+$-$In_{0.53}Ga_{0.47}As$ MISFET with a heavily doped channel," *IEEE Electron Device Lett.*, vol. EDL-8, no. 11, p. 534, 1987.

[23] J. A. del Alamo and W. J. Azzam, "A floating-gate transmission-line model technique for measuring source resistance in heterostructure field-effect transistors," *IEEE Trans. Electron Devices*, vol. 36, no. 11, p. 2386, 1989.

[24] W. J. Azzam and J. A. del Alamo, "An all-electrical floating-gate transmission line model technique for measuring source resistance in heterostructure field-effect transistors," *IEEE Trans. Electron. Devices*, vol. 37, no. 9, p. 2105, 1990.

[25] A. Christou and N. Papanicolaou, "Redistribution of aluminum in MODFET ohmic contacts," *Solid-State Electron*, vol. 29, no. 2, p. 189, 1986.

[26] S. R. Bahl and J. A. del Alamo, "An $In_{0.52}Al_{0.48}As/n^+$-$In_xGa_{1-x}As$ heterostructure field-effect transistor with an In-enriched channel," in *Proc. 2nd Int. Conf. on InP and Related Compounds* (Denver, CO, Apr. 1990), p. 100.

[27] I. C. Kizilyalli and K. Hess, "Physics of real-space transfer transistors," *J. Appl. Phys.*, vol. 65, no. 5, p. 2005, 1989.

[28] M. S. Shur, D. K. Arch, R. R. Daniels, and J. K. Abrokwah, "New negative resistance regime of heterostructure insulated gate transistor (HIGFET) operation," *IEEE Electron Device Lett.*, vol. EDL-7, no. 2, p. 78, 1986.

[29] E. Delhaye, T. Aguila, M. Wolny, and P. Boissenot, "Circuit applications of the negative differential resistances in heterojunction GaAs MISFETs," *Japan. J. Appl. Phys.*, vol. 29, no. 2, p. 236, 1990.

[30] J. W. Matthews and A. E. Blakeslee, "Defects in epitaxial multilayers," *J. Crystal Growth*, vol. 27, p. 118, 1974.

[31] J. M. Woodall, G. D. Pettit, T. N. Jackson, and C. Lanza, "Fermi-level pinning by misfit dislocations at GaAs interfaces," *Phys. Rev. Lett.*, vol. 51, no. 19, p. 1783, 1983.

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Lg=1.0 μm