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An InAlAs/InAs MODFET

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Abstract

We report what we believe is the first InAs modulation-doped field-effect transistor (MODFET) using an epitaxial heterostructure based entirely on arsenides. The heterostructure was grown by MBE on InP and contains a 30 Å InAs channel. An L_G=2 μm device displays well behaved characteristics, showing sharp pinch-off (V_{th}=-0.8 V) and small output conductance (5 mS/mm) at 300 K. The maximum tansconductance is 170 mS/mm with a maximum drain current of 312 mA/mm. Strong channel quantization results in an unprecedented breakdown voltage of -9.6 V, a several-fold improvement over previous InAs MODFETs based on antimonides. Low-temperature magnetic field measurements show strong Shubnikov-de Haas oscillations from which the electron channel is confirmed to be the InAs layer.

Introduction

The small electron effective mass of InAs makes this material an attractive candidate for the active channel of heterostructure field-effect transistors (HFETs) since it results in high electron mobility and large electron peak velocity with potential for high performance devices [1]. Additionally, the low effective mass of InAs might bring about stronger electron quantization and longer electron coherence lengths which is promising for quantum-effect electronic devices with high operating temperatures [2]. Recently, the first InAs channel HFETs have been fabricated with barriers based on antimonides [3,4]. It would however be of interest to develop InAs channel HFETs that only contain arsenides because of their well established growth and processing technologies.

In this paper we describe the fabrication and characterization of an InAlAs/InAs MODFET. The device shows excellent characteristics with strong channel quantization resulting in a very large breakdown voltage. We have carried out Shubnikov-de Haas measurements to confirm that the electron channel resides in the InAs layer.

Fabrication

For the growth of our heterostructure, we have taken advantage of recent progress in MBE growth of highly-strained AlAs/InAs heterostructures on InP for resonant tunneling devices [5]. The heterostructure shown in Fig. 1 consists, from top to bottom, of a 50 Å undoped $In_{0.53}Ga_{0.47}As$ cap, a 370 Å n^+-$In_{0.52}Al_{0.48}As$ (Si - doped at 5 × 10^{17} cm^{-3}) supply layer, a 60 Å undoped $In_{0.52}Al_{0.48}As$ spacer, a 30 Å undoped AlAs barrier, a 30 Å undoped InAs channel, a 400 Å undoped $In_{0.53}Ga_{0.47}As$ buffer, and an undoped 4000 Å $In_{0.52}Al_{0.48}As$ buffer on a (100) SI-InP substrate. Except for the InAs and AlAs layers, growth was carried out at an As/In beam-equivalent pressure ratio of 25 and a growth rate of 0.8 μm/hr. The substrate growth temperature for all the layers except the InAs layer was 490°C. In order to maintain two-dimensional growth, the InAs layer was grown at 420°C after a growth interrup-

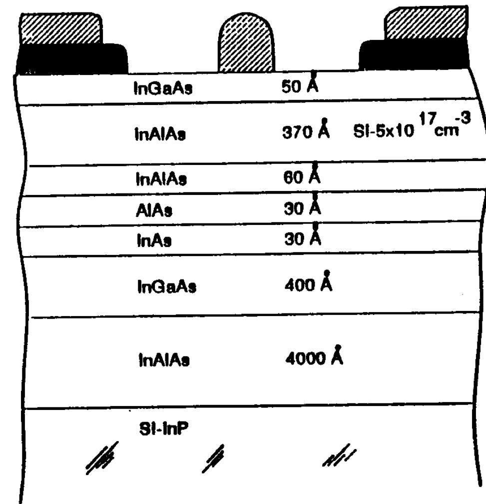

Fig. 1. Cross-section of device structure.

tion during which the substrate temperature was ramped down. Then a monolayer of GaAs was grown on top of the InAs to prevent evaporation and with growth interrupted again, the temperature was ramped up to 490°C. The InAs and AlAs layers were grown at 1 monolayer/sec. The InAs thickness was limited to 30 Å because reflection high energy electron diffraction (RHEED) oscillations were no longer observed for thicker InAs layers. This is consistent with the maximum thickness of InAs of 30 Å that de Miguel et al. were able to grow by MBE and still observe strong photoluminescence in $In_{0.52}Al_{0.48}As/InAs$ quantum wells on InP [6,7].

Device processing proceeded with mesa isolation using a H_2SO_4:H_2O_2:H_2O in a 1:10:220 solution. The etch rate was about 60 Å /sec. Ohmic contacts were formed by annealling a Au/Ge/Ni multilayer in an AG Associates 410 reactor at 350°C for 10 seconds. Finally a 350Å /3500Å bilayer of Ti/Au was lifted-off to form the gate and pads. The measurements reported here are for L_G=2 μm and W_G=20 μm MODFETs with a source-drain separation of 10 μm.

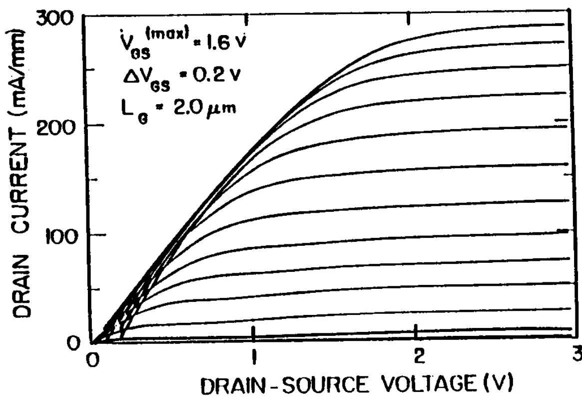

Fig. 2. I_D-V_{DS} characteristics of an L_G=2 μm device at room temperature.

Results

The room temperature output characteristics, shown in Fig. 2 for a typical device, are well behaved displaying a sharp pinch-off (V_{th}=-0.8 V) and small output conductance (5 mS/mm). These characteristics represent a significant improvement over InAs HFETs based on antimonides which have not shown complete pinch-off and also have rather large output conductances at V_{DS} as small as 1 V [3,4]. The transconductance at T=300 K, shown in Fig. 3, displays a double hump feature and has a maximum g_m of 170 mS/mm. We will show that the first hump corresponds to the initial turn-on of the InAs layer and the second corresponds to the additional turn-on of the InGaAs layer underneath the InAs. The intrinsic transconductances, g_{mo}, for the first and second peak are 180 mS/mm and 380 mS/mm respectively. As Fig. 3 shows, there is a broad gate-voltage of roughly 1.5 V at which the transconductance is greater than 100 mS/mm. This allowed a maximum drain current of 312 mA/mm before the onset of parallel conduction through the InAlAs barrier.

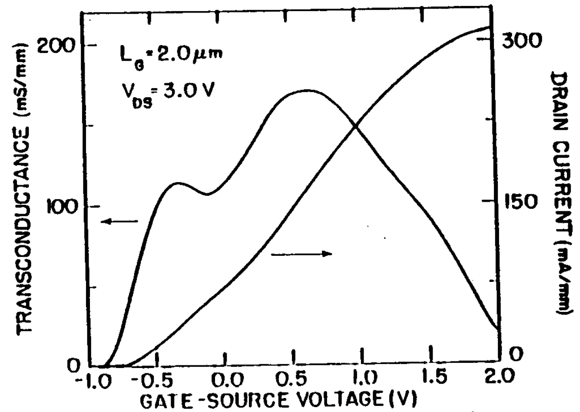

Fig. 3. Transconductance and I_D-V_{GS} characteristics of an L_G=2 μm device at room temperature.

An outstanding feature of this device is its high breakdown voltage. As Fig. 4 shows, the reverse gate leakage current is as small as 78 μA at V_{GS}=-7 V (V_{DS}=0 V). The breakdown voltage of this device occured at V_{GS}=-9.6 V. This is a significant improvement over previous InAs HFETs which at best had a source-drain breakdown voltage of less than 1.5 V. Our results arise from the artificial enlargement of the bandgap produced by strong electron quantization in the 30 Å InAs well, as Bahl and del Alamo have experimentally found in quantum-channel InGaAs HFETs [8].

The contact resistance measured using a four probe transmission line method (TLM) was 0.3 Ω-mm and the sheet resistance was 728 Ω/□ at room temperature. The series resistance, including the contact resistance, for our 4 μm gate-source gap was 3.2 Ω-mm. From Fig. 3, the K-factor for the first hump which we will show in the discussion to be transport only through the InAs layer

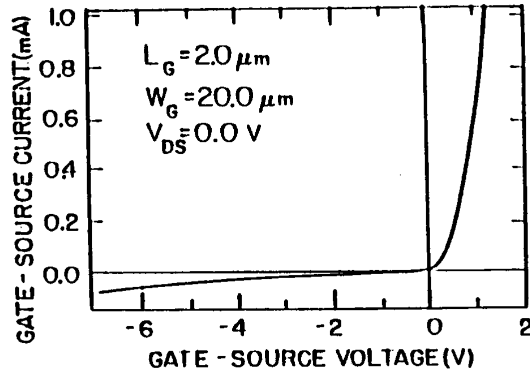

Fig. 4. Gate current characteristics of a 2 μm device at room temperature.

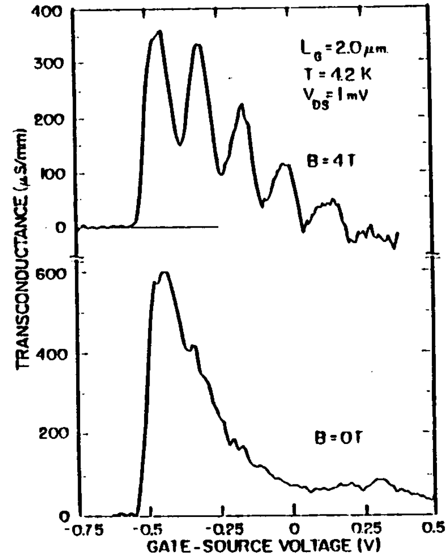

Fig. 5. Transconductance at T=4 K for a 2 μm device in a 4 Tesla magnetic field, showing Shubnikov-de Haas oscillations (above) with a reference transconductance in absence of a magnetic field (below).

equals 328 $\frac{mS}{mm-V}$. Taking into account series resistance, this translates into a mobility of 5400 $\frac{cm^2}{V-sec}$ for the InAs layer. The K-factor for the second hump which results from the additional turn-on of the InGaAs layer is 129 $\frac{mS}{mm-V}$. From this we calculate the mobility to be 9000 $\frac{cm^2}{V-sec}$ for the InAs/InGaAs channel.

Low-temperature magnetic field measurements were conducted in the linear regime of device operation to confirm electron transport through the InAs channel. In a fixed magnetic field, we observed strong oscillations in the transconductance at 4 K as shown in Fig. 5. The oscillations are a result of the Fermi level sweeping through the fixed Landau levels resulting from the magnetic field [9]. From the spacing between two oscillations, ΔV_{GS}, we can calculate the gate-channel capacitance [9]. The capacitance for different V_{GS} and for different magnetic fields is plotted in Fig. 6. The gate-channel capacitance can be used to calculate the depth of the 2DEG from the surface and confirm transport through the InAs. In the discussion we will show that for V_{GS} up to the first hump the channel depth corresponds exactly to the InAs depth.

Discussion

In order to better understand the characteristic double hump in the transconductance shown in Fig. 3, we have used a classical one-dimensional Poisson solver to simulate the energy band diagram of the device for different gate-source voltages [10]. The results of the simulations, plotted in Fig. 7, show that at 300 K the InAs layer turns on at roughly V_{GS}=-0.5 V with the InGaAs layer underneath the InAs beginning to conduct at around V_{GS}=0 V. Finally, parallel conduction through the doped InAlAs barrier occurs at voltages greater than 0.5 V. Additionally, a simple analytical solution of Schrödinger's equation for our InAs/InGaAs well shows the existence of a single bound state in the InAs at 0.21 eV from the bottom of the well with higher lying excited states extending into the InGaAs.

The results of these simulations suggest, therefore, that the double hump feature in the transconductance is due to the initial turn on of the InAs channel followed by the additional turn-on of the InGaAs layer underneath the InAs. The separate turn-on of the InAs layer and the InGaAs layer can be experimentally confirmed through a capacitance measurement. In the quantum regime, we expect the centroid of charge to shift further from the interface when the InGaAs turns on. This is verified from the Shubnikov-de Haas measurements which exactly measures the gate-channel capacitance and channel depth.

In the low-temperature magnetic field measurement, the spacing ΔV_{GS} between the oscillations in g_m can be used to calculate the gate-channel capacitance [9], shown in Fig. 6 for various magnetic fields and gate-source voltages. For V_{GS} between 0 and -0.5 V, where we expect conduction to be primarily in the InAs, the capacitance is roughly 2.1 × 10^{-7} F/cm^2. From this value we estimate the channel depth to be 523 Å. This is almost exactly at the center of the InAs layer which from the MBE growth calibrations is at 525 Å. As the InGaAs channel turns on with V_{GS} greater than about 0 V, the capacitance decreases to 1.75 × 10^{-7} F/cm^2, corresponding to a channel

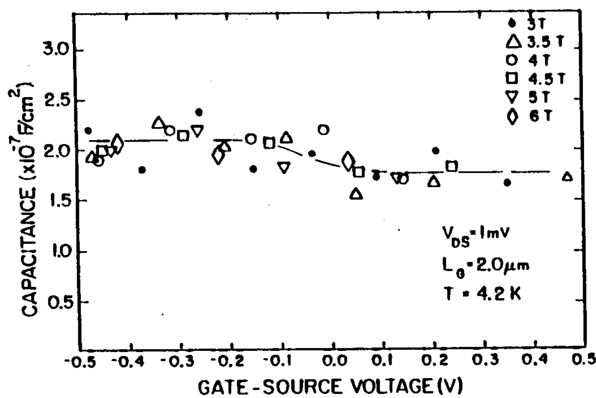

Fig. 6. Capacitance calculated from the ΔV_{GS} spacings of the Shubnikov-de Haas oscillations in magnetic fields from 3 T to 6 T at 4 K.

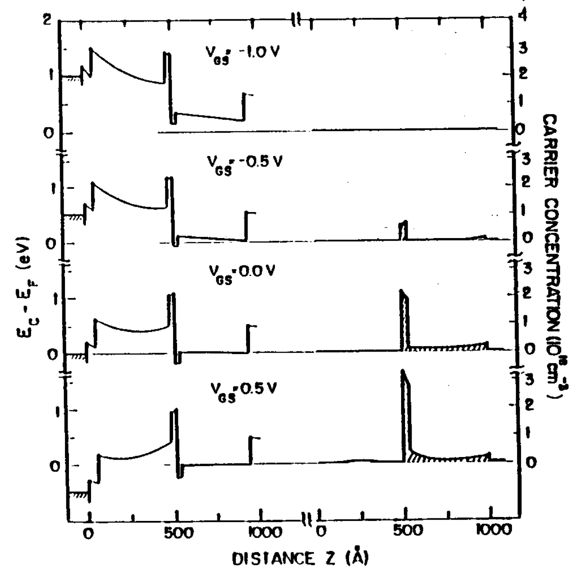

Fig. 7. Simulations of the energy band diagrams and electron charge for different V_{GS}.

depth of 646 Å. This is 136 Å from the InAs/AlAs interface and 79 Å from the center of the InGaAs well (including the InAs layer). This asymmetry in the position of the charge centroid towards the InAs well is reasonable since the InAs well is highly populated. As parallel conduction onsets through the InAlAs, the oscillations in g_m disappear. This is expected since the mobile charge in the doped InAlAs barrier screens the channel from the gate.

The mobility of the InAs layer, about 5400 $\frac{cm^2}{V-sec}$, is relatively low in comparison with what one might expect from such a low effective mass material. Asymmetry in the sample suggests that there might be some dislocations which would limit the mobility. This is substantiated by the fact that the mobility does not increase much as the temperature decreases. A second possibility is the roughening of the InAs/AlAs interface as a result of excessive strain. This was observed by TEM by de Miguel et al. in their 30 Å InAlAs/InAs quantum well structure [6,7]. If this is the case, then in order to increase the mobility in future devices, the InAs layer should be thinner.

Conclusion

We have reported excellent device characteristics with sharp pinch-off and unprecedented breakdown voltages in InAlAs/InAs MODFETs. The results show substantial improvements in device characteristics over InAs MODFETs based on antimonides. This is largely due to the more established growth and processing technologies of arsenides over antimonides and the effective bandgap enhancement through strong electron quantization.

Acknowledgements

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