A Recessed-Gate $In_{0.52}Al_{0.48}As/n^+$-$In_{0.53}Ga_{0.47}As$ MIS-type FET

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***Abstract*—Scaling of the $In_{0.52}Al_{0.48}As$ insulator thickness of $In_{0.52}Al_{0.48}As/n^+$-$In_{0.53}Ga_{0.47}As$ MIS-type FET's is found experimentally to result in a drastic drop in performance below 200 Å. This is demonstrated to arise from an increase in the sheet resistance of the extrinsic portions of the device that accompanies insulator scaling. In order to solve this problem, a recessed-gate MISFET with a very thin (300 Å) n^+-$In_{0.53}Ga_{0.47}As$ cap layer has been fabricated. A 1.5-μm-long gate device showed a transconductance of 285 mS/mm and a current-gain cutoff frequency of 19.4 GHz. This result proves the ability of a thin n^+-$In_{0.53}Ga_{0.47}As$ cap to reduce source resistance and improve device performance. The fabricated recessed-gate structure is a promising candidate for high-performance-scaled MIS-type FET's based on thin, heavily doped $In_{0.53}Ga_{0.47}As$ channels.**

I. INTRODUCTION

FIELD-EFFECT transistors (FET's) based on $In_{0.53}Ga_{0.47}As$ have been the subject of intense research due to their potential for high-speed and high-frequency applications [1]. A number of device structures have been demonstrated that utilize $In_{0.53}Ga_{0.47}As$ as an active channel and $In_{0.52}Al_{0.48}As$ as wide-bandgap gate material: modulation-doped FET's (n-$In_{0.52}Al_{0.48}As$/undoped-$In_{0.53}Ga_{0.47}As$) [2], MIS-type FET's (undoped-$In_{0.52}Al_{0.48}As$/undoped-$In_{0.53}Ga_{0.47}As$) [3], and MIS-type FET's with a doped channel (undoped-$In_{0.52}Al_{0.48}As$/n-$In_{0.53}Ga_{0.47}As$) [4]. Recently, the latter structure has been fabricated with a thin and heavily doped n^+-$In_{0.53}Ga_{0.47}As$ channel, and the resulting performance compared favorably with modulation-doped FET's of the same gate length [5].

Although electrons have a lower mobility in a heavily doped channel than in an undoped channel, there are a number of advantages in a doped-channel MIS-type FET (MIDFET, metal-insulator-doped semiconductor FET, for short) over the more conventional MODFET [5], [6]. In the MIDFET, the $In_{0.52}Al_{0.48}As$ wide-bandgap material is undoped, and therefore its thickness can be scaled down with more freedom than in MODFET's where it is doped, and the maximum attainable doping level sets up a lower limit to the $In_{0.52}Al_{0.48}As$ thickness. This flexibility in scaling should result in higher performance for the MIDFET. Additionally, for large positive gate voltages, parallel conduction can take place in a parasitic channel that appears inside the doped $In_{0.52}Al_{0.48}As$ layer of a MODFET; this results in a sharp transconductance collapse [7], [8]. This phenomenon is experimentally confirmed not to appear in MIDFET's [5] because of the absence of doping in the $In_{0.52}Al_{0.48}As$ layer. This same feature results in higher breakdown voltages in MIDFET's in comparison to MODFET's.

The results obtained so far in 2-μm-long gate MIDFET's with a thin heavily doped $In_{0.53}Ga_{0.47}As$ channel have been very encouraging. An extrinsic transconductance, g_m, of 152 mS/mm, and a current-gain cutoff frequency, f_T, of 12.4 GHz were obtained from a 2-μm gate length FET [5]. Furthermore, g_m and f_T exhibit very high values for a wide range of gate bias [9], which constitutes a significant merit over MODFET's and MESFET's.

In an effort to further improve its performance, in this paper we report the fabrication of $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ MIDFET's with a scaled-down insulator thickness and our previous undoped cap. Our experiments reveal that simple scaling of insulator thickness in a device that has an undoped cap results in intolerably high source resistance that drastically degrades transistor performance. To solve this severe problem we demonstrate a recessed-gate MIDFET with a thin n^+-$In_{0.53}Ga_{0.47}As$ cap.

n^+-$In_{0.53}Ga_{0.47}As$ cap layers have been extensively used for this purpose in n-$In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ MODFET's [10], [11]. Because of the high doping level that exists inside the $In_{0.52}Al_{0.48}As$ layer of a MODFET, tunneling across the n^+-$In_{0.53}Ga_{0.47}As$-cap/n-$In_{0.52}Al_{0.48}As$-insulator/$In_{0.53}Ga_{0.47}As$-channel heterostructure is the likely mechanism that explains the reduction in source resistance that is observed in MODFET's [12]. As we demonstrate in this paper, the mechanism of reduction of source resistance in $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ MIDFET's as a result of the incorporation of an n^+-cap is likely to be very different from MODFET's. We speculate that in a MIDFET the n^+-cap induces an accumulation layer of electrons at the heterointerface between the channel and the insulator in the extrinsic portions of the FET. The large sheet density of electrons, therefore, reduces the sheet resistance of the extrinsic channel and, consequently, the source resistance.

This paper will describe first the experimental fabrication of the scaled MIDFET's with an undoped cap and the

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new recessed-gate MIDFET. It will then present the main results of this effort, demonstrating the superiority of the recessed-gate structure. Finally, it will discuss the origin of the large resistance in undoped-cap MIDFET's and its suppression in the recessed-gate device.

II. Experimental

Schematic cross sections of the devices studied in this work are shown in Fig. 1(a) and (b). The epitaxial structures were grown by MBE on (100) semi-insulating Fe-doped InP substrates at a 520°C substrate temperature. Fig. 1(a) represents the basic MIDFET structure with a very thin undoped cap, which is similar to the device demonstrated before [5]. The n^+-$In_{0.53}Ga_{0.47}As$ channel in all the present devices is nominally 120 Å thick and Si-doped to a concentration of 1.5×10^{18} cm^{-3}. Three different device structures with $In_{0.52}Al_{0.48}As$ insulator thicknesses of 50, 150, and 300 Å were grown.

The new recessed-gate MIDFET is shown in Fig. 1(b). The epitaxial structure is similar to the conventional MIDFET except for the incorporation of an n^+-$In_{0.53}Ga_{0.47}As$ cap, 300 Å thick and 3×10^{18} cm^{-3} Si doped. An $In_{0.52}Al_{0.48}As$ insulator thickness of 300 Å was selected.

Device processing for the undoped-cap MIDFET's is similar to the one described in [5]. In summary, isolation was performed by chemically etching a mesa down to the InP substrate. AuGeNi ohmic contacts were e-beam evaporated, lifted off, and alloyed at 400°C for 30 s. A Ti/Au gate and contact pads were also e-beam evaporated and lifted off. Processing for the recessed-gate MIDFET was identical except for a recess etch performed immediately before Ti/Au gate metal evaporation. The etchant, $H_3PO_4 : H_2O_2 : H_2O$ (1 : 1 : 38), is widely referenced in the literature of this semiconductor system [3].

DC and microwave device characterization was carried out at room temperature. In particular, the S parameters were measured from 0.1 to 26.5 GHz, and from them the current gain as a function of frequency was obtained. This allowed the extraction of f_T, the current-gain cutoff frequency.

The source resistance and its two main components, the contact resistance and the extrinsic channel sheet resistance, were measured in the case of the undoped-cap MIDFET's using the Transmission Line Method (TLM) [13] on structures located next to the devices. For the recessed-gate MIDFET, the TLM technique cannot be used because it measures the sheet resistance of the n^+-$In_{0.53}Ga_{0.47}As$ channel in parallel with the n^+-$In_{0.53}Ga_{0.47}As$ cap layer. As a result, the measurements grossly underestimate the correct contact and sheet resistances [12].

III. Results

Fig. 2 shows the peak extrinsic and intrinsic transconductances of undoped-cap MIDFET's and the peak extrinsic transconductance of a recessed-gate MIDFET with 1.5×200 μm^2 gate dimensions as functions of the gate-insulator thickness. As displayed, the gate insulator plotted in the abcissa includes the 50-Å-thick undoped $In_{0.53}Ga_{0.47}As$ cap shown in Fig. 1(a).

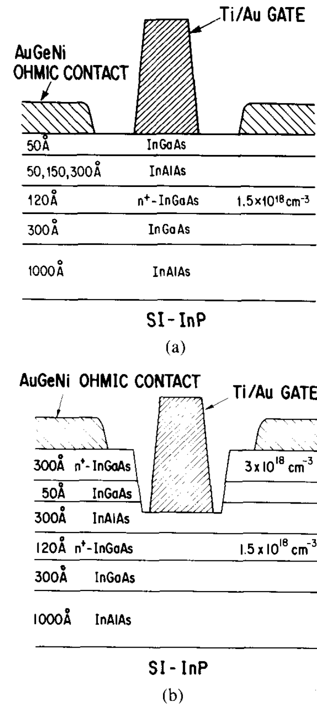

Fig. 1. Schematic cross section of fabricated devices. (a) Undoped-cap MIDFET. (b) Recessed-gate MIDFET. Three undoped-cap devices were fabricated with $In_{0.52}Al_{0.48}As$ thicknesses of 50, 150, and 300 Å.

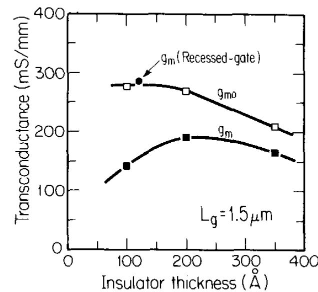

Fig. 2. Measured extrinsic transconductance g_m and estimated intrinsic transconductance g_{mo} for undoped-cap MIDFET's as a function of total device insulator thickness (see text). The extrinsic transconductance of the recessed-gate MIDFET is also shown. The device gate dimensions are in all cases 1.5×200 μm^2.

Fig. 2 reveals that the extrinsic transconductance g_m of the undoped-cap MIDFET's initially increases as the insulator is scaled down, but drops precipitously beyond about 200 Å.

In order to understand the origin of this loss of transconductance in thin-insulator MIDFET's, we have measured the contact resistance R_c and the sheet resistance of the extrinsic channel R_{sh} using the TLM technique [13]. With these two parameters, we have estimated the source

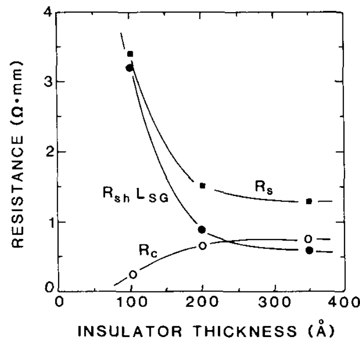

Fig. 3. Values of contact resistance (R_c), extrinsic channel resistance ($R_{sh}L_{SG}$), and source resistance (R_s) of undoped-cap MIDFET's as a function of total insulator thickness ($W_i + W_c$).

resistance R_s. Fig. 3 plots R_s and its two components, the contact resistance and the resistance of the extrinsic channel $R_{sh}L_{SG}$ (where $L_{SG} \simeq 1$ μm is the source-to-gate separation), as a function of total insulator thickness.

As Fig. 3 indicates, R_s quickly increases for undoped-cap MIDFET's with an insulator thickness lower than 200 Å. The extrinsic-channel resistance $R_{sh}L_{SG}$ is found to be responsible for this behavior since, as it should be expected, the contact resistance decreases with insulator thickness. A discussion on the scaling properties of the extrinsic-channel resistance is carried out in Section IV.

From the knowledge of the source resistance, we have estimated the intrinsic transconductance g_{mo} through the expression $g_{mo} = g_m/(1 - g_m R_s)$. The open squares in Fig. 2 represent g_{mo} for the undoped-cap MIDFET's. g_{mo} increases significantly as the insulator thickness is scaled down to about 200 Å, but beyond this value, g_{mo} appears to saturate. The phenomenon responsible for this g_{mo} saturation has not been investigated.

In contrast with this behavior, the recessed-gate MIDFET shows a very high extrinsic transconductance, 285 mS/mm (see Fig. 2). As discussed above, we cannot estimate the intrinsic transconductance of this device. It is clear, however, that the recessed-gate structure results in extremely low source resistance, since its g_m is comparable to the g_{mo} of the undoped-cap MIDFET's. The threshold voltage of the recessed MIDFET indicated that, as a result of the recess process, the insulator thickness had been reduced to about 120 Å of $In_{0.52}Al_{0.48}As$. This value was consistent with the calibrated etch rate of the chemical etchant.

The recessed-gate MIDFET structure is therefore successful in reducing the source resistance and obtaining large values of extrinsic transconductance. Fig. 4 shows the common-source I-V characteristics of a 1.5 × 200 μm gate-recessed device. The threshold voltage V_{th} is about −0.5 V. Good pinchoff characteristics are obtained. Fig. 5 shows the transconductance as a function of gate–source voltage for the same device and the three undoped-cap MIDFET's (labeled in the figure as "reference FET"), with the insulator thickness as parameter.

Microwave measurements were also performed on the same devices up to 26.5 GHz. From the measured S parameters, the current gain h_{21} was deduced. Fig. 6 displays h_{21} as a function of frequency for the recessed-gate device. h_{21} exhibits a −6-dB/octave slope at high frequencies. The current-gain cutoff frequency f_T of this device was found to be 19.4 GHz at $V_{DS} = 2.5$ V and $V_{GS} = 0.5$ V, as Fig. 6 shows. The undoped-cap MIDFET with 300-Å $In_{0.52}Al_{0.48}As$ thickness showed, on the other hand, an f_T of 15.2 GHz at $V_{DS} = 4.0$ V and $V_{GS} = -0.8$ V. This result is in line with what we obtained previously on a 2-μm gate-length devices [5] when the difference of gate lengths is taken into consideration. The f_T of our 1.5-μm recessed-gate MIDFET is higher than reports on comparable gate length $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ MODFET's [14].

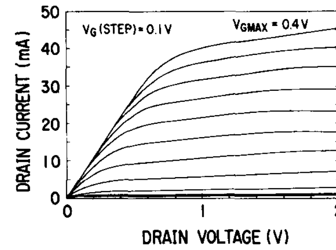

Fig. 4. Common-source current-voltage characteristics of a 1.5 × 200 μm² gate recessed MIDFET. The maximum gate-source voltage is 0.4 V. The gate-source voltage step is 0.1 V.

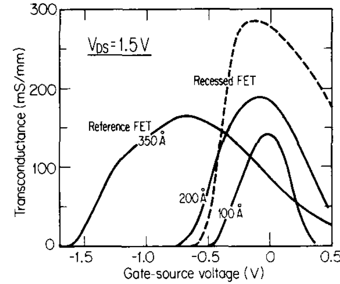

Fig. 5. Transconductance versus gate-source voltage for the 1.5 × 200 μm² recessed-gate MIDFET and the three undoped-cap MIDFET's (labeled "reference") with the total insulator thickness as a parameter.

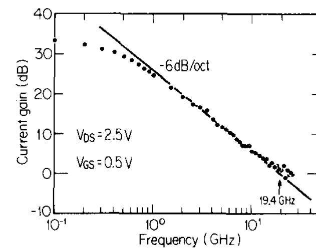

Fig. 6. Current gain as a function of frequency for recessed-gate MIDFET with 1.5 × 200 μm² gate dimensions.

IV. Discussion

The TLM measurements revealed that the increase in the source resistance of the conventional MISFET's that occurs as the $In_{0.52}Al_{0.48}As$ thickness is scaled down resulted from a large increase in the sheet resistance of the

extrinsic channel (see Fig. 3). The underlying cause of this behavior is the Fermi level pinning that occurs at the semiconductor surface. This is illustrated in the schematical equilibrium cross-section conduction band diagram of the extrinsic portion of the device shown in Fig. 7(a). As the figure indicates, surface Fermi level pinning partially depletes the extrinsic n^+-channel. The thickness of this depletion layer W_d can easily be shown to be

$$W_d = \sqrt{\left(\frac{\epsilon_s}{\epsilon_i} W_i + W_c\right)^2 + \frac{2\epsilon_s}{qN_D}(\phi_B - \phi_n)} - \left(\frac{\epsilon_s}{\epsilon_i} W_i + W_c\right) \quad (1)$$

where W_c and W_i represent, respectively, the thickness of the undoped $In_{0.53}Ga_{0.47}As$ cap and the undoped $In_{0.52}Al_{0.48}As$ insulator; ϵ_i and ϵ_s indicate, respectively, the permittivity of $In_{0.52}Al_{0.48}As$ and $In_{0.53}Ga_{0.47}As$; $q\phi_B$ is the energy barrier height at the surface; $q\phi_n$ is the energy difference between the conduction band edge and the Fermi level in the conducting channel; N_D is the doping level of the channel.

In deducing (1), we have assumed that the residual doping level of the nominally undoped $In_{0.53}Ga_{0.47}As$ and $In_{0.52}Al_{0.48}As$ layers is negligible in comparison with the active-channel doping level. This is a plausible assumption, since our nominally undoped $In_{0.53}Ga_{0.47}As$ layers have a residual donor doping in the mid 10^{15} cm^{-3} level. We have not estimated the residual doping level of the $In_{0.52}Al_{0.48}As$ layers, but it is expected also to be of that order.

The sheet resistance of the extrinsic source can be calculated through

$$R_{sh} = \frac{1}{q\mu_e N_D (W_{ch} - W_d)} \quad (2)$$

where q is the electron charge, μ_e is the electron mobility, and W_{ch} is the thickness of the active channel.

We have calculated R_{sh} for various $In_{0.52}Al_{0.48}As$ thicknesses and doping levels, and the result is shown in Fig. 8. Many of the parameters that enter in the calculation are not very well known in $In_{0.53}Ga_{0.47}As$ and $In_{0.52}Al_{0.48}As$. For ϕ_B we have taken 0.2 eV [15]. In the calculation of ϕ_n we have used Fermi–Dirac statistics and a value of 0.041 for the electron effective mass [16]. ϵ_s and ϵ_i have been taken, respectively, as $13.9\epsilon_0$ and $12.4\epsilon_0$ [16], where ϵ_0 is the free-space permittivity. Electron mobility measurements as a function of doping level (from Fujii *et al.* [17]) have been used.

Fig. 8 shows that as the insulator thickness decreases, the sheet resistance of the extrinsic source increases very rapidly, particularly for low doping levels. In spite of the lack of precise knowledge of the physical parameters involved in the calculation, reasonable agreement is found between the theoretical values and the experimental measurements. The required doping level for the channel doping level is between 1.5 and 4.0 × 10^{18} cm^{-3}, in substantial agreement with the nominal 1.5 × 10^{18} cm^{-3}. For low insulator thickness, R_{sh} is a very strong function of it. In consequence, small variations in the MBE growth-rate calibration may result in large variations in R_{sh}.

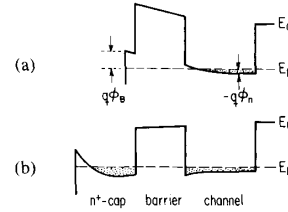

Fig. 7. Schematical cross section of conduction band diagram of extrinsic device in (a) an undoped-cap MIDFET, and (b) a recessed-gate MIDFET.

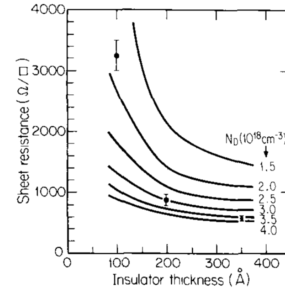

Fig. 8. Sheet resistance of extrinsic n^+-channel in a conventional MIDFET as a function of total insulator thickness and channel-doping level. Experimental measurements are also indicated.

Fig. 8 drastically illustrates the need for a recessed-gate structure in scaled MIDFET's. n^+-$In_{0.53}Ga_{0.47}As$ cap layers have been extensively used in $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ MODFET's to reduce source resistance [10], [11]. They are effective because electrons tunnel across the n^+-$In_{0.53}Ga_{0.47}As$/n-$In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ heterostructure that exists at the extrinsic channel [12]. In the n^+-$In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$/$n^+$-$In_{0.53}Ga_{0.47}As$ structure of the extrinsic MIDFET this mechanism is very unlikely. This is because the $In_{0.52}Al_{0.48}As$ layer is undoped and the large conduction-band discontinuity between $In_{0.52}Al_{0.48}As$ and $In_{0.53}Ga_{0.47}As$ (about 0.5 eV [18]) precludes any significant thermionic emission or tunneling across the barrier.

Fortunately, a different mechanism is expected to bring about a reduction in the source resistance of $In_{0.52}Al_{0.48}As$/n^+-$In_{0.53}Ga_{0.47}As$ MIDFET's when a n^+-$In_{0.53}Ga_{0.47}As$ cap is utilized. The fundamental concept is illustrated in Fig. 7(b), which shows a cross section of the extrinsic portion of the $In_{0.52}Al_{0.48}As$/n^+-$In_{0.53}Ga_{0.47}As$ MIDFET with an n^+-$In_{0.53}Ga_{0.47}As$ cap. The effect of the cap, if heavily doped, is to force the Fermi level to penetrate well inside the conduction band of the cap layer. Since the $In_{0.52}Al_{0.48}As$ layer is undoped, the edge of the conduction band in the n^+-$In_{0.53}Ga_{0.47}As$ channel is also lowered at its interface with the $In_{0.52}Al_{0.48}As$ layer. This not only impedes the formation

of a depletion region, but even creates a small electron-accumulation layer at the $In_{0.52}Al_{0.48}As/n^+$-$In_{0.53}Ga_{0.47}As$ interface. The overall effect is a reduction in the sheet resistance of the extrinsic channel.

An important feature of this phenomenon is that there should be negligible current flow in the n^+-cap of a recessed MIDFET. This appears not to be the case in MODFET's in which current flows along the n^+-cap and across the doped wide-bandgap material down to the channel. In our MIDFET this current path is very unlikely, as mentioned above, and as a result, the cap does not need to exceed the thickness of the space-charge region that is formed at the surface due to surface Fermi level pinning (see Fig. 7(b)). For a doping level of 3×10^{18} cm^{-3}, this thickness is only about 130 Å. A thin cap has many important manufacturing advantages that stem from the shallow recess required before gate metal deposition.

V. Conclusions

Simple scaling of the insulator thickness of $In_{0.52}Al_{0.48}As/n^+$-$In_{0.53}Ga_{0.47}As$ MIDFET's results in degraded performance due to increased sheet resistance of the extrinsic channel. This is a consequence of Fermi level pinning at the surface of the semiconductor. The efficacy of a thin n^+-$In_{0.53}Ga_{0.47}As$ cap in reducing the source resistance of $In_{0.52}Al_{0.48}As/n^+$-$In_{0.53}Ga_{0.47}As$ MIDFET's has been demonstrated by fabricating a 1.5-μm gate-length device that showed a transconductance of 285 mS/mm and a current-gain cutoff frequency of 19.4 GHz. This recessed-gate structure is favored for scaled down MIDFET's. This work confirms the potential of doped-channel MIS-type FET's for high-frequency applications.

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From 1977 to 1981, he was a Research Assistant at the Institute of Solar Energy of the Polytechnic University of Madrid, working on silicon solar cells. From 1985 to 1988, he was a Research Engineer with the Nippon Telegraph and Telephone Corporation at the NTT LSI Laboratories in Atsugi, Japan. There he conducted research on heterostructure field-effect transistors based on InP, InAlAs, and InGaAs, fabricated by molecular-beam epitaxy. He is presently an Assistant Professor in the Department of Electrical Engineering and Computer Science of the Massachusetts Institute of Technology, Cambridge, where he is continuing research on heterostructure devices based on compound semiconductors.

Dr. del Alamo received the first prize in the 1980 IEEE Region 8 Undergraduate Student Paper Contest, and an Electrochemical Society Research Summer Fellowship Award in 1983. He was a Vinton Hayes Fellow at MIT during 1988. He is a member of the Electrochemical Society, the American Physical Society, and the Japanese Society of Applied Physics.

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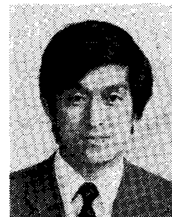

Takashi Mizutani (M'84) was born in Gifu, Japan, on October 12, 1948. He received the B.S., M.S., and Ph.D. degrees in electronic engineering from Nagoya University, Aichi, Japan, in 1971, 1973, and 1984, respectively.

In 1973, he joined Musashino Electrical Communication Laboratory, Nippon Telegraph and Telephone Public Corporation, Tokyo, Japan, where he worked on planar Gunn effect functional devices, development of ion-implanted FET's, fabrication of GaAs IC's, and characterization of GaAs substrates for GaAs IC's. In 1983, he moved to the NTT Atsugi Electrical Communications Laboratories, Kanagawa, Japan. His current research interests include high-speed device design and performance in heterostructure FET's and MESFET's, characterization of heterostructures, and current transport in heterostructures. He is currently a Senior Research Engineer in the Heterostructure Device Section and responsible for research and development of heterostructure FET's.

Dr. Mizutani is a member of the Institute of Electrical and Communication Engineers of Japan and the Japan Society of Applied Physics.