A Self-Aligned Enhancement-Mode AlGaAs/InP MISFET

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Abstract—**An enhancement-mode insulated-gate field-effect transistor (FET) has been fabricated by a self-aligned technique on semi-insulating InP substrate with an AlGaAs gate barrier grown by molecular beam epitaxy (MBE). A device with a gate length of 1 μm exhibited a transconductance of 134 mS/mm and a threshold voltage of 0.9 V. The characteristics are insensitive to light down to 77 K and hysteresis is completely absent. The performance of this device shows that the fabrication of enhancement-mode devices on severely lattice-mismatched heterostructures is feasible.**

InP is a promising semiconductor for the fabrication of field-effect transistors (FET's) for microwave high-power applications and optoelectronic integration with long-wavelength optical communication devices. Normally-off or enhancement-mode metal–insulator–semiconductor (MIS) type FET's [1] have received a great deal of attention because they are particularly well suited for high-speed digital circuits.

Up to the present time, enhancement-mode MISFET's based on InP have made use of dielectric materials as gate insulator, in particular SiO_2 [2]. A fundamental problem of this approach lies in the damage inflicted upon the active interface of the device during the deposition of the dielectric [3]. In comparison with MISFET type devices based on GaAs [4] or InGaAs [5] fabricated by molecular beam epitaxy (MBE), the maximum transconductance reported to date is only 220 mS/mm on a 0.8-μm-long gate device [1].

The use of MBE for the gate fabrication of InP MISFET's offers a number of potential advantages over the conventional SiO_2 approach. *In-situ* cleaning of the active interface has been shown to be possible by heating the sample under an As flux [6]. In addition to this, a passivating InAs surface appears to be formed as a result of this cleaning procedure [7], [8] with a markedly reduced interface state density [9]. A final merit of the use of MBE lies in the flexibility for gate design given by the wide range of materials that can be grown and the possibility of growth control at the atomic layer level.

In contrast with FET's based on GaAs and InGaAs, lattice-matched gate-barrier semiconductors which offer sufficient conduction-band discontinuity over InP are not available in conventional MBE. The fabrication of FET's on InP by MBE therefore necessitates the use of strained or mismatched gate semiconductors. In this letter we explore the feasibility of the use of mismatched AlGaAs as a gate barrier. Recently a depletion-mode AlGaAs/InP FET using a conducting n-channel has been demonstrated [10]. An enhancement-mode device on a semi-insulating substrate, however, poses more stringent demands on the quality of the heterointerface, and requires the preservation of the integrity of the gate structure during the self-aligned process.

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The devices were fabricated on semi-insulating Fe-doped (100) InP wafers. After etching the substrates using the procedure of Nishitani and Kotani [11], the samples were introduced into an MBE apparatus. The substrates were heated under the flux of an As beam to about 500°C, a temperature at which the surface oxides desorb [6]. This "*in-situ*" cleaning technique results in a two-monolayer InAs surface on the InP substrate just immediately before growth [7], [8]. Next 450 Å of $Al_{0.3}Ga_{0.7}As$ and 50 Å of GaAs are grown at the same substrate temperature. The total gate-barrier thickness was confirmed to within 10 percent by means of an Alpha-Step 200 profilometer.

The rest of the process is essentially identical to that of self-aligned MISFET structures fabricated in the AlGaAs/GaAs system [12]. In summary, WSi_x as gate electrode is deposited by sputtering and patterned using CF_4 reactive ion etching. The gate semiconductor is subsequently chemically etched with a selectivity over InP better than 100:1. Si ion implantation is performed at 100 keV to a dose of 5×10^{13} cm^{-2} and is rapid thermal annealed at 700°C for 4 s using a capless technique. This results in a sheet resistance of 500 Ω/sq. AuGeNi ohmic metal is subsequently evaporated and alloyed at 400°C for 30 s. A Ti/Au cover is evaporated to provide low-resistance probing pads to the source, drain, and gate. The resulting structure is schematically shown in Fig. 1.

The measured I–V characteristics at 300 K of a device with a 1×20-μm^2 gate are shown in Fig. 2. The maximum extrinsic transconductance is obtained at $V_{DS} = V_{GS} = 4.5$ V and is 134 mS/mm. The gate–source resistance is 1.25 Ω·mm which arises from a 0.25-Ω·mm contact resistance and a 1.00-Ω·mm resistance of the n^+-implanted layer. Of special relevance is the lack of hysteresis, commonly observed in devices based on SiO_2 [1], and the light insensitivity, down to liquid nitrogen temperature (77 K), of the characteristics shown in Fig. 2.

Fig. 3 displays the square root of the drain current versus the gate voltage for the same device at $V_{DS} = 4$ V. A linear dependence is obtained at high voltages. The extrapolation of this line to zero drain current gives a threshold voltage of 0.9 V. From its slope, a K value of 21.6 mA/V^2·mm can be extracted.

Fig. 4 summarizes the best transconductance and K-value

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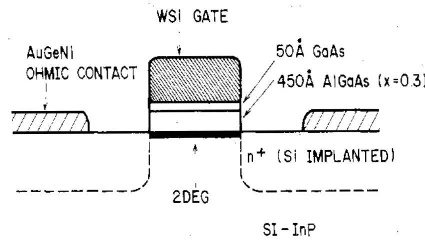

Fig. 1. Schematic cross section of AlGaAs/InP MISFET.

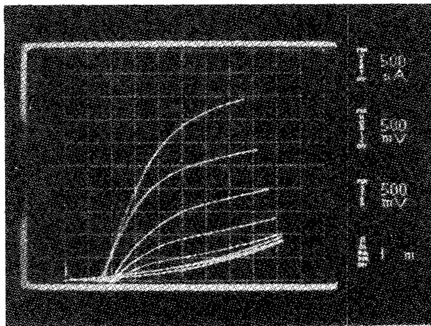

Fig. 2. Current-voltage characteristics of a $1 \times 20\text{-}\mu m^2$ gate device at room temperature. The gate-source voltage is stepped from 0 to 4 V in 0.5-V intervals.

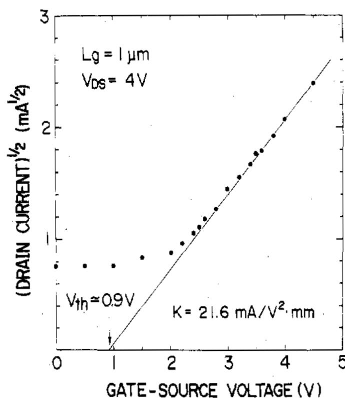

Fig. 3. Square root of drain current versus gate-source voltage for the same device of Fig. 2 at room temperature.

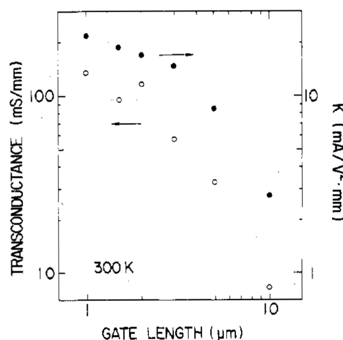

Fig. 4. Summary of best transconductance and K-value results as a function of gate length. The gate width in all cases is 20 μm.

results obtained in various devices as a function of gate length. The gate width in all cases is 20 μm.

In both Figs. 2 and 3 the absence of pinch-off is observed. Additionally, significant leakage current flows between gate and source (drain). For the device shown in Figs. 2 and 3, this leakage current reaches 8.5 mA when source and drain are short circuited and the gate-source voltage is 4 V. While we do not have direct evidence yet, these occurrences may be related to the probable presence of misfit dislocations inside the epitaxial gate barrier. In a $GaAs/In_{0.53}Ga_{0.47}As$ system [13], which has a similar lattice mismatch as the present AlGaAs/InP system, about 3.6-percent, dislocations have been observed by cross-sectional TEM for the same layer thickness [14]. In fact, using the theory of Matthews and Blakesklee [15], the critical layer thickness for this degree of mismatch in a bilayer system is found to be around 13 Å. In spite of the large lattice mismatch and the possible occurrence of misfit dislocations, the fabrication of enhancement-mode FET's on severely lattice-mismatched heterostructures is demonstrated to be feasible.

In conclusion, an AlGaAs/InP enhancement-mode MIS-type FET has been demonstrated. A maximum transconductance of 134 mS/mm and a threshold voltage of 0.9 V are obtained in a 1-μm-long gate device. The use of mismatched semiconductors for the fabrication of MISFET's on InP appears to be a promising alternative to the conventional SiO_2 technology.

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