Forward-Bias Tunneling: A Limitation to Bipolar Device Scaling

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Abstract—**Forward-bias tunneling is observed in heavily doped p-n junctions of bipolar transistors. A simple phenomenological model suitable to incorporation in device codes is developed. The model identifies as key parameters the space-charge-region (SCR) thickness at zero bias and the reduced doping level at its edges which can both be obtained from *CV* characteristics. This tunneling mechanism may limit the maximum gain achievable from scaled bipolar devices.**

THE SCALING of silicon bipolar transistors demands a reduction in the base thickness and an accompanying increase in the base doping level. Among the peculiar physical phenomena that arise from high base impurity concentrations [1], [2], forward-bias tunneling in the base–emitter junction has received little attention. Forward-bias tunneling currents, however, have been recently observed at the periphery of self-aligned polysilicon bipolar transistors across the junction formed by the emitter and the heavily doped extrinsic-base contact [3], [4]. Adequate spacer technology has achieved the suppression of this perimeter tunneling. As device scaling advances and the intrinsic base doping level is raised, tunneling is expected to occur at the whole emitter–base area. This may pose a limitation to the gain of scaled bipolar transistors.

While a great deal of research was carried out in the sixties on forward-bias tunneling currents in heavily doped p-n junctions, the experimental work was confined to alloyed junctions and the theoretical formulations were too cumbersome to be incorporated in device modeling programs. The work that we present here attempts to fill this gap. We have carried out detailed experiments using modern technology and we have developed a simple theory that accounts for the main features of the observations. The theoretical formulation identifies two key parameters responsible for the observed tunneling phenomena. These two parameters are routinely calculated in available device modeling programs and the model is therefore suitable for immediate incorporation into existing device numerical codes.

The transistors used in the present work were designed to measure the hole transport parameters in heavily doped n-type silicon [5]. In brief, the base was fabricated by epitaxy and is therefore uniformily doped with phosphorus to a value that can be measured very precisely [6]. Subsequently, B was implanted to a total dose of 9×10^{15} cm^{-2} (4×10^{15} cm^{-2} at 100 keV, 3×10^{15} cm^{-2} at 60 keV, and 2×10^{15} cm^{-2} at 35 keV) and thermally annealed at 1050°C during 30 min. The *I–V* and *CV* characteristics of the resulting p^{++}-n^{+} diode were measured in forward bias at 297 K. The reported data correspond to 100×100-μm^2 area devices, but measurements on larger diodes confirmed that the peripheral component of the current and capacitance were negligible. The devices considered in this work had base doping levels ranging from 8.8×10^{17} to 4.0×10^{19} donors per cubic centimeter.

Forward *I–V* curves of selected devices are shown in Fig. 1. At low voltages a strong increase in the current occurs as the base donor doping level is raised beyond approximately 5×10^{18} cm^{-3}. This "excess current" is essentially exponential and can then be fitted with an equation of the form

$$I_T = A J_{oT} \exp \frac{V}{V_T} \tag{1}$$

where J_{oT} is denoted as the tunneling saturation current and V_T as the characteristic tunneling voltage. The space-charge-region (SCR) width W_{SCR} and the reduced doping level $N_a N_d/(N_a + N_d)$ at the SCR edge were obtained from the *CV* characteristics for small forward bias. N_a and N_d denote the net acceptor and donor concentrations at the edges of the SCR, respectively. Preliminary results were presented in [7].

Two theoretical explanations of the "excess current" observed in Esaki diodes at higher voltages than required to uncouple the conduction and valence bands were postulated in the sixties [8], [9]. The most intuitive one involves midgap states inside the SCR [8] (see the inset of Fig. 1). If a localized state inside the forbidden gap is energetically aligned with an occupied state of the conduction band of the n region, an electron may be able to tunnel into the state. It can later recombine with a valence band hole of the p region through a Shockley–Read–Hall process. An alternative explanation does not require localized states inside the gap but shallow impurities at the edges of the SCR [9]. While our experiments cannot differentiate between both hypotheses, they both have in common a tunneling process across the junction SCR that becomes the rate limiting step of the total transition. To the first order, the tunneling probability through a potential barrier of height E_T and thickness W (see, for example, [10]) is

$$T \approx \exp\left(-\frac{2W}{\hbar}\sqrt{2m^* E_T}\right). \tag{2}$$

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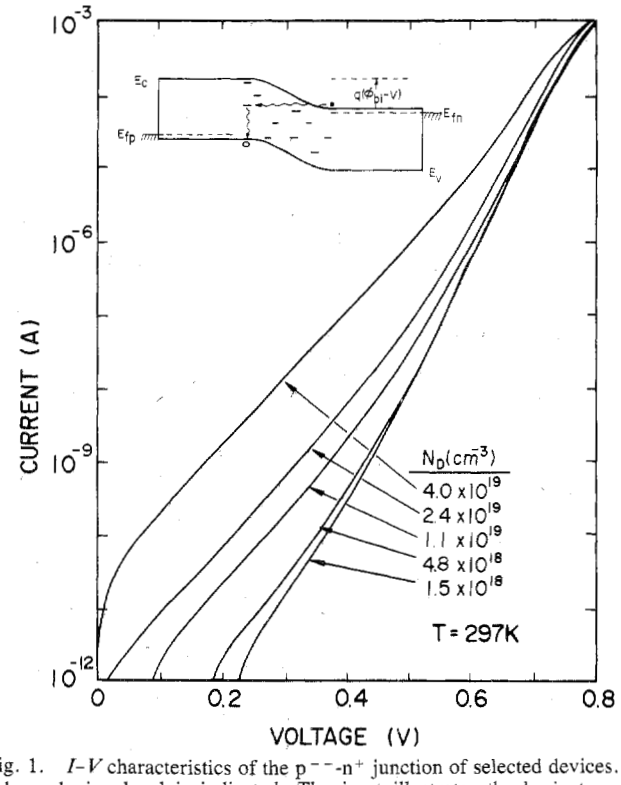

Fig. 1. I–V characteristics of the p^{--}-n^{+} junction of selected devices. The base doping level is indicated. The inset illustrates the basic tunneling process assisted by midgap states. Note that alternative explanations that do not require the existence of midgap states have been formulated.

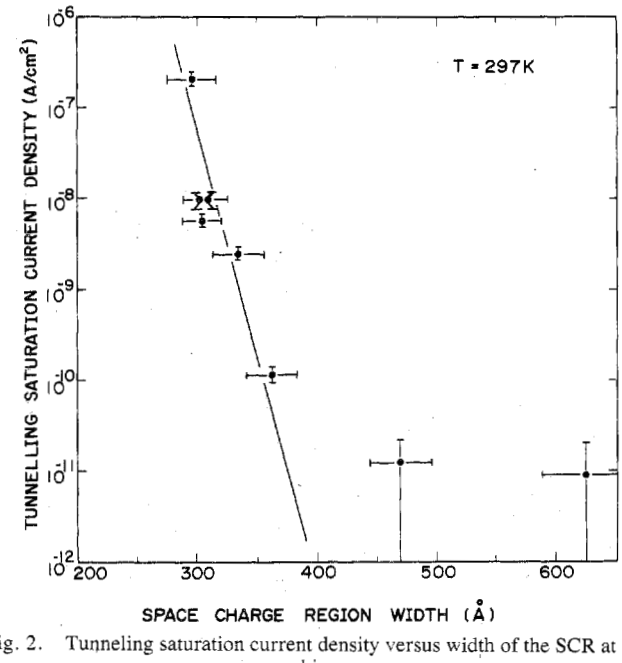

Fig. 2. Tunneling saturation current density versus width of the SCR at zero bias.

For a triangular or parabolic barrier additional numerical factors in the argument of the exponential appear but identical dependences of T on W and $\sqrt{E_T}$ are found [11].

In a p-n junction the height of the barrier to tunneling, as shown in Fig. 1, is $E_T = q(\phi_{bi} - V)$, where ϕ_{bi} is the junction built-in voltage. The thickness of the tunneling barrier is approximately, for an abrupt junction

$$W_{SCR}(V) = \sqrt{\frac{2\epsilon_s}{q}\frac{N_a+N_d}{N_aN_d}(\Phi_{bi}-V)}\,. \tag{3}$$

For other junctions, the voltage dependence of W_{SCR} may have a different functional form. However, for small forward voltages, $W_{SCR}(V)$ is not very sensitive to V and (3) suffices. Equation (2) can then be rewritten as

$$T \approx \exp\left[-\frac{2}{\hbar}\sqrt{2m^*q\Phi_{bi}}\,W_{SCR}(0)\right] \cdot \exp\left[\frac{4\sqrt{m^*\epsilon_s}}{\hbar}\sqrt{\frac{N_a+N_d}{N_aN_d}}\,V\right] \tag{4}$$

and the tunneling probability exponentially increases with the forward voltage.

Within the theoretical frame that involves midgap states, a tunneling current exponentially increasing with voltage requires a midgap state distribution that is exponential or uniform in energy. The first alternative is expected if band tailing of the conduction and valence band edges occurs due to heavy doping [12]. Tails are expected to extend very deep into the forbidden gap in the SCR because of the lack of mobile carriers that screen the dopant impurities in neutral regions [13]. Alternatively, the theory that requires only the existence of shallow states does not impose any restrictions on their energy distribution. In both cases, then, $I_T \approx T$, and, from (4), the tunneling current may be approximately described by an equation like (1) with J_{oT} depending exponentially on the junction width at zero bias $W_{SCR}(0)$ ($\Phi_{bi}^{1/2}$ is a rather insensitive function of doping)

$$J_{oT} \simeq k_1 \exp\left[-k_2 W_{SCR}(0)\right] \tag{5}$$

and V_T depending linearly on the square root of the reduced doping level

$$V_T \simeq k_3\sqrt{\frac{N_aN_d}{N_a+N_d}}\,. \tag{6}$$

The dependences contained in (5) and (6) are verified in our experiments. In fact, Fig. 2 displays J_{OT} versus $W_{SCR}(0)$ and indeed an exponential dependence is shown to appear when $W_{SCR}(0)$ is smaller than about 400 Å. Fig. 3 plots the square of V_T against the reduced doping level. The data fit a straight line that crosses the origin, as expected from (6). The values of the constants that appear in (5) and (6) can be extracted: $k_1 = 6.02 \times 10^7$ A/cm^2, $k_2 = 1.15 \times 10^7$ cm^{-1}, and $k_3 = 4.28 \times 10^{-11}$ $V\cdot$cm$^{3/2}$.

The temperature dependence of the currents under consideration has also been studied. The model predicts that J_{oT} depends exponentially, with a minus sign, on the bandgap (through Φ_{bi}, and that V_T is essentially independent of T (see (4)). In fact, such expectations have been observed in our experiments [7]. The exponential dependence of J_{oT} on the silicon bandgap unequivocally confirms the tunneling nature

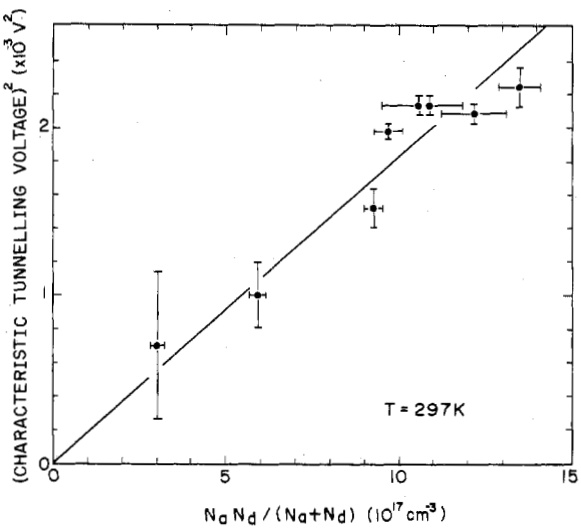

Fig. 3. Square of the characteristic tunneling voltage versus reduced doping level at the edges of the SCR.

of the current under investigation and rules out its interpretation as a recombination current inside the SCR, since J_{oT} is not thermally activated. Additionally, V_T was found to change less than 10 percent when the temperature spans a range of 160 K [7], confirming the temperature independence predicted by (4).

The model defined by (1), (5), and (6) can easily be incorporated in device modeling codes. The model identifies W_{SCR} and $N_aN_d/(N_a + N_d)$ as the key parameters controlling tunneling. These parameters are routinely predicted by existing numerical analysis programs. The constants involved, however, are expected to be somewhat process dependent. The fact that our experiments are performed on p^{++}-n^+ junctions does not limit the applicability of the results of this paper to the more practical n^{++}-p^+ junctions. The current simply flows in the opposite direction.

The tunneling current discussed in this work may limit the maximum gain achievable in scaled bipolar devices. By fabricating the devices by techniques, like MBE, that allow the preparation of a dopant-free SCR, tunneling may be suppressed [14]. Our data indicate that a 400-Å SCR yields negligible tunneling through it, but this may be too wide for high-speed devices.

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