MAJORITY AND MINORITY CARRIER TRANSPORT IN POLYSILICON EMITTER CONTACTS

E. Crabbé, S. Swirhun, J. del Alamo, R. F. W. Pease, and R. M. Swanson

Solid State Electronics Laboratories
Stanford University, Stanford, California, 94305

ABSTRACT

The minority hole transport in polysilicon emitter contacts has been studied with a novel pnp test transistor. Segregated arsenic at the polysilicon/silicon interface is mostly responsible for the base current reduction in polysilicon-contacted npn transistors. This improvement comes at a price of a higher emitter resistance. This resistance was measured with a Kelvin resistor structure and the base current/emitter resistance trade-off is quantified.

INTRODUCTION

Polysilicon emitter contacts play an increasingly important role in high-speed npn bipolar transistors and as vertical dimensions are scaled down, they become crucial for emitter thicknesses of 0.1 μm or less [1]. The decrease in base current of such devices has been extensively reported and several models to explain it have been proposed. The interface between the silicon and the polysilicon contact is now recognized to play the dominant role when the anneal conditions do not deteriorate the interfacial oxide present [2]. De Graaff and de Groot [3] have proposed that the thin interfacial oxide acts as a tunneling barrier against hole injection into the polysilicon. More recently, Neugroschel et al. [4] have shown the importance of arsenic segregation at this interface for reducing the base current. It is difficult to distinguish between these two mechanisms by measuring only the base current of standard npn transistors. We have devised a test transistor which is much more sensitive to the interface in order to study the transport of minority holes across it.

The improvement in base current reduction comes however with a higher emitter resistance. This parasitic resistance degrades the transconductance of the device and its switching performance [5]. The trade-off between base current reduction and increase in emitter resistance is investigated here as a function of interface treatments and anneal conditions. The emitter resistance measurements were obtained with a cross-bridge Kelvin structure.

HOLE INTERFACE TRANSPORT

The emitter saturation current density which can be obtained from the ideal component of the base current when negligible base recombination occurs, is a measure of the total hole injection into the emitter. This hole current has three components: recombination in the single-crystal part of the emitter, recombination at the interface and injection into the polysilicon. In order to distinguish between the passivating and the barrier behavior of the interface, it is desirable to measure the hole current that has crossed the interface. A pnp transistor with the critical interface located in the base will allow such a measurement (Fig. 1). The device is operated in the inverted mode with the substrate acting as the emitter. The base profile is identical to the npn single-crystal emitter profile. Placing the base-collector rather than the emitter-base junction in the polysilicon eliminates the problems associated with biased polysilicon p-n junctions. The effect of the bulk polysilicon on minority hole transport is minimized by locating the base-collector junction in close proximity to the interface. The collector current is hence a direct measure of the number of holes that traverse the interface.

Experimental Details

Two types of pnp transistors were fabricated to vary the segregation of arsenic at the interface. In the first type (single-poly devices), arsenic diffuses from the implanted base into the undoped polysilicon during the anneal at 900°C. At this temperature, the grain-boundary diffusion coefficient of arsenic is almost three orders of magnitude larger than that in single-crystal [6]. Thus, the polysilicon is a sink for arsenic and little pile-up occurs at the interface as verified by SIMS analysis. The purpose of the second set of transistors (double-poly devices) was to ensure arsenic segregation at the interface by implanting the polysilicon with arsenic. Following a 900°C anneal, the polysilicon was thinned to 25-30 nm by plasma etching and a second polysilicon film was deposited. Both sets of transistors received a heavy boron implant and rapid thermal anneal at 750°C to activate the dopant atoms. SIMS analysis confirmed that this short anneal minimizes boron diffusion to the interface. The arsenic surface concentration ($1x10^{20}$ cm^{-3}) and anneal conditions were chosen to preserve the integrity of the thin native interfacial oxide [2].

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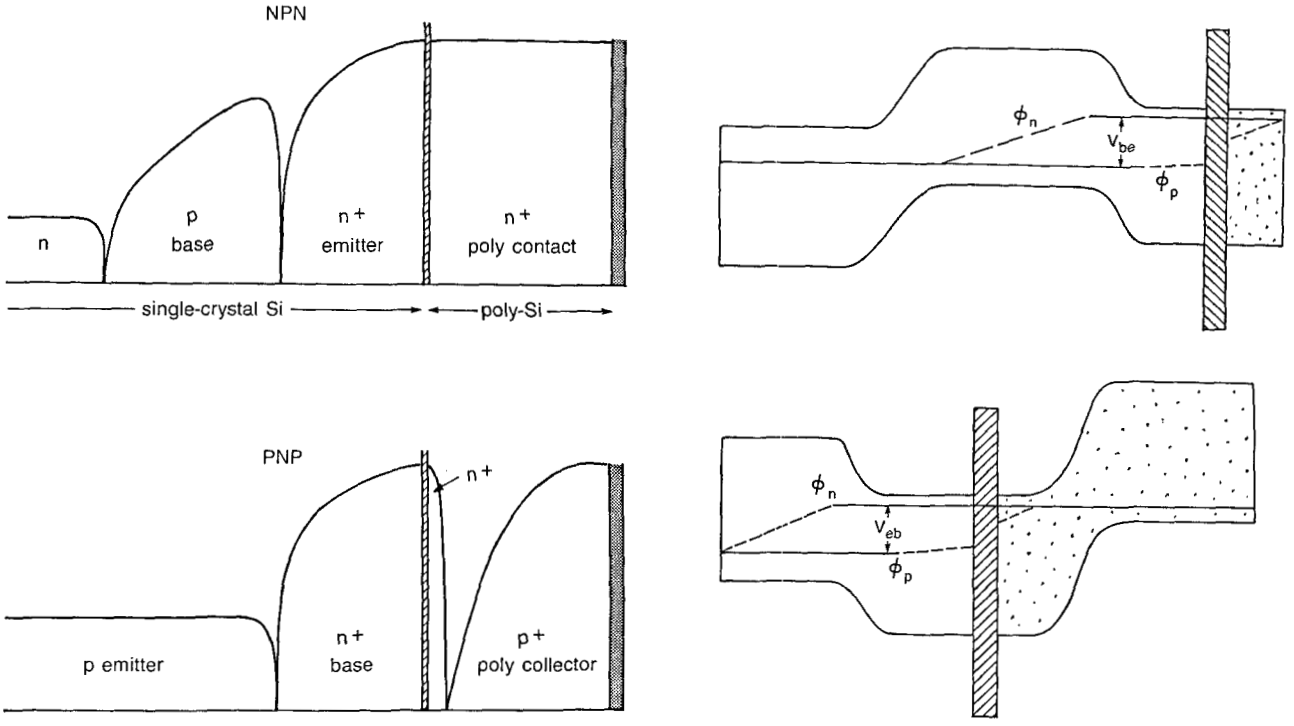

Fig. 1 Cross sections and band diagrams of npn polysilicon-emitter transistor and of pnp test structure with the polysilicon-single crystal interface in the base.

Results and Discussion

Figure 2 shows typical I-V characteristics for a double-poly pnp transistor. The base current is ideal over many orders of magnitude and is dominated by injection of holes in the substrate. The collector characteristic has the ideal exponential characteristic over a small range between the low-bias region dominated by the high leakage current of the base-collector junction and the high-bias region dominated by the emitter series resistance caused by the low doping of the substrate.

The collector saturation current density J_{oe} for a double-poly device at 300K is 3.5×10^{-14} A/cm^2 compared to 4×10^{-12} A/cm^2 for a single-poly device. As they both received identical interface treatments, the two order of magnitude decrease in J_{oe} can only be attributed to the presence of arsenic at the interface of the double-poly device. This is a confirmation of the results of Neugroschel et al. [4] demonstrating the importance of arsenic segregation at the interface to reduce hole injection into the polysilicon. The presence of arsenic at the interface has a much stronger effect on J_{oe} than the interfacial oxide. Nonetheless this thin native oxide is necessary to prevent epitaxial realignment, and it may act as a sink for arsenic facilitating the electrical activation of the segregated arsenic atoms at the interface.

In order to gain some understanding about hole transport across the interface, we investigated the temperature dependence of the collector saturation current of these devices in the range 280 K to 419 K. To remove the dominant temperature dependence of n_i^2, the collector current was divided by the base current. This base current is ideal over a larger range of biases and does not have a bandgap narrowing temperature dependence as the substrate (emitter) is lowly doped. The current gain in the double-poly devices has a positive temperature coefficient with an activation energy of 130meV. It is important to realize that the bandgap narrowing in the base which is heavily doped should lead to a negative temperature coefficient. A second double-poly device with an arsenic chemical concentration of 5×10^{-19} cm^{-3} exhibited a similar temperature dependence with an activation energy of 120meV. By contrast, the temperature dependence of the single-poly device with no arsenic is much lower with an activation energy of 32meV. These preliminary results suggest that a thermionic emission process governs the hole transport through the arsenic segregated interface, and that the height of the barrier set up by the segregated arsenic is on the order of 100meV.

EMITTER RESISTANCE

Majority carrier transport was characterized with a novel Kelvin resistor structure where the high sheet resistance of the thin polysilicon layer was shunted by the top-layer metal (Fig. 3). At the contact, the potential drop between the metal and the silicon substrate is probed. This contact resistance structure permits a much more accurate extraction of the emitter series resistance than the conventional Gummel plot analysis at high bias. The contribution of the

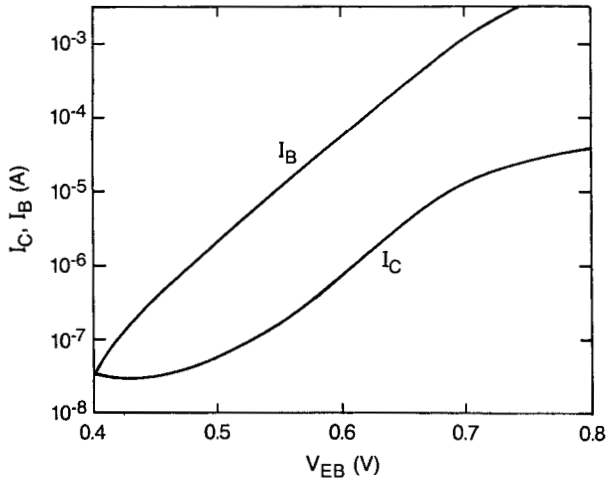

Fig. 2 I-V characteristics of a pnp test transistor.

metal-to-polysilicon contact resistance was obtained with a similar structure.

The emitter resistance was correlated with the base current of npn bipolar transistors with the same pre-implanted emitters. Since base recombination is negligible in these devices, the ideal component of the base current is a direct measure of the emitter saturation current density J_{oe}. Large devices were used in order to minimize the perimeter component of J_{oe}. The data was normalized to 300°K to eliminate the exponential temperature dependence of J_{oe}.

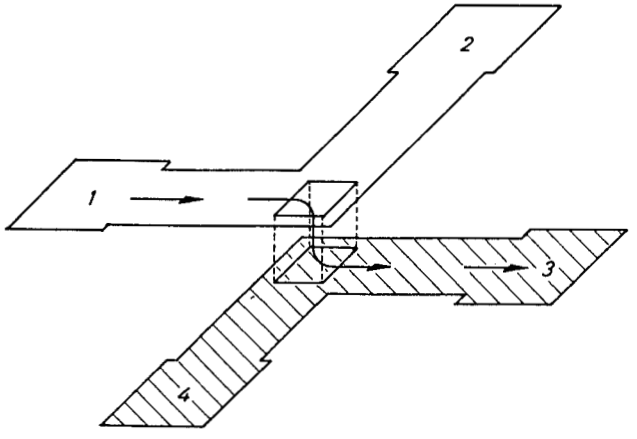

Fig. 3 Kelvin resistor structure. Current direction is shown by arrows; voltage is probed normal to current flow. For R_e measurements, the shaded region is the n^+ emitter, and the top layer is polysilicon covered by metal. For the measurement of $R_{metal-poly}$, the bottom layer is polysilicon and the top layer is metal.

Fabrication

The effect of two surface treatments prior to the polysilicon deposition were investigated. After an RCA clean, most of the wafers received an HF dip etch to minimize the interfacial oxide and some others were chemically oxidized in a solution of ammonium hydroxide. Various anneal cycles were performed and the polysilicon doping level was varied in the range of interest for VLSI transistors. Sputtered titanium/aluminum-silicon contacted the devices to reduce the metal to polysilicon component of R_e.

Experimental Results

For both chemical oxide and native oxide interfaces, the transport of electrons displays a non-ohmic behavior when the anneal temperature is 900°C (Fig. 4). As the anneal temperature is

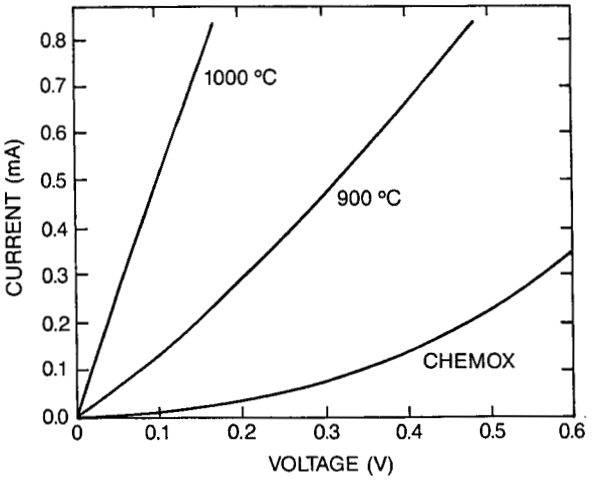

Fig. 4 I-V characteristics of contacts chemical oxide interface and native oxide interface for a 1.75x1.75 μm^2 contact.

increased to 1000°C, the integrity of the interfacial native oxide is destroyed, epitaxial realignment occurs [7], and the electron transport becomes ohmic. The specific contact resistivity at low current densities of these emitters is obtained by measuring R_e for Kelvin structures with different areas (Fig. 5). The metal to polysilicon component does not dominate as it varies from $1x10^{-6}$ $\Omega.cm^2$ at 900°C to $2x10^{-7}$ $\Omega.cm^2$ for a 1000°C anneal. Figure 6 summarizes the J_{oe} and R_e results. The ideal region of operation on that figure is the lower left-hand corner. The chemical oxide devices are located at the upper left of the figure: their J_{oe} are the lowest, but the emitter resistance is very large. Native oxide devices are located on the bottom right of the figure: R_e is improved but J_{oe} has increased. Higher polysilicon doping levels and higher anneal temperatures decrease R_e but increase J_{oe}. For high speed transistors, the desirable region of operation is at the lower right of the figure but for applications

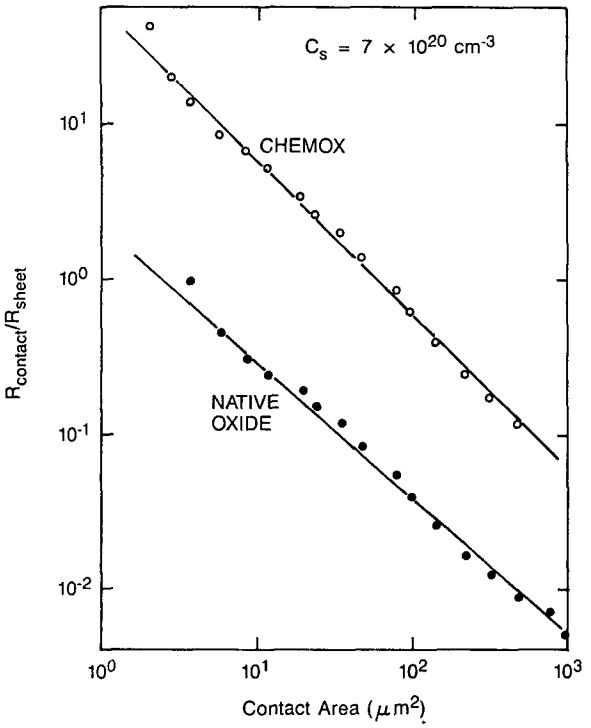

Fig. 5. Normalized emitter resistance vs contact area. The emitter specific contact resistivity drops from $8x10^{-5}$ $\Omega.cm^2$ for a chemical oxide interface to $3x10^{-6}$ $\Omega.cm^2$ for a native oxide interface (900°C anneal).

such as solar cells, a low J_{oe} is highly desirable and the increase in emitter resistance is not of critical concern.

CONCLUSIONS

By measuring the minority hole current tansport across the polysilicon/silicon interface with a pnp test transistor we have demonstrated that arsenic segregation at the interface has a much more pronounced effect on transport than the interfacial native oxide present. The transport mechanism for holes appears to be dominated by a thermionic emission process over a potential barrier created by the arsenic. The majority carrier current is also affected by the interface which is responsible for a large emitter series resistance. This resistance can be traded off for an increase in based current by modifying the anneal conditions.

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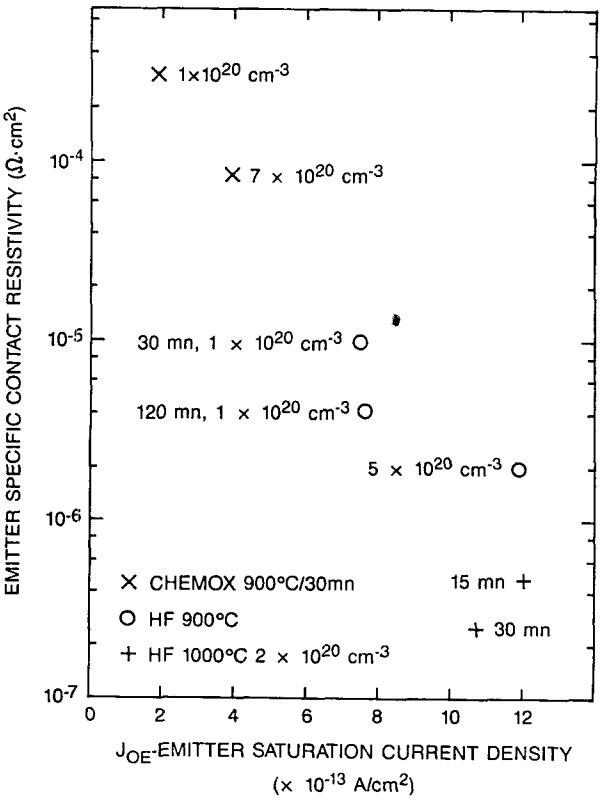

Fig. 6 Emitter specific contact resistivity vs emitter saturation current density for 2 interface treatments and various anneal cycles.

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