Extended Abstracts of the 18th (1986 International) Conference on Solid State Devices and Materials, Tokyo, 1986, pp. 283-286

Forward-Bias Tunnelling Current Limits in Scaled Bipolar Devices

J. del Alamo
NTT Labs., Atsugi, Kanagawa, Japan 243-01

R. M. Swanson
Stanford University, Stanford, CA 94305, U.S.A.

Tunnelling assisted by midgap states in forward bias is observed in bipolar transistors containing heavily doped p-n junctions. A simple phenomenological model suitable to incorporation in device codes is developed. The model identifies as key parameters the space-charge-region thickness at zero bias and the reduced doping level at the SCR edges. Both parameters can be obtained from C-V characteristics. This tunnelling mechanism may limit the maximum gain achievable from scaled bipolar devices.

Introduction

The scaling of silicon bipolar transistors demands a reduction in the base thickness and an accompanying increase in the base doping level. A number of peculiar physical phenomena have been shown to arise from the high base impurity concentrations. Some of them are beneficial, like bandgap narrowing in the base which yields an improvement in the gain [1], but most of them are harmful. Such are the reduction of breakdown voltage and the appearance of Zener tunnelling at reverse bias [2].

In this paper we study a potentially more deleterious mechanism: forward-bias tunnelling in the base-emitter junction. If both sides of a p-n junction are heavily doped, a thin space-charge-region (SCR) results that may allow the tunnelling of electrons across it. If both sides of the junction are degenerate, the Esaki effect is observed and a region of negative resistance appears in the forward I-V characteristics. Without such high doping levels, i.e., when one or neither of the two sides are degenerate, tunnelling may also occur assisted by states located inside the gap [3].

Tunnelling currents of this nature have been recently observed at the periphery of self-aligned poly-silicon bipolar transistors across the junction formed by the emitter and the heavily-doped extrinsic-base contact [4,5]. Adequate spacer technology has been able to supress this perimeter tunnelling. As device scaling advances and the intrinsic base doping level is raised, tunnelling is expected to occur at the whole emitter-base area. This tunnelling current may pose a limitation to the maximum gain achievable from scaled bipolar devices.

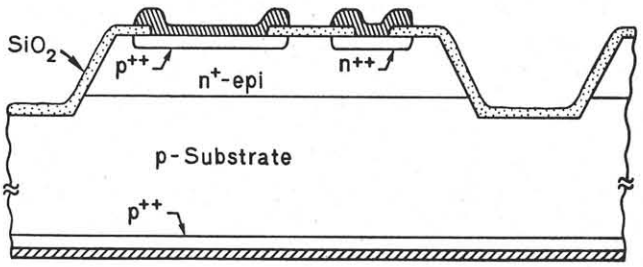

Fig. 1 Cross section of bipolar transistor.

Experimental

The transistors (Fig. 1) used in the present work were designed to measure the hole transport parameters in heavily-doped n-type silicon [6]. The base was fabricated by epitaxy and is therefore uniformily doped with phosphorus to a value that can be measured very precisely [7]. B was then implanted through an oxide mask to a dose of 9×10^{15} cm^{-2}. Contact to the base was provided through n^+ regions outdiffused from P-doped glass. Metal contact to the device was realized with evaporated Al.

The I-V and C-V characteristics of the top p^{++}-n^+ diode were measured in forward bias at 297 K. Forward I-V curves of selected devices are shown in Fig. 2, with the base doping level used as label. At low voltages a strong increase in the current occurs as the base doping level is raised beyond about 5×10^{18} cm^{-3}. This "excess current" is approximatelly exponential and can then be fitted with an equation of the form:

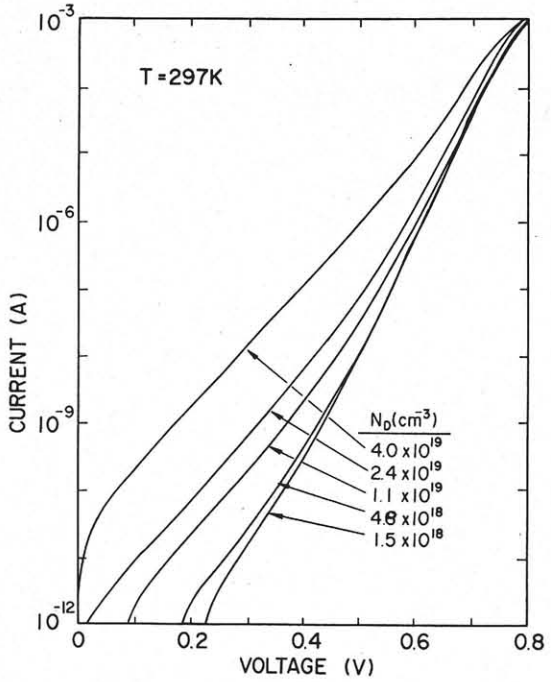

Fig. 2 I-V characteristics of the p^{++}-n^{+} junction of selected devices

$$I_T = A\, J_{OT}\, exp\, \frac{V}{V_T} \qquad (1)$$

Since I_T is postulated to be of a tunnelling nature, J_{oT} is denoted as the tunnelling saturation current and V_T is the tunnelling characteristic voltage. A is the device area. J_{oT} and V_T were extracted from the measured data.

The space-charge-region width and the reduced doping level $N_aN_d/(N_a+N_d)$ at the SCR edge can be obtained from the C-V characteristics for small forward bias. N_a and N_d denote the net acceptor and donor concentrations at the edges of the SCR. The results of all measurements are collected in Table I.

N_D (cm^{-3})	J_{oT} (A/cm^2)	V_T (mV)	$W_{SCR}(0)$ (A)	$N_aN_d/(N_a+N_d)$ (cm^{-3})
8.8×10^{17}	9.1×10^{-12}	26	620	3.0×10^{17}
1.5×10^{18}	1.1×10^{-11}	32	470	5.9×10^{17}
4.8×10^{18}	1.3×10^{-10}	39	360	9.3×10^{17}
1.1×10^{19}	2.5×10^{-9}	45	340	9.7×10^{17}
1.4×10^{19}	5.7×10^{-9}	47	300	1.4×10^{18}
1.8×10^{19}	1.0×10^{-8}	46	310	1.1×10^{18}
2.4×10^{19}	9.8×10^{-9}	46	310	1.2×10^{18}
4.0×10^{19}	2.2×10^{-7}	46	300	1.1×10^{18}

Table I

Theory

Tunnelling assisted by midgap states across a forward-biased p-n junction was postulated in order to explain the "excess current" that appeared in Esaki diodes at higher voltages than required to uncouple the conduction and valence bands [3]. This excess current can exist even if one or neither of the two sides of the junction are degenerate, as our experiments show. The basic process is shown in Fig. 3. If a localized state inside the forbidden gap is energetically aligned with an occupied state of the conduction band of the n-side of the junction, an electron can tunnel into the localized state and later recombine with a valence band hole of the p region through a Shockley-Read-Hall process. This requires that the SCR be sufficiently thin to achieve an appreciable tunnelling probability.

The establishment of a rigorous theory that accuratelly describes this tunnelling phenomenon presents considerable challenges. Even in simple tunnelling processes, order of magnitude agreement between experiments and theory is at best what can be expected [8]. With this background, our intention in the present work is to demonstrate the tunnelling nature of the excess currents displayed in Fig. 2 by developing a simplified theory that contains the most relevant physics in a non-rigorous way. A model results that is suitable for incorporation into device codes.

For the purpose of grasping the fundamental physics it is sufficient to consider the tunnelling probability through a potential barrier of height E_T and thickness W [9]:

$$T \approx exp\,(-\frac{2W}{\hbar}\sqrt{2m^*E_T}) \qquad (2)$$

For a triangular or parabolic barrier additional numerical factors in the argument of the exponential appear [10], but identical dependences of T on W and $\sqrt{E_T}$ are found.

There are several difficulties in extending this simple quantum mechanical theory to tunnelling assisted by midgap states. Among them, the electron in the localized state cannot be described by a free-space wave function corrected by the

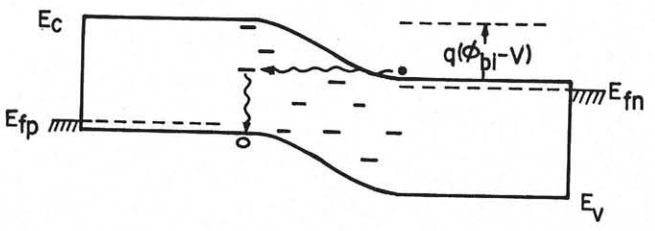

Fig. 3 Illustration of basic tunnelling process assisted by midgap states.

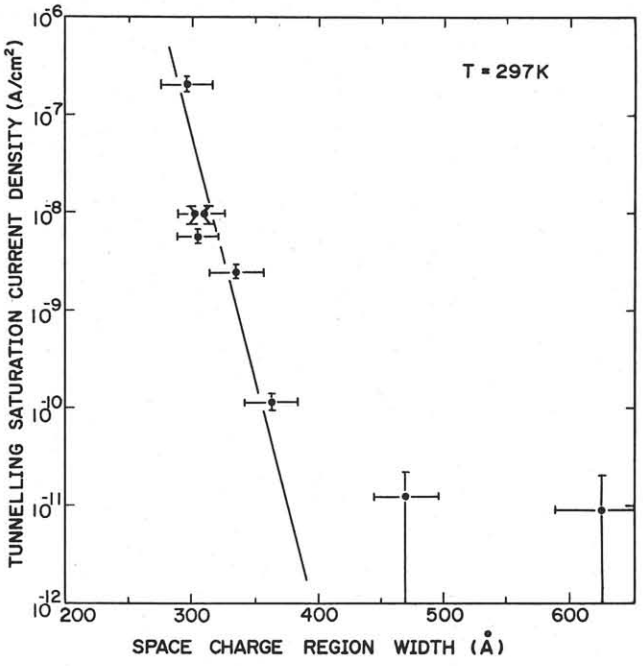

Fig. 4 J_{oT} versus $W_{SCR}(0)$.

effective mass of the host crystal, as assumed in the derivation of (2). The effective mass, m^*, of eq. 2 takes therefore an unclear meaning. Eq. 2 should be regarded as a functional dependence relationship with unknown constants.

The height of the barrier to tunnelling, as shown in Fig. 3, is by definition of junction built-in voltage:

$$E_T = q\,(\Phi_{bi} - V) \tag{3}$$

The thickness of the tunnelling barrier is approximatelly, for an abrupt junction:

$$W_{SCR}(V) = \sqrt{\frac{2\varepsilon_s}{q}\,\frac{N_a + N_d}{N_a\,N_d}\,(\Phi_{bi} - V)} \tag{4}$$

For other junctions, the voltage dependence of W_{SCR} may have a different functional form. However, for small forward voltages, $W_{SCR}(V)$ is not very sensitive to V and (4) suffices.

Introducing (3) and (4) into (2), we obtain:

$$T \approx exp\left[-\frac{2}{\hbar}\sqrt{2m^* q\,\Phi_{bi}}\,W_{SCR}(0)\right]$$

$$exp\left[\frac{4\sqrt{m^*\varepsilon_s}}{\hbar}\sqrt{\frac{N_a + N_d}{N_a\,N_d}}\,V\right] \tag{5}$$

and the tunnelling probability exponentially increases with the forward voltage. The observation of such a dependence in the experimental current indicates that the midgap state distribution is either exponential or uniform in energy. The first alternative is expected if band tailing of the conduction and valence band edges occurs due to heavy doping [11]. Tails are expected to extend very deep into the forbidden gap in the SCR because of the lack of mobile carriers that screen the dopant impurities in neutral regions [12].

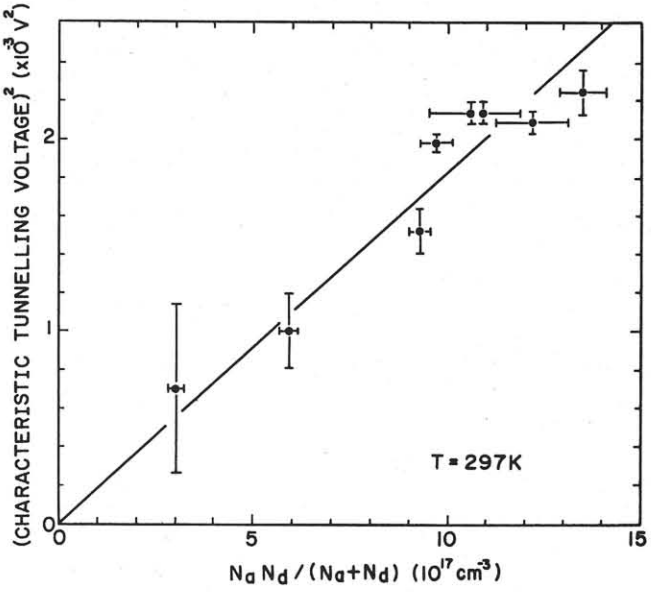

Fig. 5 V_T^2 versus reduced doping level.

Eq. 5 implies that the tunnelling current may be approximatelly described by an equation like (1) with J_{oT} depending exponentially on the junction width at zero bias $W_{SCR}(0)$ ($\Phi_{bi}^{1/2}$ is a rather insensitive function of doping):

$$J_{OT} \simeq k_1\,exp\,[-k_2\,W(0)] \tag{6}$$

and V_T depending linearly on the square root of the reduced doping level:

$$V_T = k_3\sqrt{\frac{N_a\,N_d}{N_a + N_d}} \tag{7}$$

The dependences contained in eqs. 6 and 7 are verified in our experiments. In fact, Fig. 4 displayes J_{oT} versus $W_{SCR}(0)$ and indeed an exponential dependence is shown to appear when $W_{SCR}(0)$ is smaller than about 400 Å. Fig. 5 plots the square of V_T against the reduced doping level. The data fits a straight line that crosses the origin, as expected from eq. 7. The values of the constants that appear in eqs. 6 and 7 can be extracted: $k1=6.02\times10^{7}$ A/cm^2, $k2=1.15\times10^{7}$ cm^{-1}, and $k3=4.28\times10^{-11}$ V.cm$^{3/2}$.

The temperature dependence of the currents

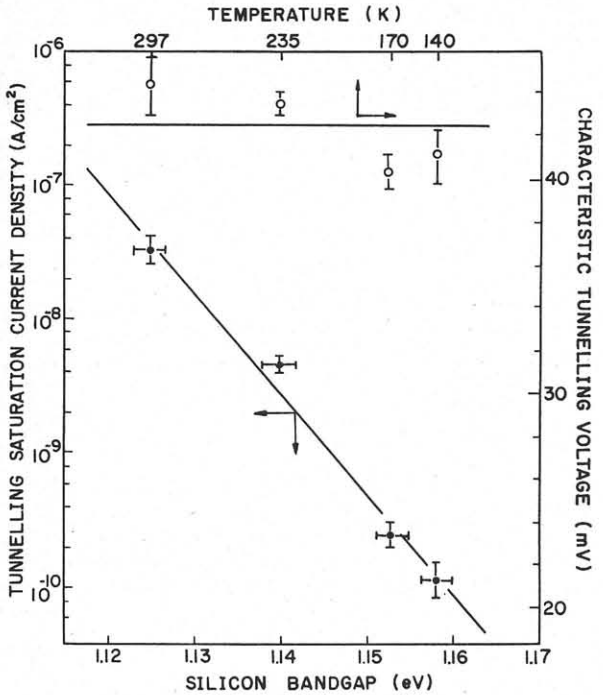

Fig. 6 Temperature dependence of J_{oT} and V_T for a typical device.

under consideration has also been studied. The model summarized in eqs. 1, 6 and 7 predicts that J_{oT} depends exponentially, with a minus sign, on the bandgap (through ϕ_{bi}), and that V_T is essentially independent of T. In fact, Fig. 6 shows measurements for a typical sample. The exponential dependence of J_{oT} on the silicon bandgap unequivocally confirms the tunnelling nature of the current under investigation and rules out its interpretation as a recombination current inside the SCR, since J_{oT} is not thermally activated. Additionally, V_T changes less than 10% when the temperature spans a range of 160 K, confirming the temperature independence predicted by eqn. 5.

Discussion

The model defined by eqs. 1, 6, and 7 can easily be incorporated in device modelling codes. Although the model identifies W_{SCR} and $N_aN_d/(N_a+N_d)$ as the key parameters controlling tunnelling, the constants involved are expected to be somewhat process dependent. For one thing, heavy compensation of the p^{++} emitter occurs in the high doping range yielding gradual junctions. This is understood by observing the dependence of the reduced doping level on the epitaxial donor concentration which is plotted in Fig. 7. Since the slope of the doping distribution at the junction of a real device is expected to be process dependent, the junction potential shape, and the constants in eqs. 3, 6 and 7 will probably be sensitive to the details of the process. Nevertheless, the model defined by eqs. 1, 6, and 7 may be a reasonable starting point for the prediction of tunnelling in practical devices.

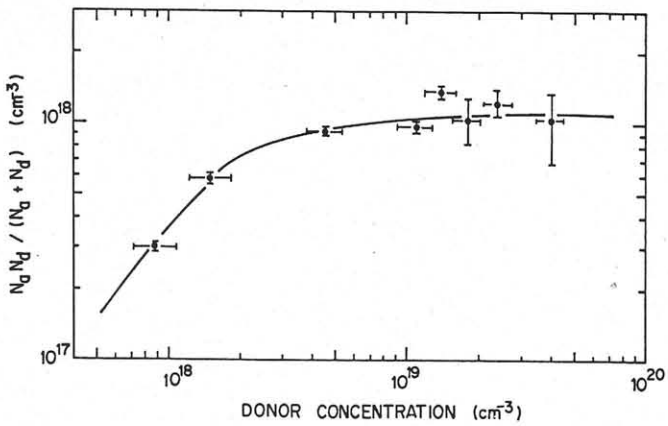

Fig. 7 Reduced doping level versus donor concentration in the base.

The tunnelling current identified in this work may limit the maximum gain achievable in scaled bipolar devices. This limitation may be avoided by fabricating the devices by techniques, like MBE, that allow the preparation of a dopant-free SCR [13]. A trade-off between the maximum tolerable tunnelling current and the intrinsic delay in electron transport across the SCR will exist. Our data indicates that a 400 Å SCR yields negligible tunnelling through it, but this may be too wide for high-speed devices.

Conclusions

Tunnelling assisted by midgap states has been shown to occur in forward-biased p-n junctions. A simple model suitable for incorporation in device codes has been developed. This tunnelling mechanism may limit the gain in scaled bipolar transistors.

References

1. T. H. Ning, 16th Conf. on Solid State Devices and Materials, Kobe 1984, p. 205.
2. J. M. C. Stork and R. D. Isaac, IEEE Trans. Electr. Dev. ED-30, 1527 (1983).
3. A. G. Chynoweth, W. L. Feldmann, and R. A. Logan, Phys. Rev. 121, 684 (1961).
4. A. Cuthbertson and P. Ashburn, IEEE Trans. Electr. Dev. ED-32, 242 (1985).
5. E. Hackbarth, G. P. Li, and T. C. Chen, 44th Device Research Conf., Boston 1986.
6. J. del Alamo, S. Swirhun, and R. M. Swanson, Int. Electron Device Meeting, Washington D. C. 1985, p. 290.
7. J. del Alamo and R. M. Swanson, J. Electrochem. Soc. 132, 3011 (1985).
8. C. B. Duke, "Tunneling in Solids", Academic Press 1969.
9. K. Seeger, "Semiconductor Physics", Springer-Verlag 1982 (2nd edition).
10. P. N. Butcher, K. F. Hulme, and J. R. Morgan, Solid-St. Electr. 5, 358 (1962).
11. E. O. Kane, Solid-St. Electr. 28, 3 (1985).
12. J. R. Lowney, Solid-St. Electr. 28, 187 (1985).
13. P. M. Solomon, Proc. IEEE 70, 489 (1982).