Impact of Nanotopography on STI CMP in Future Technologies

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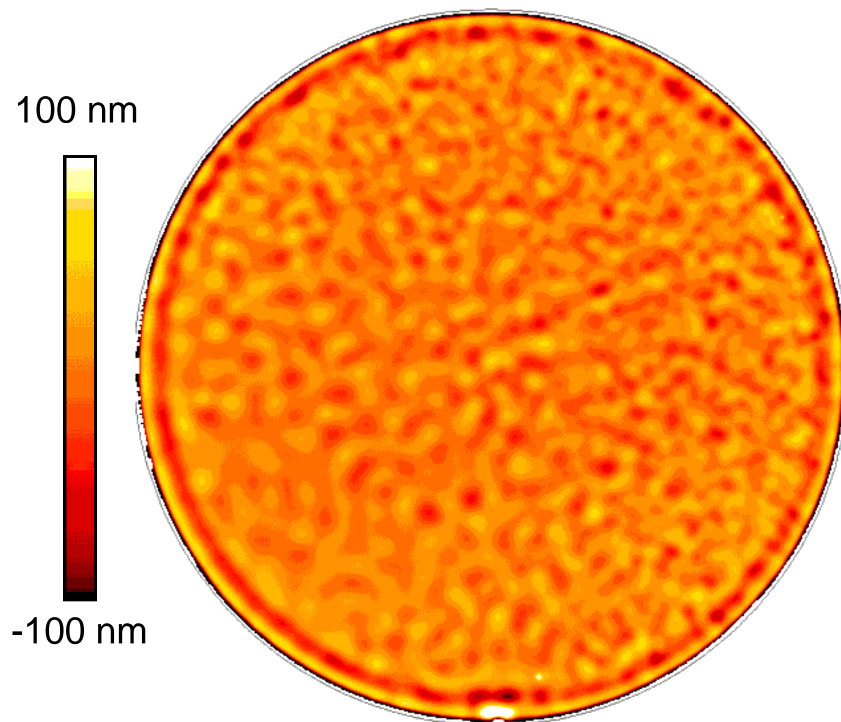
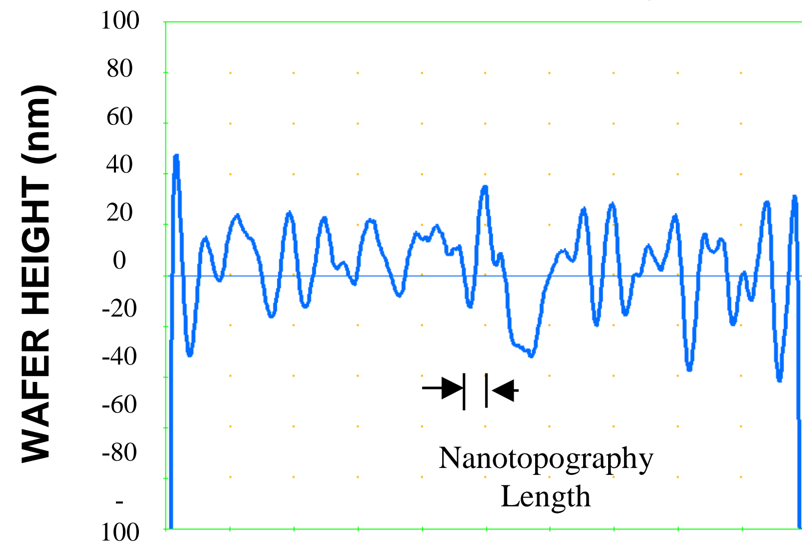
Outline

- Review: Nanotopography Interaction with CMP
  - Experiments demonstrate oxide thinning over nanotopography
- What impact does nanotopography have on STI as we scale from 130 nm to 100 nm and beyond?
- Approach:
  - Simulate CMP of STI stacks over nanotopography
  - Yield Problem #1: failure to clear oxide
  - Yield Problem #2: excessive nitride thinning
- Conclusions:
  - Nanotopography requirements can be based on STI yield impact
  - Can generate yield problem maps given a measured nanotopography map

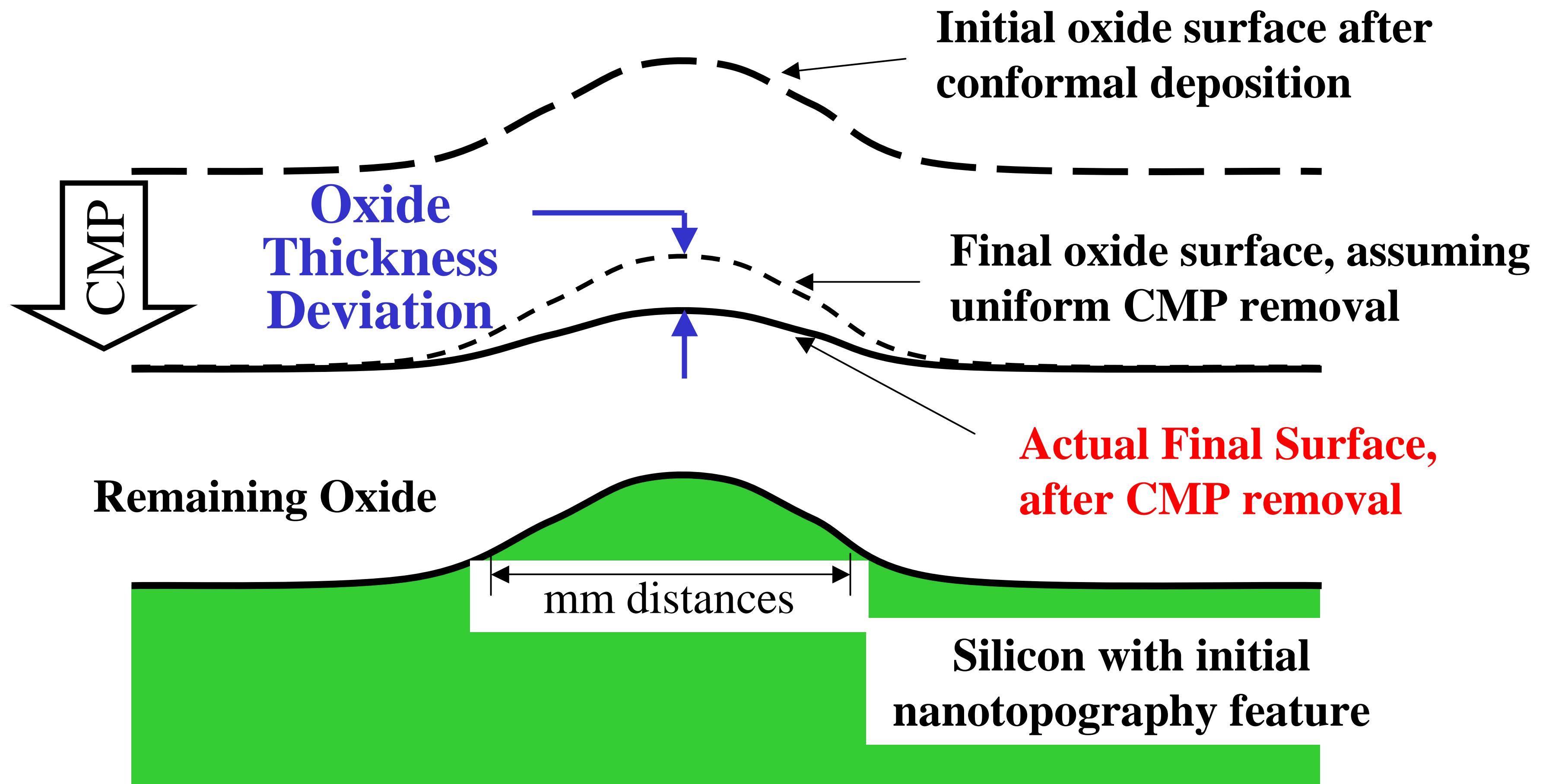
Review: Nanotopography

- Nanometer height variations occurring on millimeter lateral length scales in virgin silicon wafers

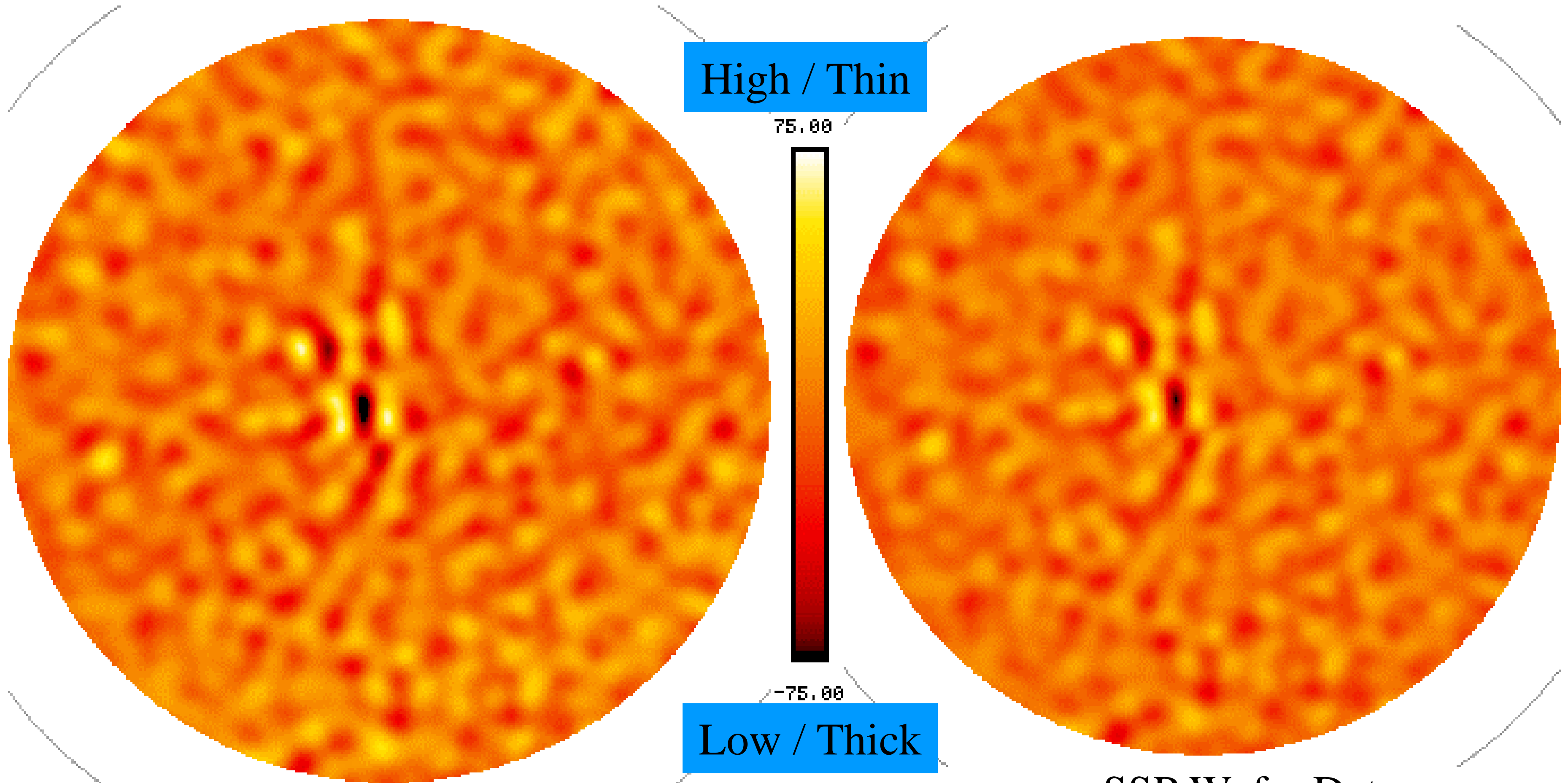




Problem: Oxide Thickness Deviation (or Oxide Thinning) During CMP

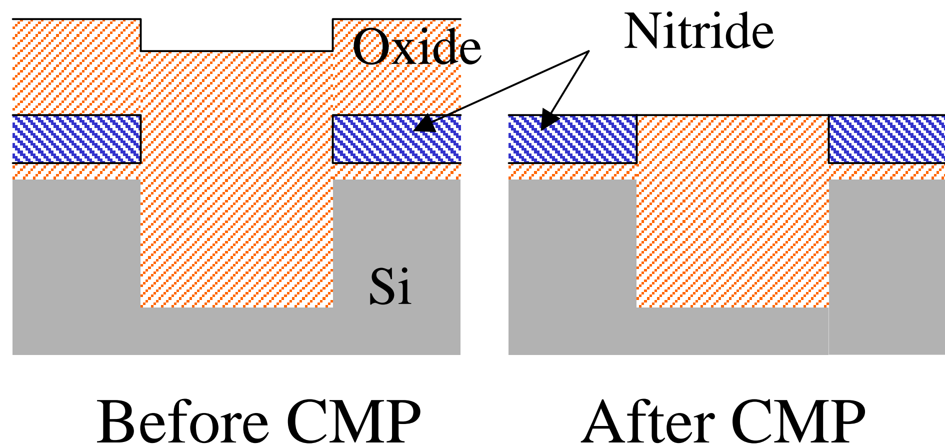


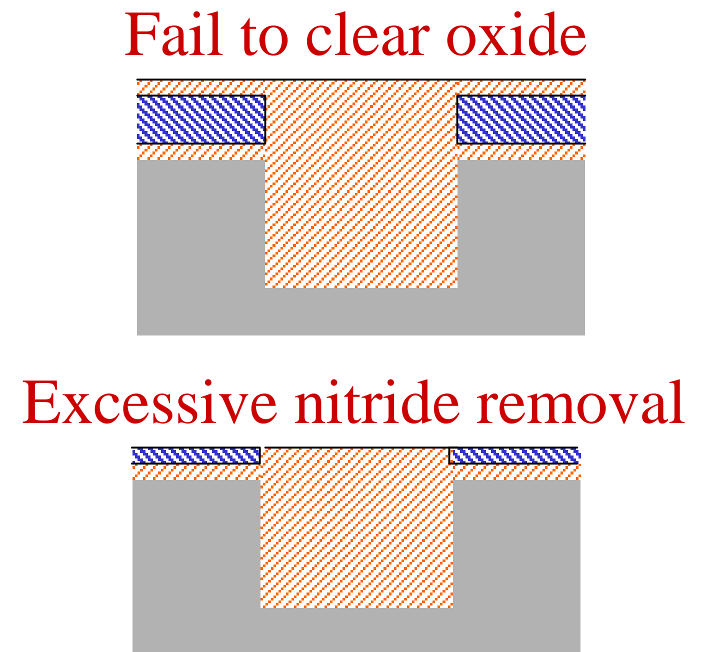
Nanotopography & Oxide Thinning



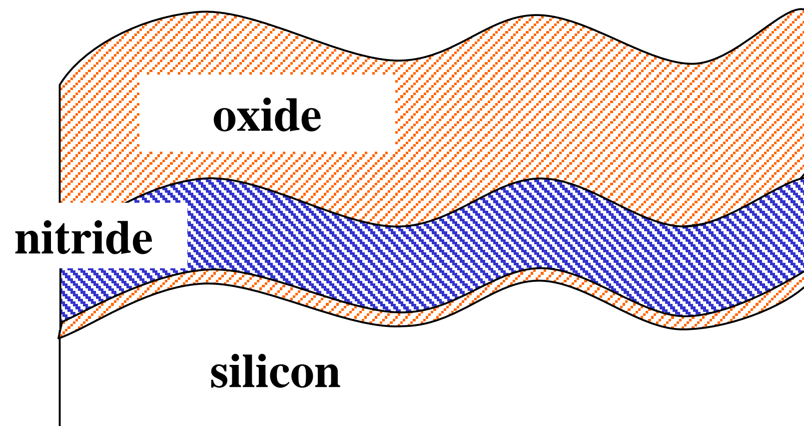
Impact of Nanotopography in STI CMP?

- Previous experiments on blanket oxide over nanotopography show oxide thinning in CMP
- But… STI processes involve CMP of a multilayer oxide/nitride/oxide stack



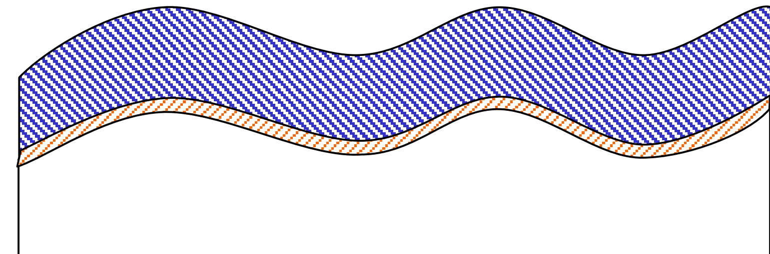


Approach: Simulate Effect of Nanotopography on CMP of STI Stack



STI stack over nanotopography: **pre-CMP**

"Ideal" result:
- Complete removal of oxide
- No removal of nitride



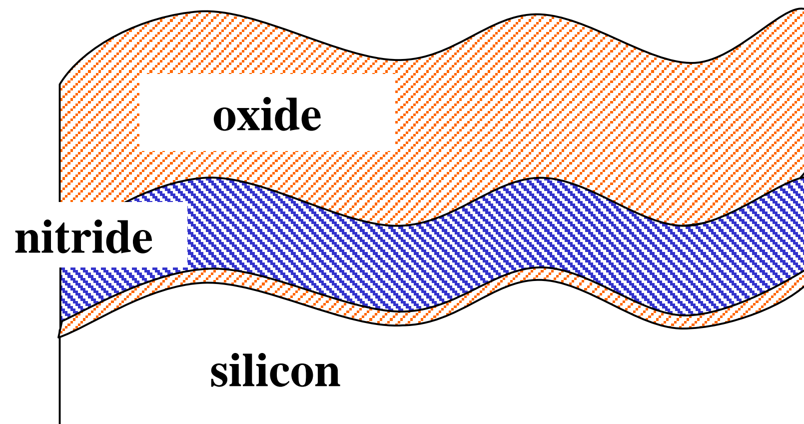
STI stack over nanotopography: **post-CMP**

Simulation Details

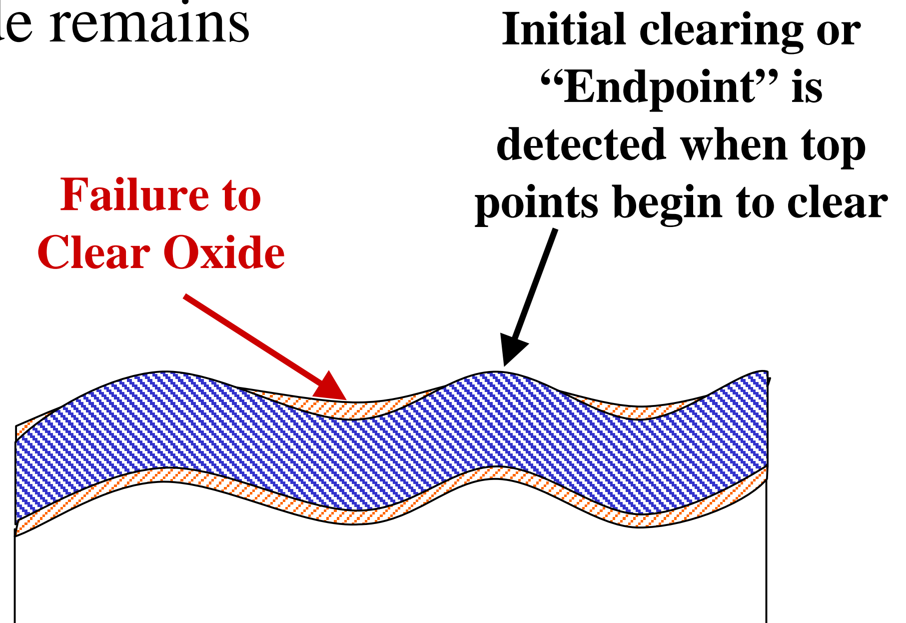
- Start with measured nanotopography data
  - Epi single-side polished substrate; use 20 mm EE
- Simulate CMP of STI stack on blanket wafer
  - Perform 3D contact wear simulation – find local pressures based on bending of elastic pad around surface
  - Consider 130 nm technology node:
    - 300 nm oxide / 100 nm nitride / 10 nm pad oxide
  - CMP process:
    - Nominal pad stiffness: E = 147 MPa
    - 5:1 oxide:nitride polish rate selectivity
- Consider Two Cases:
  - Problem #1: Failure to clear
  - Problem #2: Excessive nitride polish

Problem #1: Failure to Clear Oxide

- Polish time is determined by initial clearing (initial endpoint) plus overpolish time
  - Polish to initial clear: 84 seconds for this wafer/stack
  - Assume fixed overpolish time: 14 seconds
- Examine regions where oxide remains
  - These result in device failure



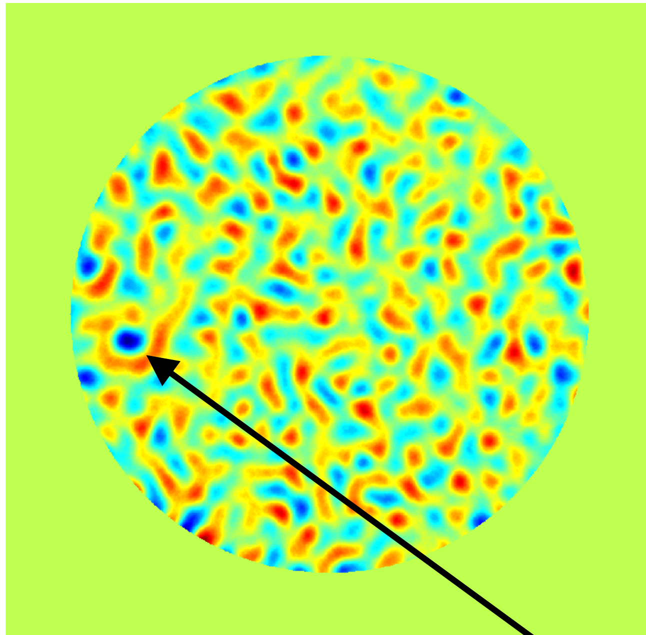
STI stack: pre-CMP

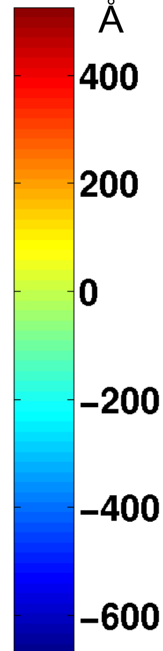


Post-CMP with too little overpolish

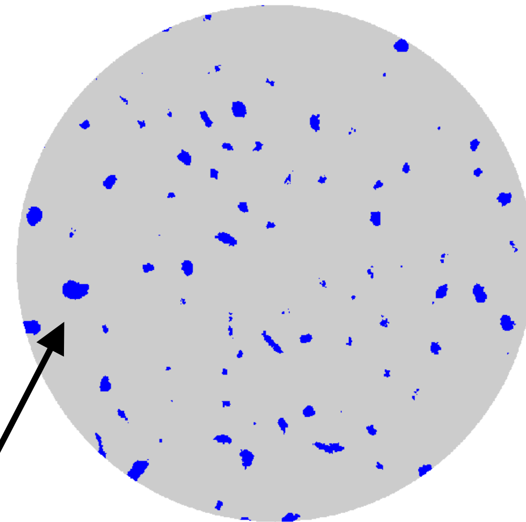
Simulated Result: Oxide Clearing Map

Initial Nanotopography





3% of wafer does not clear



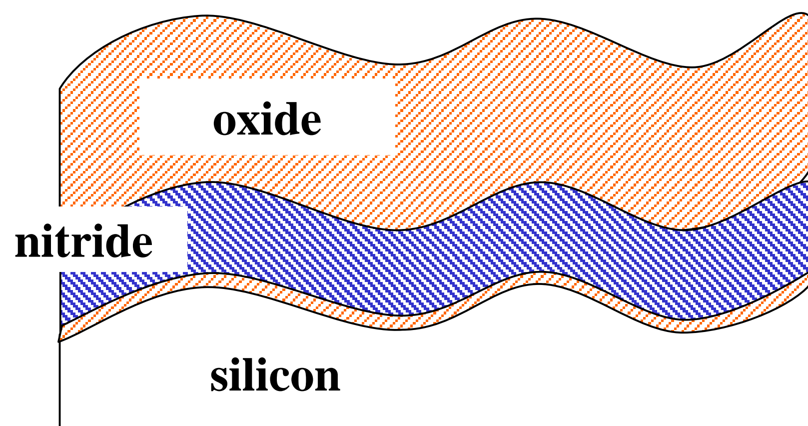
Blue indicates uncleared areas

Initial Nanotopography

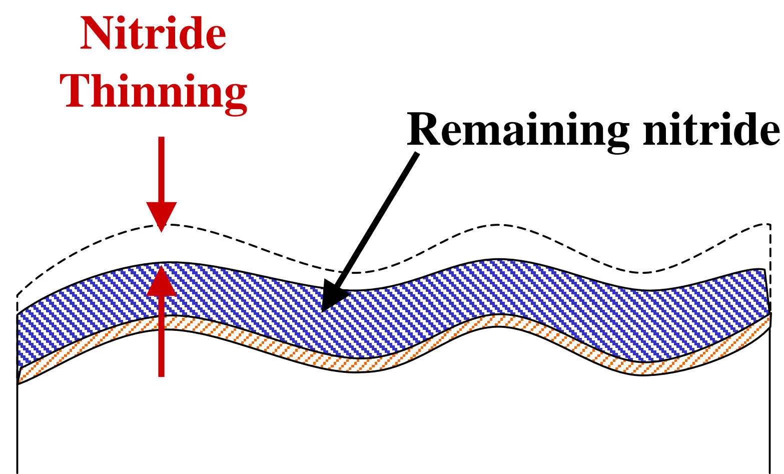
Note visual correlation with initial nanotopography “low spots”

Problem #2: Excessive Nitride Loss

- Failure to clear - causes incomplete transistor formation
  - Alternative: Increase overpolish time to ensure complete clearing of oxide in all nanotopography valleys everywhere on wafer
- Nanotopography thus forces *additional* overpolish time!
  - In addition to overpolish due to wafer level or chip pattern effects
- Resulting problem: excessive nitride loss - causes transistor performance degradation



STI stack: pre-CMP



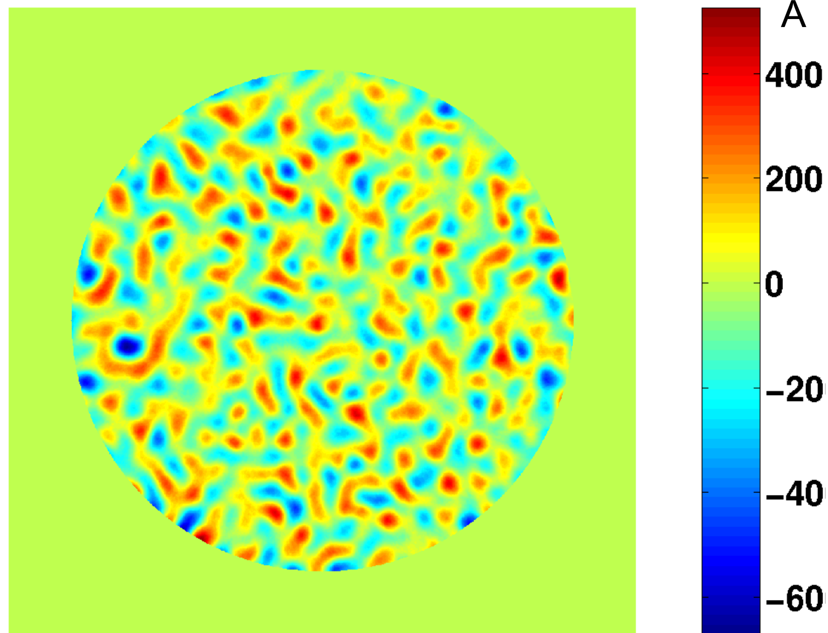
STI stack: post-CMP

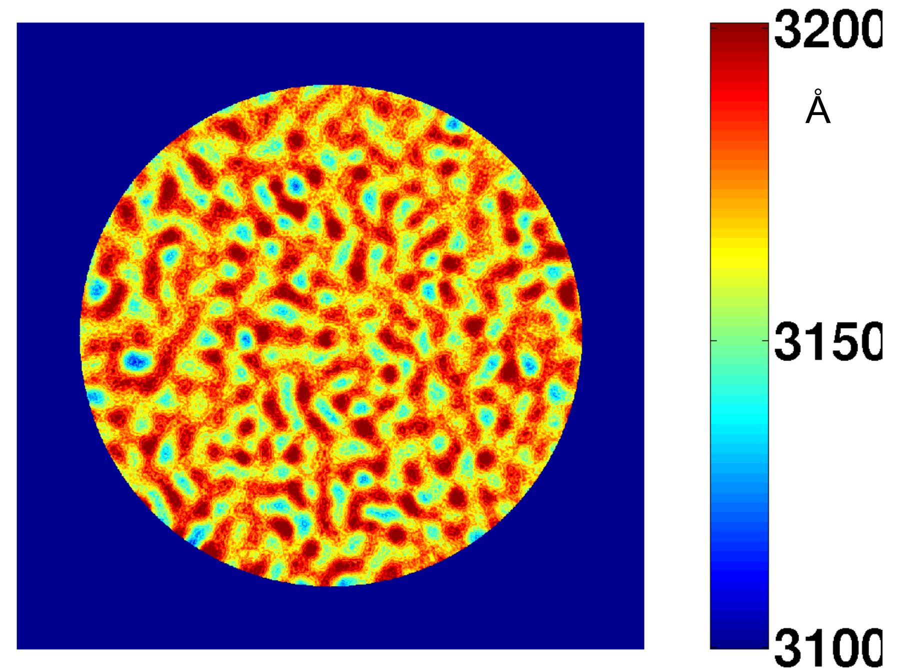
Simulation Details

- Extend CMP over-polish time until oxide has just finished clearing everywhere
- Plots:
  - Initial nanotopography
  - Total amount removed (oxide and nitride)
  - Nitride thinning
  - Potential device failure points
    - Assume a 20% nitride film thickness loss budget

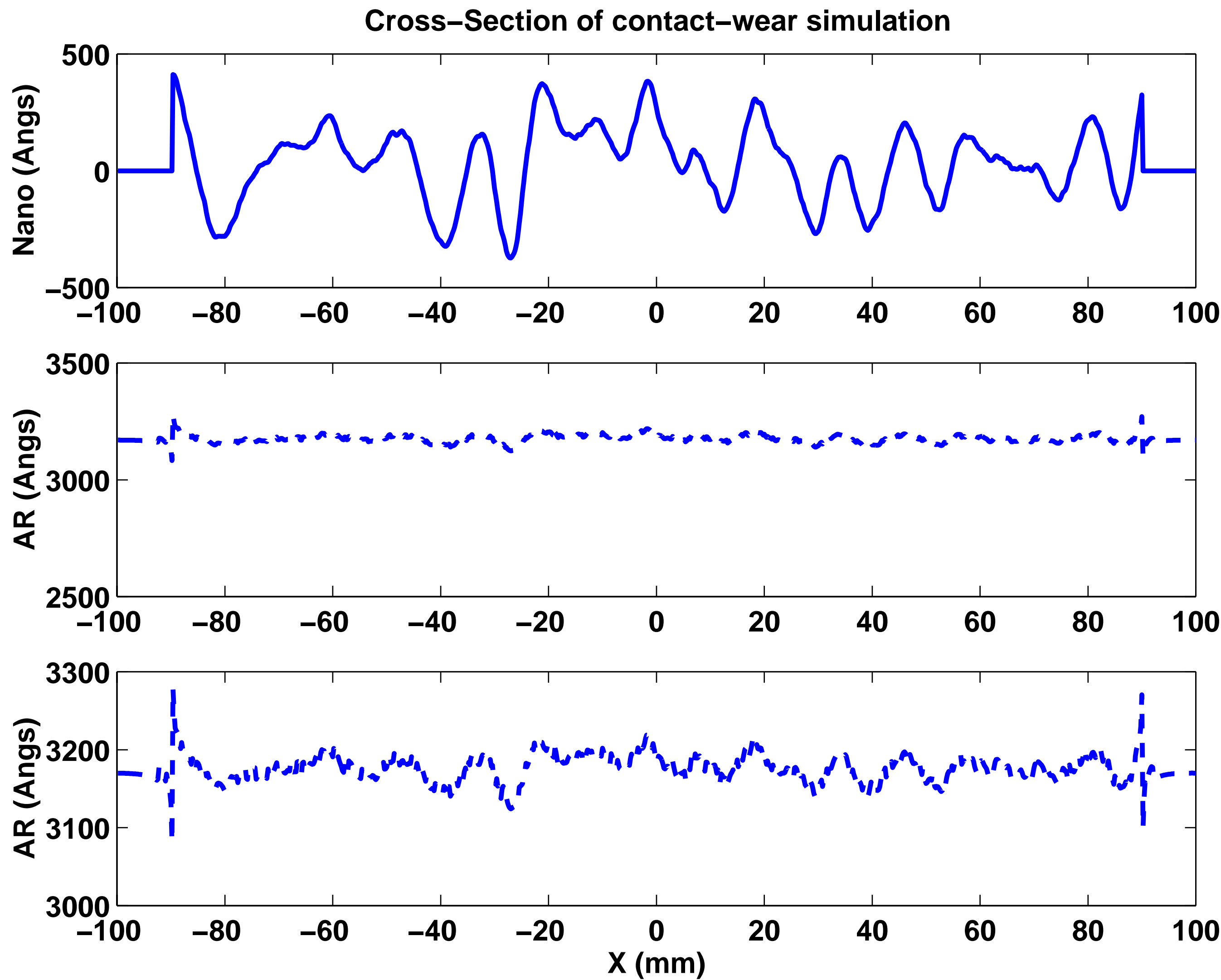
Initial Nanotopography

Total Amount Removed





E= 147 MPa



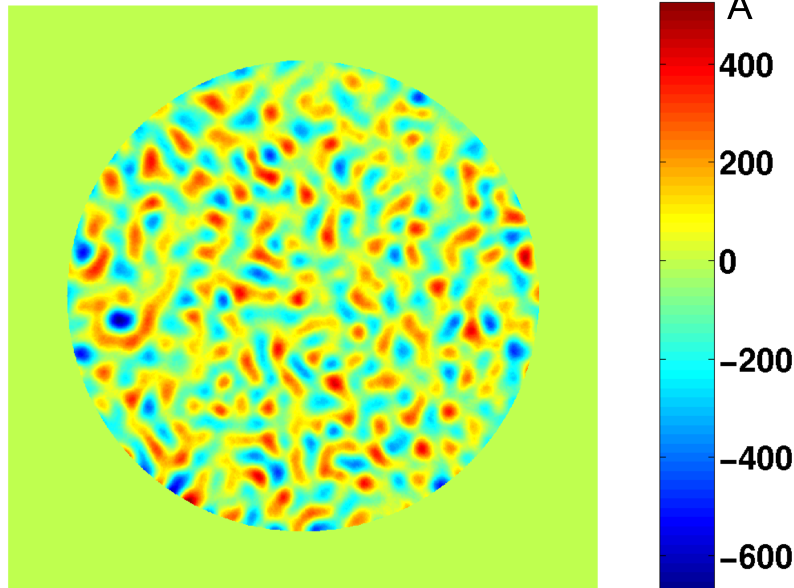
Initial Nanotopography

Total Removed

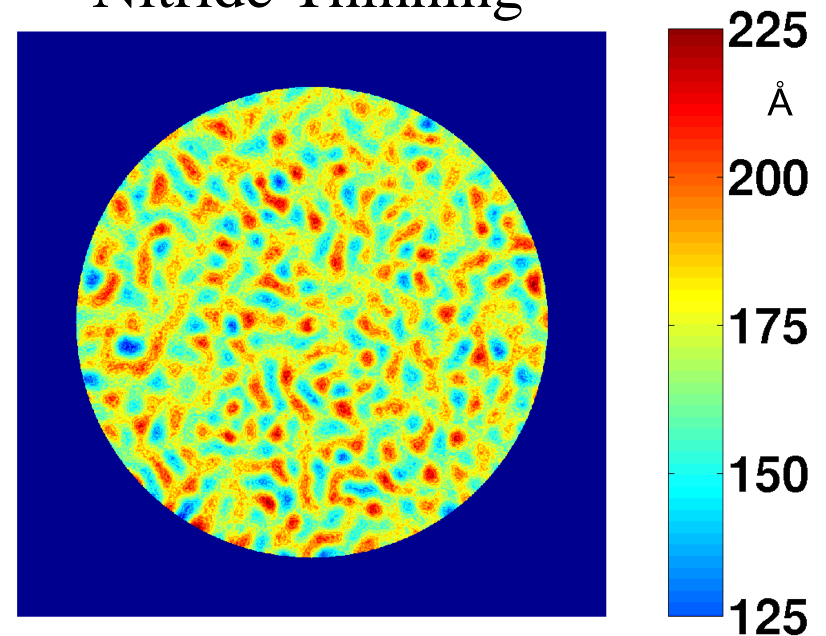
Zoom on Total Removed

Thinning of Nitride Layer (Under Oxide)

Initial Nanotopography



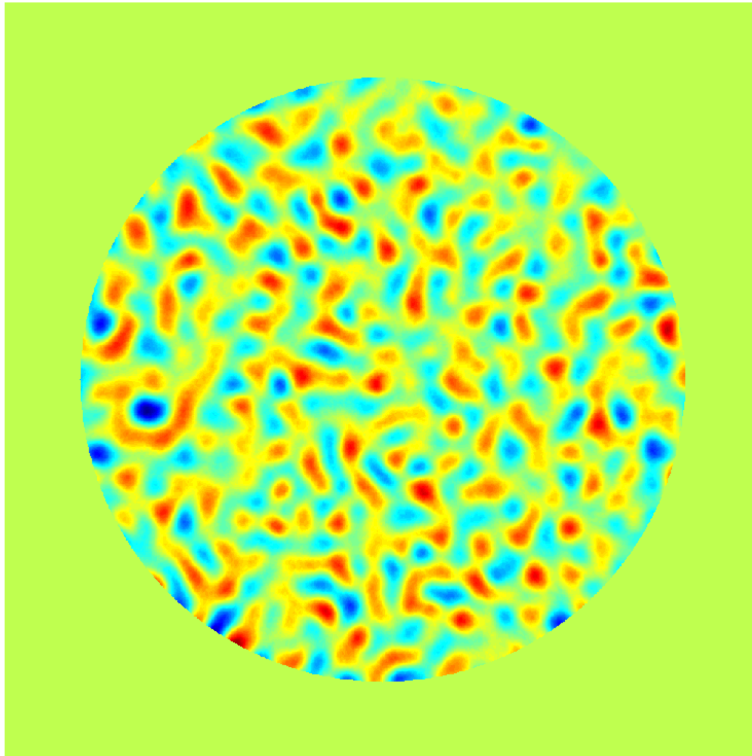
Nitride Thinning

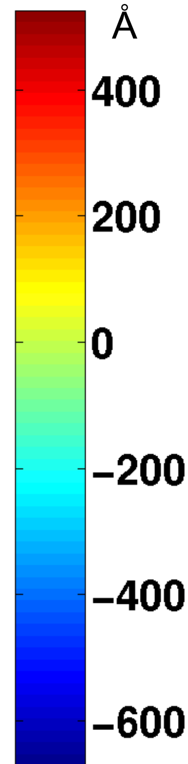


E= 147 MPa

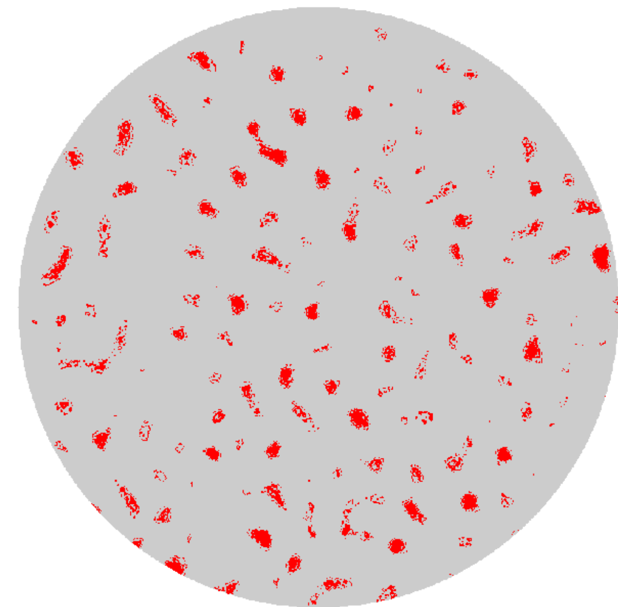
Nitride Thinning – Device Failure Map

Initial Nanotopography





Potential Failure Locations



4.5% Area Failure

E= 147 MPa

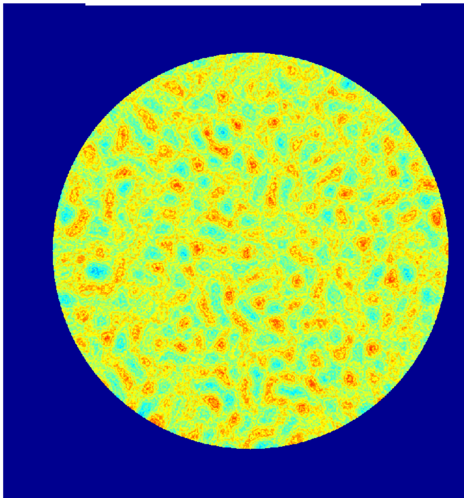
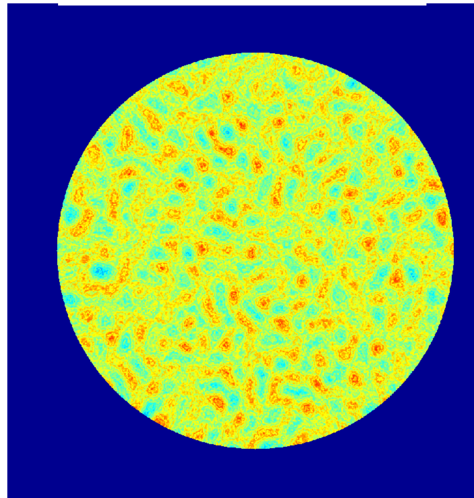
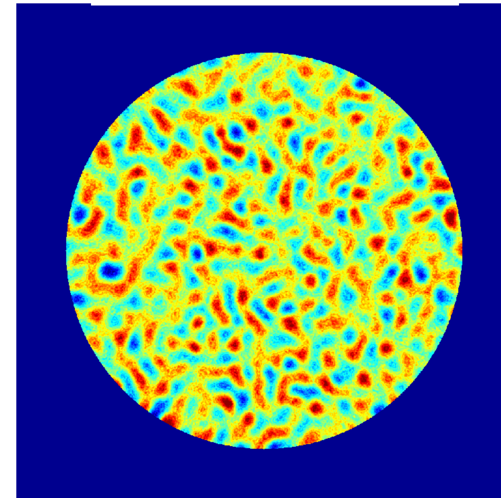
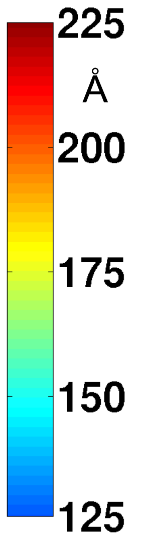
Red indicates excessive nitride thinning – greater than 20 nm (10%) budget

Effects of Pad Stiffness

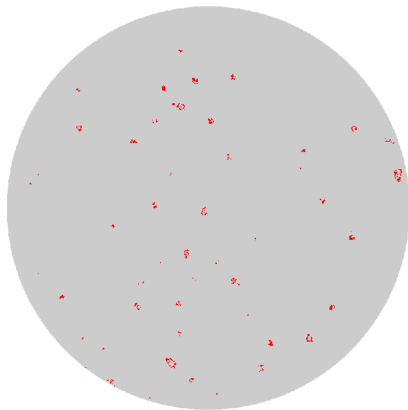
- The pad stiffness may affect the amount of nitride thinning
  - Stiffer pads result in more thinning in certain regions on the wafer
  - Less stiff pads result in less thinning
- Trend in STI CMP is toward stiffer pads in order to reduce within-die variation due to pattern densities
  - This trend may conflict with nanotopography!

Comparison: Nitride Thinning & Failure Areas

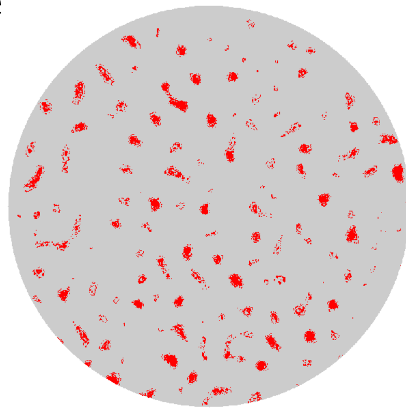
Soft Pad	Medium Pad	Stiff Pad
$E = 70$ MPa	$E = 147$ MPa	$E = 200$ MPa

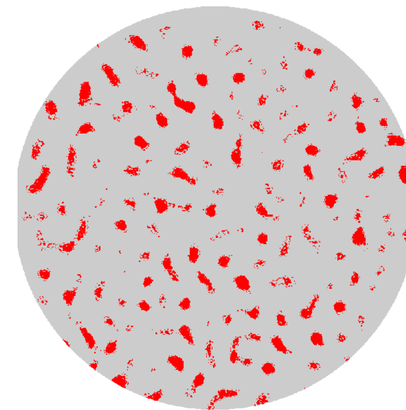
Failure Areas



0.4%



4.5%

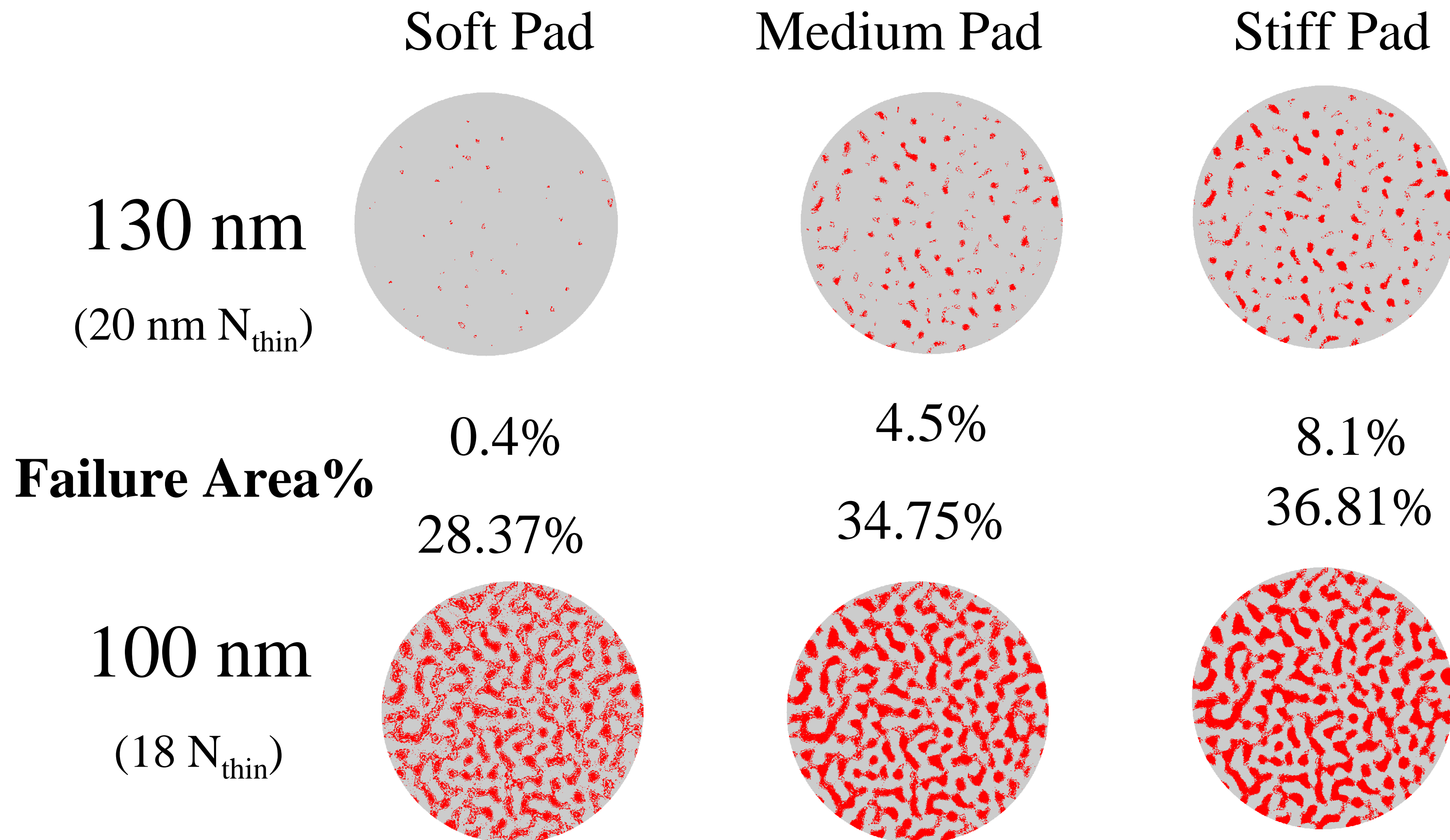


8.1%

Future Generations

- As technology scales, film thicknesses will also decrease
- Nitride thinning budget for STI processes will also decrease
- Examine 130 nm to 100 nm transition
- Conservative Scaling Assumption:
  - nitride film thickness shrinks to 90 nm (from 100 nm)
  - thinning budget of 20% or 18 nm (from 20 nm)

Excessive Nitride Thinning – Device Failure Comparison



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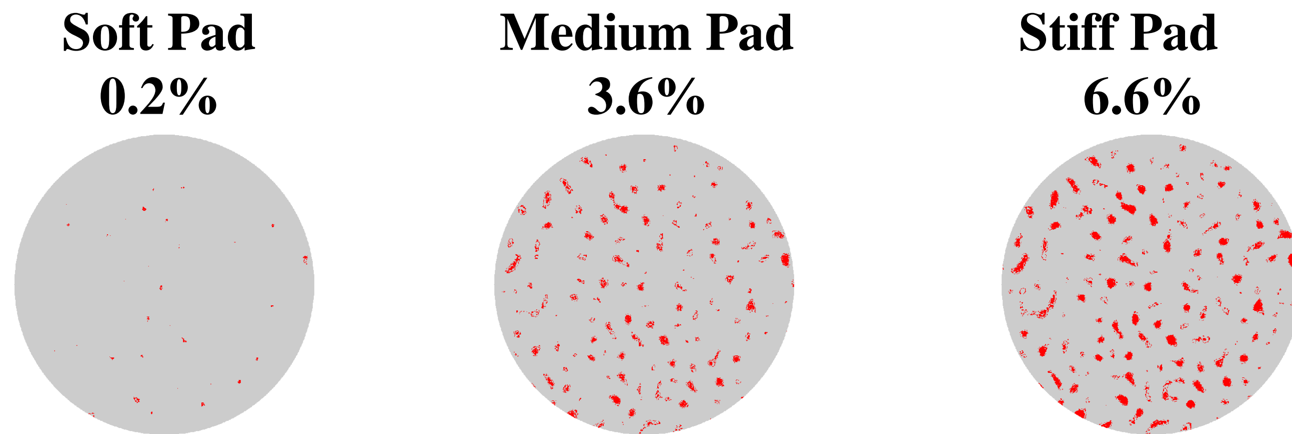
Modified Nanotopography Requirement

- Given nitride thinning spec (18 nm), how much must we scale nanotopography to achieve same % failure area?
  - Example: Scale nanotopography by 90%, adjust polish time



- Conjecture for future nanotopography requirements:
  - Need to scale nanotopography height at same rate as nitride thickness
  - May need to improve nanotopography height or spatial characteristics more aggressively if STI CMP moves to stiffer pads

Conclusions

- Nanotopography can interact with CMP to cause device yield concerns in the STI process
- Yield concerns can be predicted and yield impact maps produced from nanotopography maps:
  - Problem #1: failure to clear oxide
  - Problem #2: excessive nitride thinning
- Degree of impact depends on pad stiffness
- Future technology scaling will require
  - Continued tightening of nanotopography specs
  - Full wafer measurement and analysis of nanotopography
- Future work: STI stack simulation on patterned wafers with nanotopography

References

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