Variation Issues in On-Chip Optical Clock Distribution

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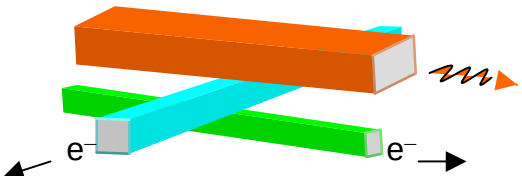
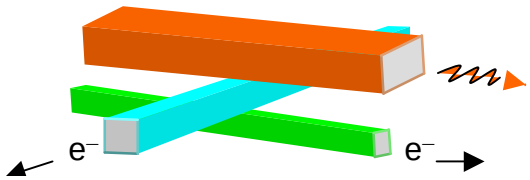
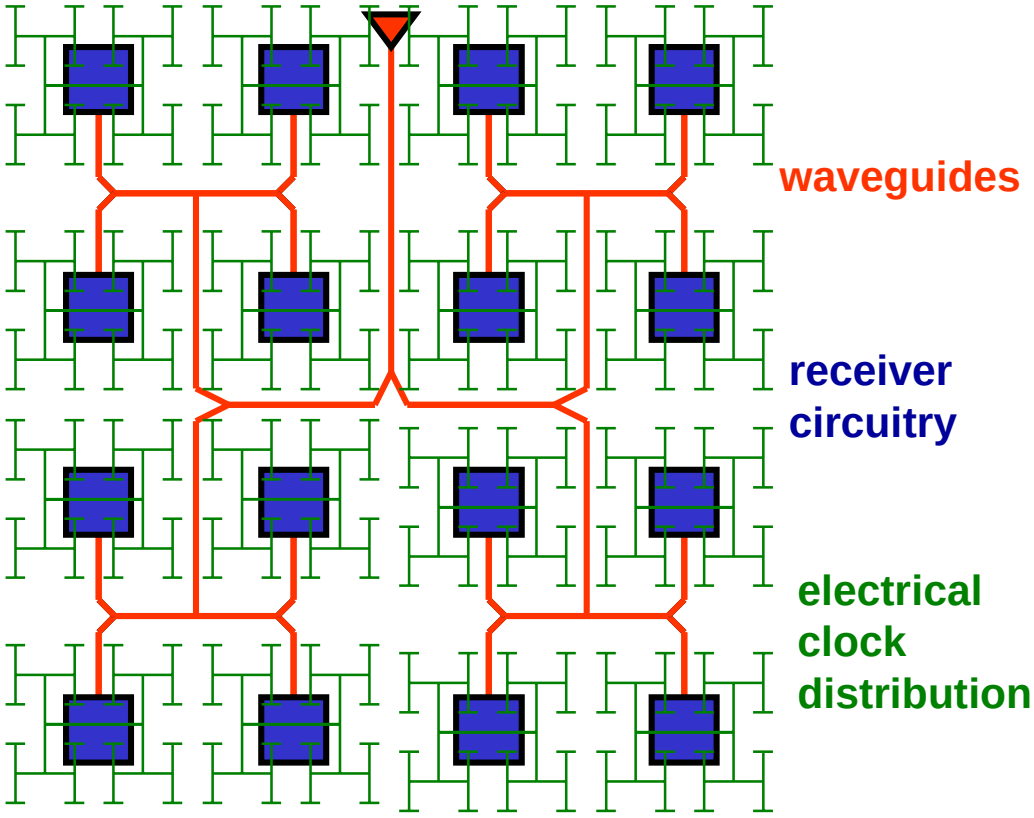
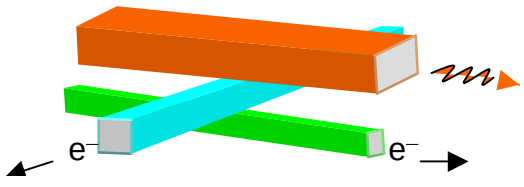


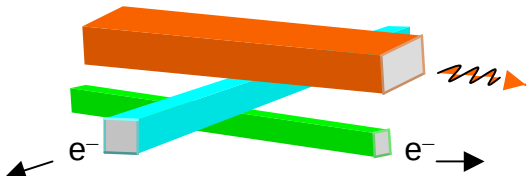


Opportunity: Optical Clock Distribution

- Approach:
  - off-chip optical source
  - distribute by waveguides
  - optoelectronic conversion: detector and receiver circuit
  - local electrical clock network
- Potential Advantages:
  - low skew distribution: *high speed clocking*
  - low noise
  - power reduction
- Variation Concern:
  - how will variation introduce skew and limit optical clocks?

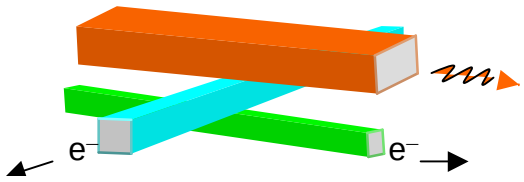


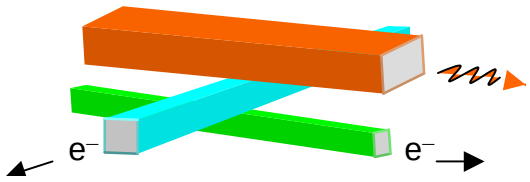




Outline: Variation Issues in Optical Clock Distribution

- Motivation
- Variation Sources
- Baseline Optoelectronic Receiver Design
- Variation Analysis Approach
- Variation Analysis Results
- Summary and Future Work

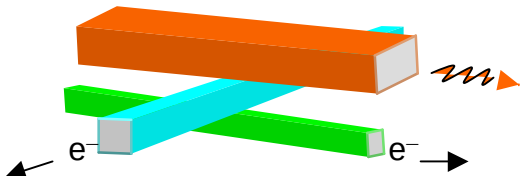


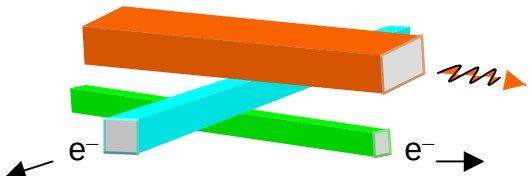


Variation Sources in Optical/Electronic System

- Concerns:
  - what variation is expected in the system?
  - how will this variation introduce skew and thus limit the achievable on-chip optical clock distribution speeds?

- Potential Sources of Variation:
  - external optical source:
    - jitter, power variations (neglect in this study)
  - waveguides:
    - geometric variation introducing optical arrival skew
  - opto-electronic receiver -- key focus of this study
    - detector
    - device/interconnect
    - operating conditions (e.g. power supply, temperature)
  - local electrical clock distribution (neglect in this study)

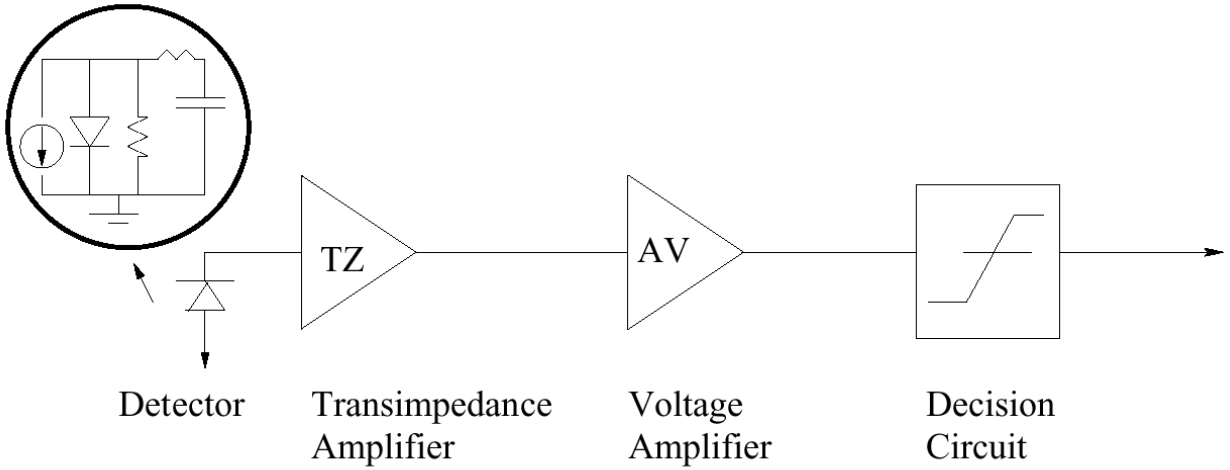




Approach: Baseline Receiver Design and Analysis

- Baseline optical receiver circuit design
  - enable variation/design trade-off analysis

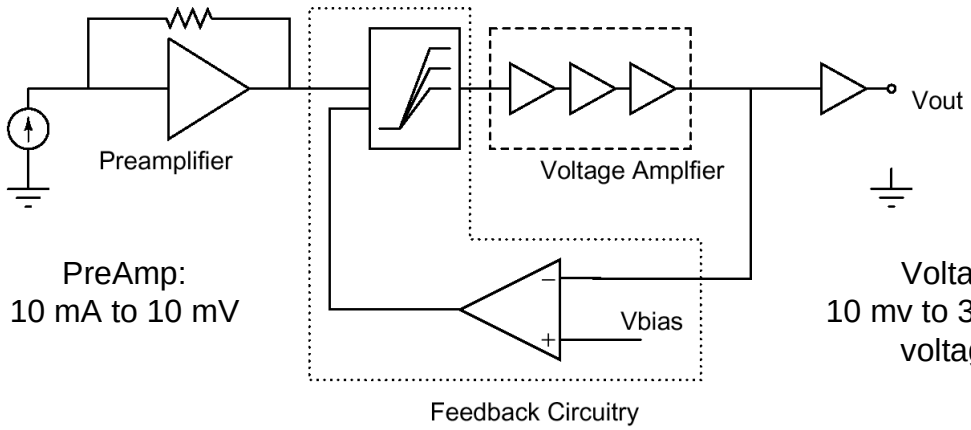
Photodiode model: current source w/ diode cap. and res.



- Test chip fabrication
  - validate working design

Baseline Receiver Circuit Design

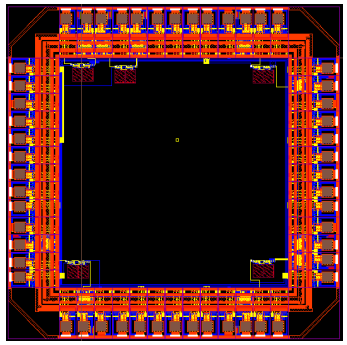
- Approach: CMOS Transimpedance Amplifier and Voltage Amplification

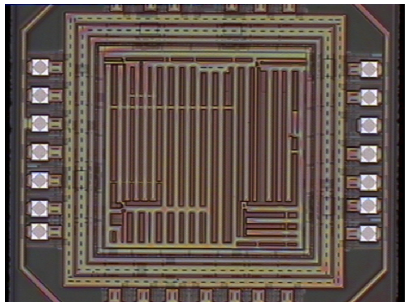


- Constraints/Design Goals
  - 1 GHz bandwidth (in 0.35 μm CMOS)
  - standard CMOS without analog extensions
  - power dissipation in mW range -- enable dense on-chip optical interconnects

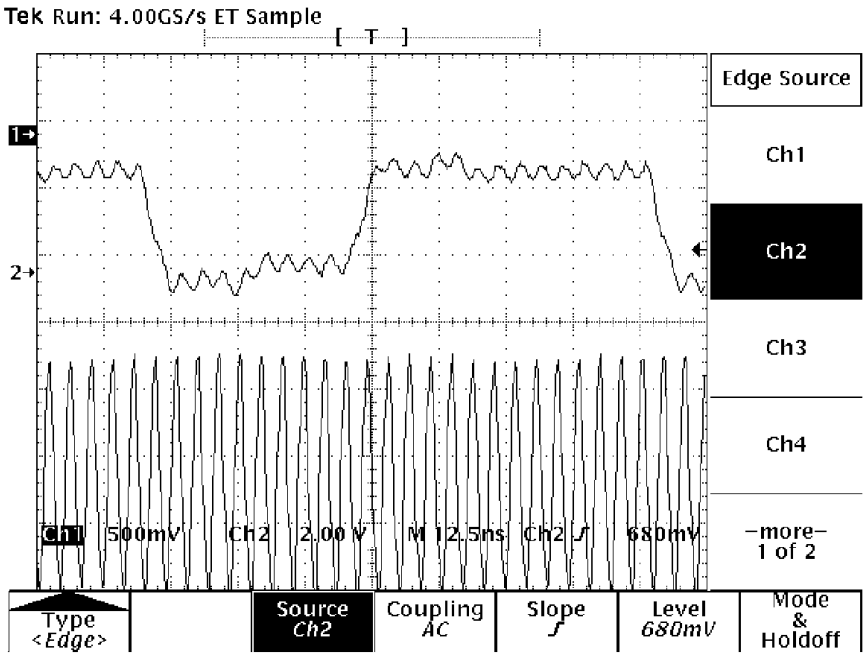
Test Chip Fabrication

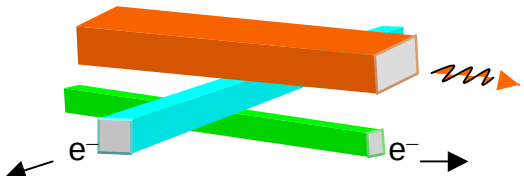
- Test chip fabrication:
  - 0.35 μm MOSIS
  - validate working design
  - simple Si diode detector
  - 4 receivers at corners and one at center edge of 2mm x 2mm chip

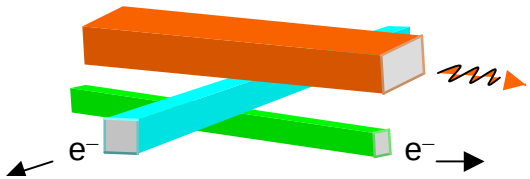




- Results
  - circuit found to function correctly
  - limitations in received optical power through narrow top metal slits: redesign needed

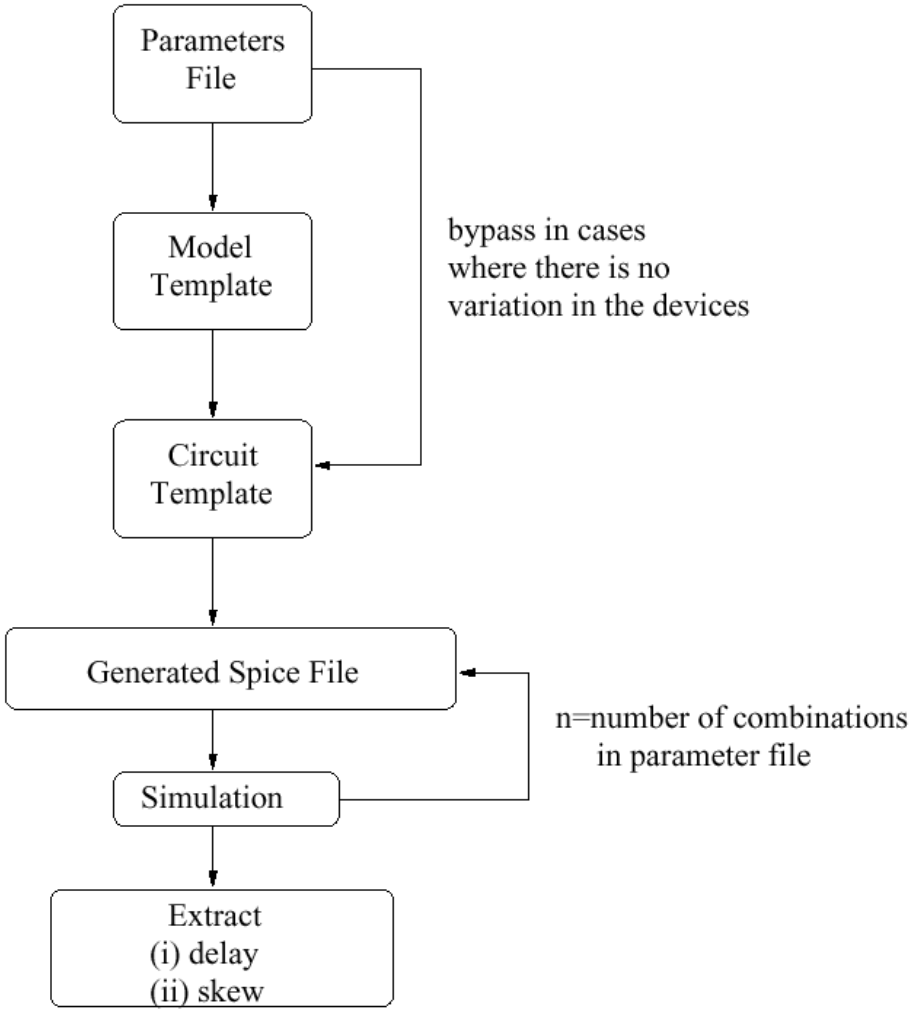






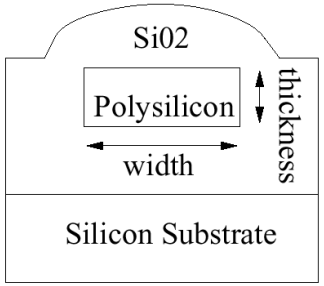
Variation Analysis Approach

- Use Spice models for the circuit
- Approach:
  - consider each variation source (detector, systematic device geometry, environmental)
  - circuit simulation to extract delay and skew
  - evaluate sensitivity of delay/skew to variation source



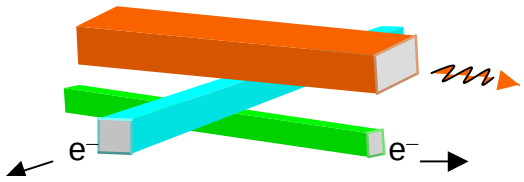
Variation Analysis Results (I)

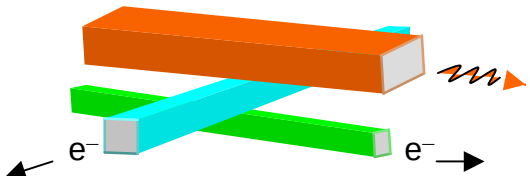
- Waveguide variation:
  - 10% geometry variation
  - ➢ 2 ps skew in light arrival time



Input Current	Absolute Skew	Average Power
8 μA	8 ps	60 mW
10 μA	0 (Nominal)	60 mW
12 μA	4 ps	60 mW
89 μA	4 ps	35.5 mW
100 μA	0 (Nominal)	35.5 mW
111 μA	2 ps	35.5 mW
900 μA	22 ps	11.5 mW
1000 μA	0 (Nominal)	11.5 mW
1100 μA	14 ps	11.5 mW

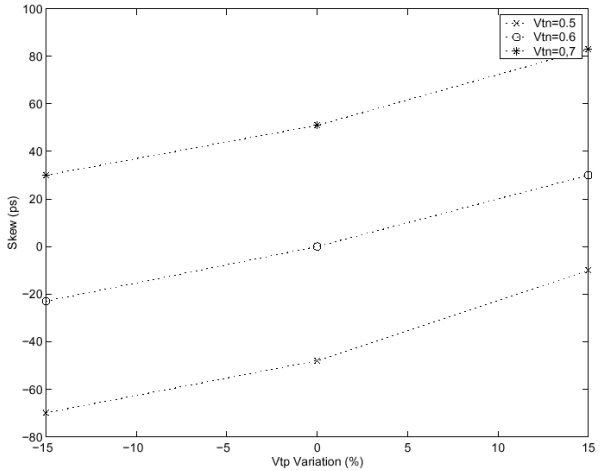
- Detector (output current) variation:
  - received optical power: 10%
  - dark current: ~1μA (constant)
  - ➢ clock skew vs. current tradeoff: at higher current, fewer amplifier stages needed



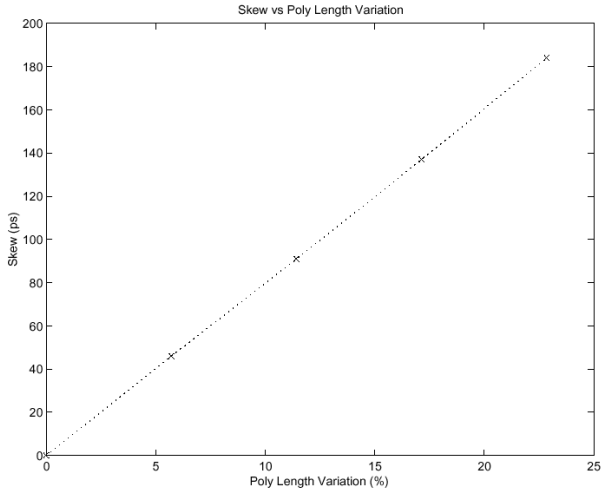


Variation Analysis Results (II)

- Receiver device V_T variation:
  - Assume area dep. variation: $\sigma_{\Delta_{VT}} = \frac{A_{VT}}{\sqrt{WL}}$
  - Matching variation: $V_T = \mu_{VT} \pm \frac{3.09}{\sqrt{2}}\sigma_{\Delta VT}$
  - ➢ skew as function of %V_T variation
  - ➢ ~ +/- 20 ps for 15% V_T variation

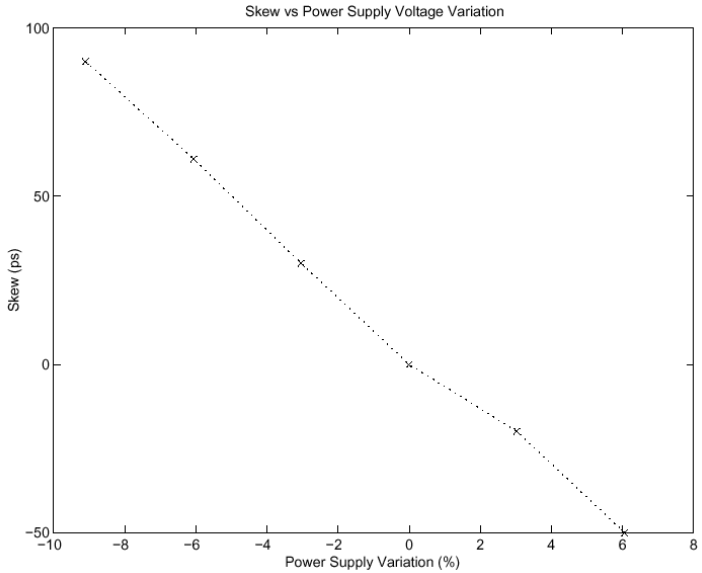


- Receiver device channel length variation:
  - Consider ΔL percent variations
  - ➢ LARGE skew for 10-20% ΔL variation



Variation Analysis Results (III)

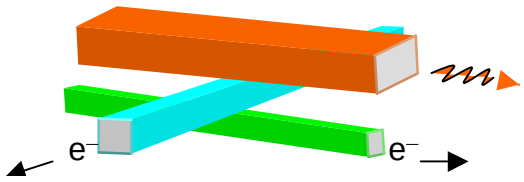
- Receiver power supply variation:
  - Assume +/- 10% V_{DD} variation
  - ➢ LARGE skew impact for modest power supply variations!

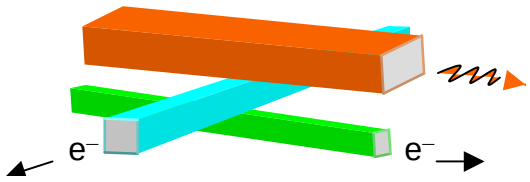


- Receiver operating temperature:
  - Consider T percent variations
  - ➢ ~100 ps skew change for 100% ΔT variation

- SUMMARY

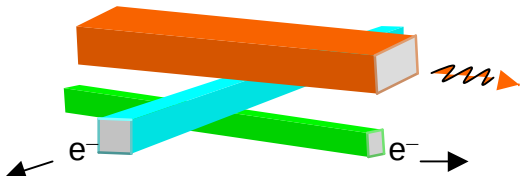
Parameter	Skew for 10% variation
Temperature	10ps
Power Supply	100ps
Threshold Voltage	20ps
Poly Length	80ps

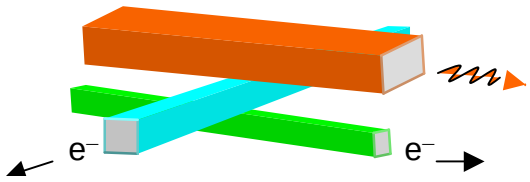




Conclusions and Future Work

- Feasibility of on-chip optical interconnects is likely to be limited by the optoelectronic conversion circuitry
- Variations in the device and operating conditions have a profound impact on the performance of optical clock distribution approach
  - Introduce substantial skew and delay in otherwise ideal system
- Future work:
  - More robust receiver circuit design should be evaluated
  - Further analysis of other optical applications and system benefits
    - Global on-chip signal distribution feasibility and variation issues
    - Electromagnetic noise reduction, isolation
    - Potential power savings





Acknowledgments

- Faculty and students in the optical interconnect thrust in the MARCO Interconnect Focus Center, including D. Lim and L. Kimerling
- This work has been supported by the DDR&E and MARCO under the Interconnect Focus Center