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Variation Issues in On-Chip Optical Clock Distribution

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Abstract - On-chip optical clock distribution is being investigated as a future means to increase clock speed and reduce clock power. While extremely small skew in the arrival of an on-chip optical signal can be achieved, the conversion of the optical signal to a local electrical clock may be subject to substantial variation. A baseline receiver circuit has been designed and fabricated. We find that sensitivity to device and operating condition variation reintroduces substantial clock skew. Future optical on-chip clock design approaches must take such variation sources into account.

Introduction - On-Chip Optical Clock Distribution

To achieve future desired clock speeds well beyond 2GHz in high performance integrated circuits, alternative technologies for on-chip signal and clock distribution are being explored. One option is optical distribution of a global clock signal, with conversion to a local electrical signal as pictured in Fig. 1. In this scenario, an off-chip optical source is brought to the chip, distributed through waveguides, and converted through receiver circuitry to a local electrical clock distribution network. The potential advantages of such optical clock distribution include a very low skew distribution of the optical signals, enabling high clock speeds. In addition, such clocks may be more noise immune and generate less on-chip noise, and power reductions may also be possible [1].

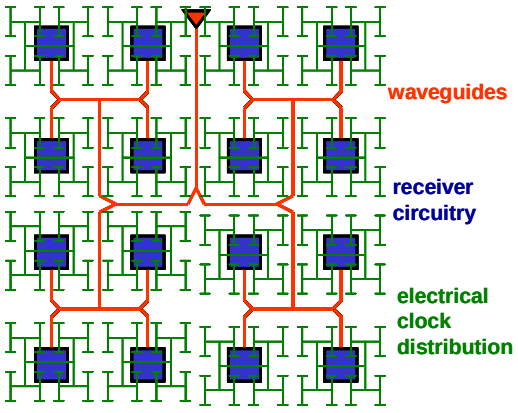

Figure 1. Optical distribution of global clock signal, with conversion to local electrical clock distribution.

In previous work, we have examined process variation concerns in electrical clock distribution [2]. In this paper, we examine variation issues in the implementation of an optical clock distribution approach. First, we examine what variation might be expected in the system, and consider potential sources of that variation. In order to make concrete evaluations of process and operating condition variation impact, we present a baseline optical receiver design. A test chip was fabricated to verify the operation of the design. Variation impact analysis is reported to identify potential limitations on clock speed due to variations.

Variation Sources

Considering Fig. 1, several potential sources of variation can be identified. First, the external optical power source will have some limitations, in terms of jitter or power variations. In this study, we will neglect these and focus on the on-chip sources of variation. Second, the optical waveguides themselves will have some degree of geometric variation. These variations are not likely to create large arrival time skew (in terms of the time at which light reaches the different detectors across the chip). However, variations in the corners and bends, in particular, may introduce variation in the amount of optical energy loss along different paths. Third, and the key focus in this study, are variations in the optoelectronic receiver. Important variations in the receiver may include the photodetector, the transistors and interconnect in the receiver, and operating conditions (e.g. temperature or power supply variations across the chip). Finally, variations may also exist in the local electrical clock distribution network; we neglect these and focus instead on the optical receiver elements.

Baseline Receiver Design

The overall architecture of the optical receiver is shown in Fig. 2. The receiver consists of a photodiode detector which we model as a current source having some diode capacitance and resistance. The detector current is converted to a low level voltage signal by a transimpedance amplifier; additional voltage amplification may be needed (depending largely on the current

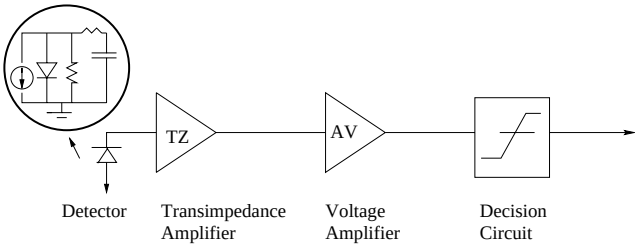

Figure 2. Overview of baseline optical receiver circuit.

level of the photodiode). This voltage signal can then be used to generate a full-swing clock signal for local distribution.

Design Goals and Constraints

Our approach is to implement the baseline receiver circuit in conventional CMOS without analog extensions [3]. For test chip fabrication, we use a 0.35µm CMOS technology provided through MOSIS. The design goal is to achieve 1 GHz bandwidth in this technology.

Implementation

The high level implementation is pictured in Fig. 3, together with the full circuit. The preamplifier converts 10mA signals to 10mv. The voltage amplifier uses a level shifting and replica feedback biasing configuration to amplify the 10mv voltage signal to a 3.3v rail-to-rail voltage.

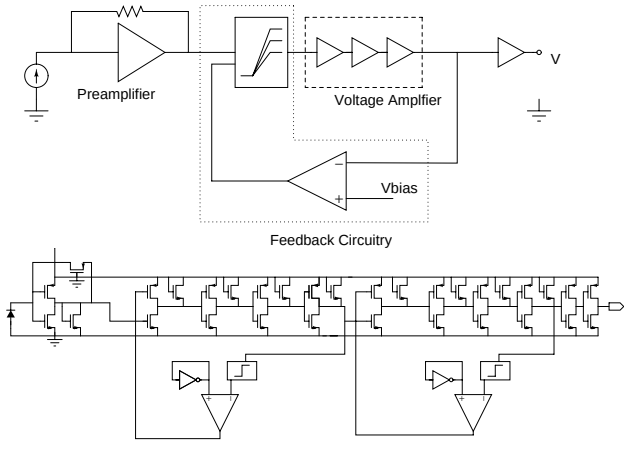

Figure 3. Receiver circuit implementation

Layout and Fabrication

The test chip was fabricated [4]; a die photo is shown in Fig. 4. Five receivers were placed at corners and center edge of a 2mm x 2mm chip, each connected to a Si diode detector. The circuit design functioned correctly; example measured waveforms are shown in Fig. 4. Limitations were found in the amount of optical power that could reach the photodiodes, due to the narrowness of slits fabricated in the top metal protective overplate. Redesign of the photodiode is needed for better optical access. Future research is expected to focus on test fabrication of the waveguide and more efficient detectors (as well as on-chip optical sources).

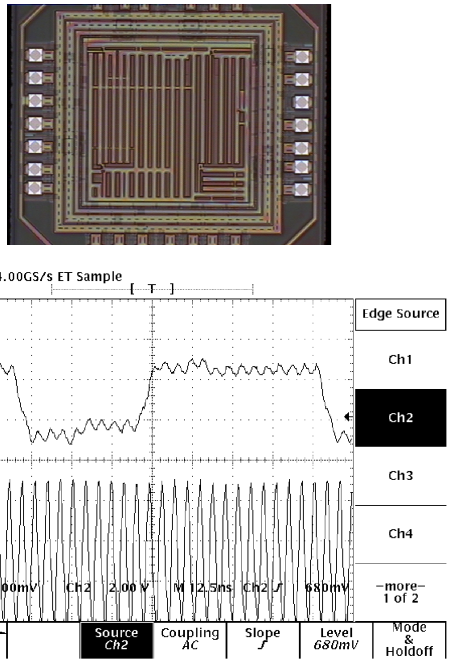

Figure 4. Die photo and waveforms from fabricated optical receiver test chip.

Variation Analysis Approach

To study the sensitivity to the variation sources discussed earlier, the methodology pictured in Fig. 5 was used. Each variation source is considered (detector, systematic device geometry, environmental). Circuit simulation is performed to extract the resulting delay along paths and skew between two clock paths. These are used to calculate a sensitivity of delay/skew to that variation source.

Variation Analysis Results

Here we consider each of several possible variation sources, and report the resulting impact.

Waveguide Variation

We assumed up to a maximum of 10% variation in

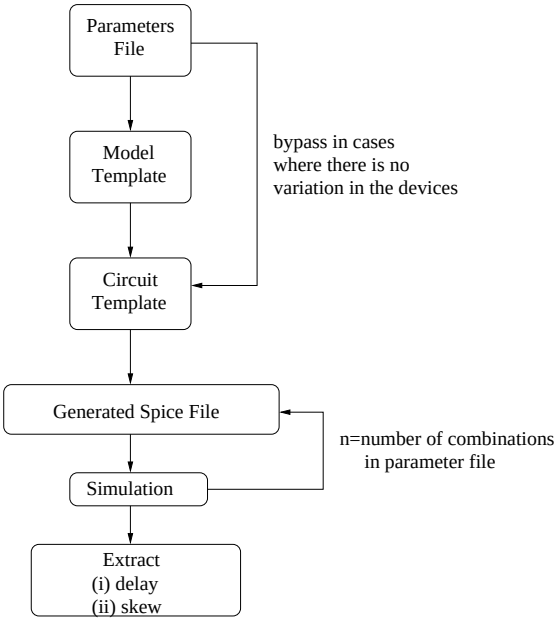

Figure 5. Variation simulation and analysis methodology.

the cross-sectional area or optical properties of the poly/oxide waveguide pictured in Fig. 6. We estimate that such variations will result in less than 2ps skew in the time of arrival of light..

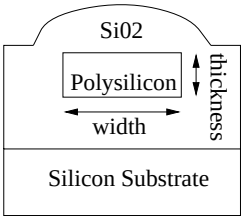

Figure 6. Optical waveguide: variation in poly width and height considered.

Detector Variation

We considered two sources of variation related to the photodiodes. First, we assume up to 10% variation in the received optical power, resulting in a 10% variation in the current produced by the diode. Second, we assumed a constant dark current of ~1μA.

An interesting trade-off exists between the size of the diode, the complexity of the receiver circuit, and the sensitivity of the circuit to these variation sources. For higher photodiode currents, fewer amplifier stages and less power is needed; larger diode currents also reduce sensitivity to dark current variation. However, larger chip area or more efficient diodes (e.g. non-silicon) are required. These trade-offs are captured in Table 1.

Input Current	Absolute Skew	Average Power
8 μA	8 ps	60 mW
10 μA	0 (Nominal)	60 mW
12 μA	4 ps	60 mW
89 μA	4 ps	35.5 mW
100 μA	0 (Nominal)	35.5 mW
111 μA	2 ps	35.5 mW
900 μA	22 ps	11.5 mW
1000 μA	0 (Nominal)	11.5 mW
1100 μA	14 ps	11.5 mW

Table 1: Skew and power for 10μA, 100μA, and 1000μA detector diode current devices.

Receiver Device V_T Variation

We assumed an area dependent transistor threshold variation:

$$\sigma_{\Delta VT} = \frac{A_{VT}}{\sqrt{WL}}$$

and a matching variation of:

$$V_T = \mu_{VT} \pm \frac{3.09}{\sqrt{2}}\sigma_{\Delta VT}$$

The resulting skew as a function of $\%V_T$ variation was simulated, and founded to give +/- 20ps skew for a 15% V_T variation.

Receiver Device Channel Length Variation

We next consider channel length variation in the receiver circuits. Assuming a systematic ΔL variation (e.g. from one region on the chip to another), a large skew can result. For example, a 10% ΔL variation can result in 70ps clock skew.

Receiver Power Supply Variation

We found the simple baseline receiver circuit to be very sensitive to power supply variation. A -10% V_{DD} variation across the chip results in nearly 100ps skew.

Receiver Operating Temperature

Large temperature variations across the chip (arising from different dissipations of nearby circuits, for example) can also result in large clock skews. A 100% ΔT variation would generate ~100ps clock skew.

SUMMARY

The results of variation analyses on the baseline receiver circuit design are summarized in Table 2. For approximately 10% variation in temperature, power

Parameter	Skew for 10% variation
Temperature	10ps
Power Supply	100ps
Threshold Voltage	20ps
Poly Length	80ps

Table 2: Summary of clock skew resulting from important variation sources.

supply voltage, threshold voltage, and polysilicon channel length, the resulting clock skews are shown. Clearly, variations have a profound impact on the performance of an optical on-chip clock distribution approach. These variations introduce substantial skew and delay in an otherwise high speed clock approach. In order for on-chip optical clock distribution to be viable, more work is needed to design receiver circuits that are robust to process and operating variation sources.

ACKNOWLEDGEMENTS

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