Layout Practice Impact on Timing and Yield

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Acknowledgments

- Joe Panganiban, Karen Gonzalez-Valentin (MIT)
- Sani Nassif, Chandler McDowell, Anne Gattiker, and Frank Liu (IBM Austin Research Laboratory)
- Manuela Huber (SEMATECH/Infineon)
- Support for this work supplied in part by International SEMATECH

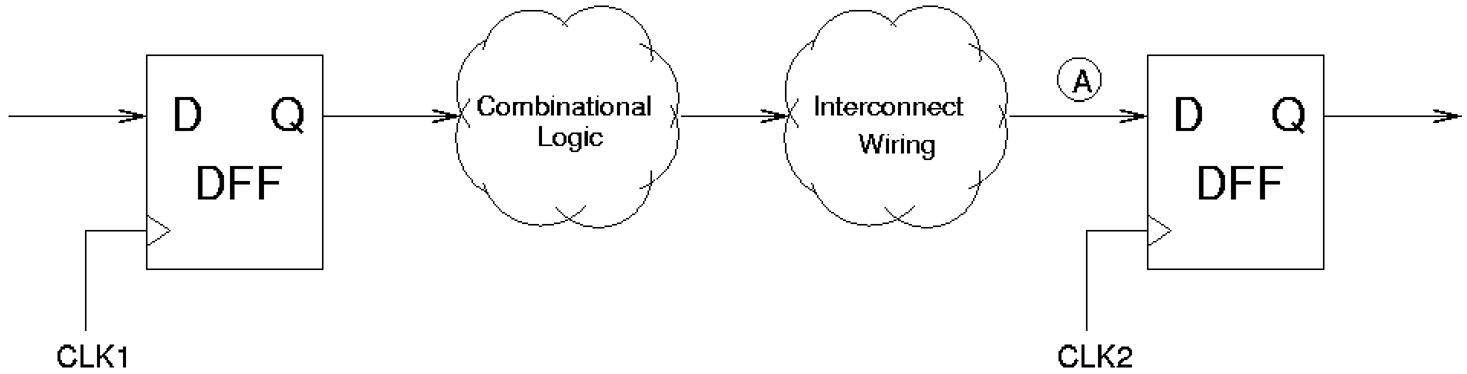
Outline

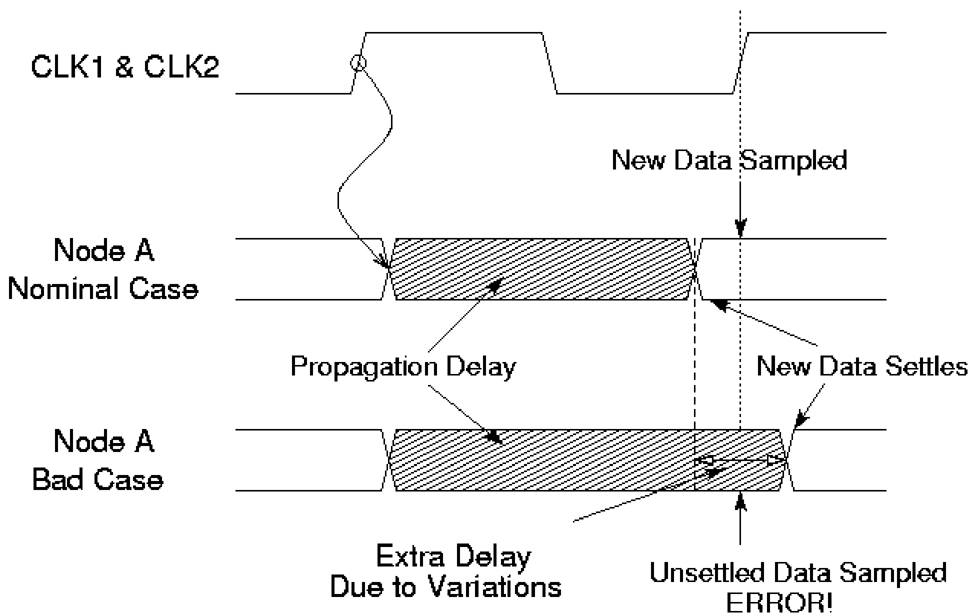
- Introduction: Process Variation and Timing
- Core Test Structure – Ring Oscillator
  - Device & Interconnect Variants
- Variation Test Chip Architecture
- Results
  - Spatial Variation
  - Layout Dependencies
- Conclusion

Introduction

- Goal: measure and extract variation in a given process and link it to circuit performance
- Focus is on *parametric* variation
  - continuous geometric or material process variations
  - not examining *defect* yield concerns
- Need to understand variation in both
  - FEOL – front end of line or *device* level
  - BEOL – back end of line or *interconnect* level

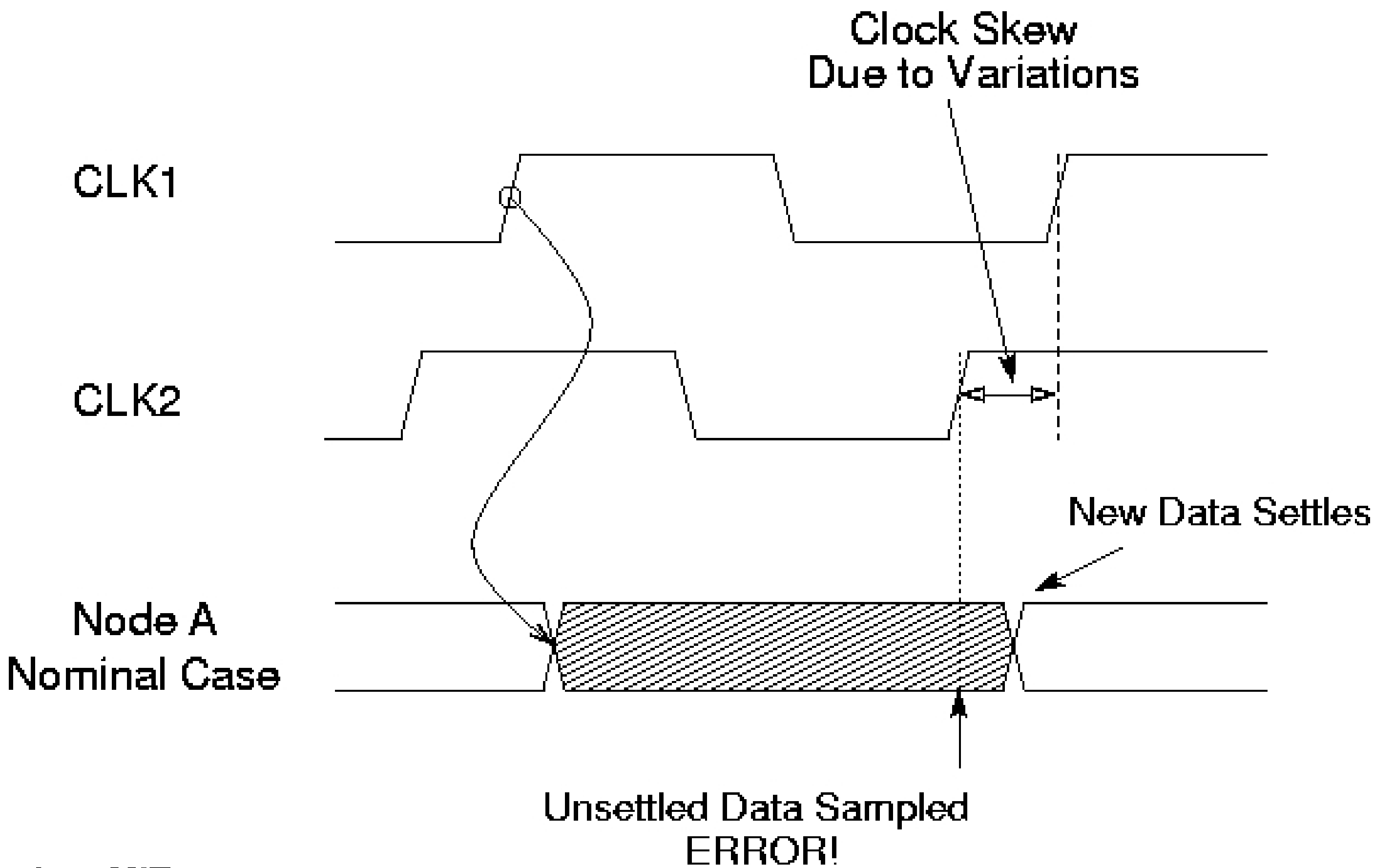
Variation Induced Timing Errors





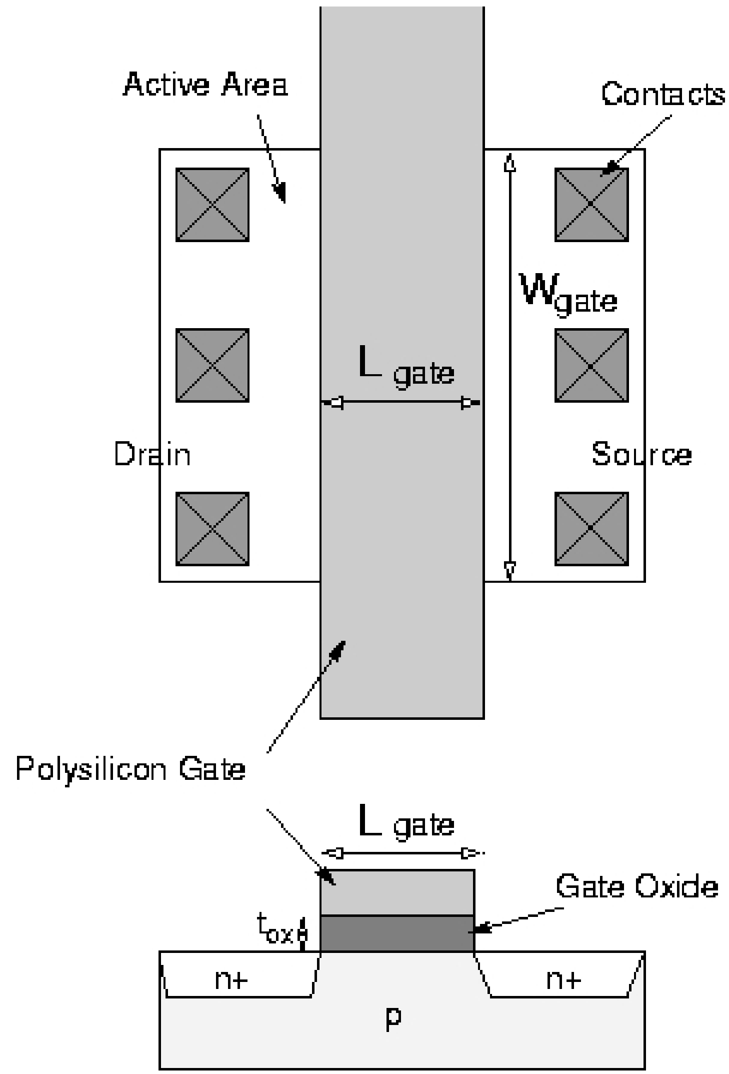
Variation Induced Clock Errors

- Variation in device and/or interconnect delay can also lead to timing errors due to clock skew

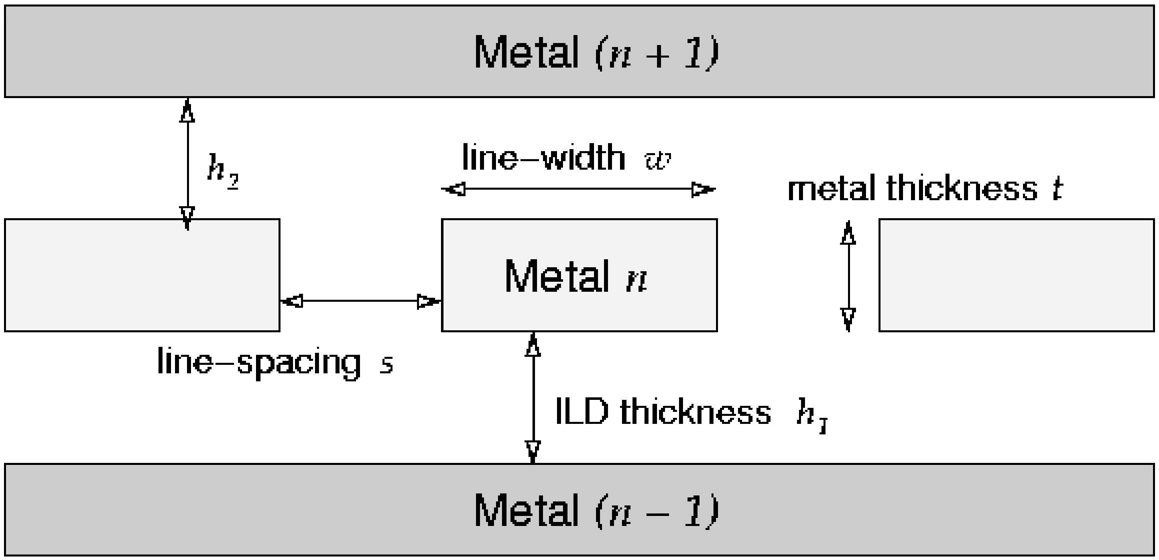


Device Variation

- Key parameters:
  - L_{gate} – channel length
  - V_T – threshold voltage
  - t_{ox} – oxide thickness



Interconnect Variation



- Key parameters:
  - – Metal thickness – t
  - – Dielectric thickness – h_1, h_2
  - – Metal line width (and line spacing) – w, s

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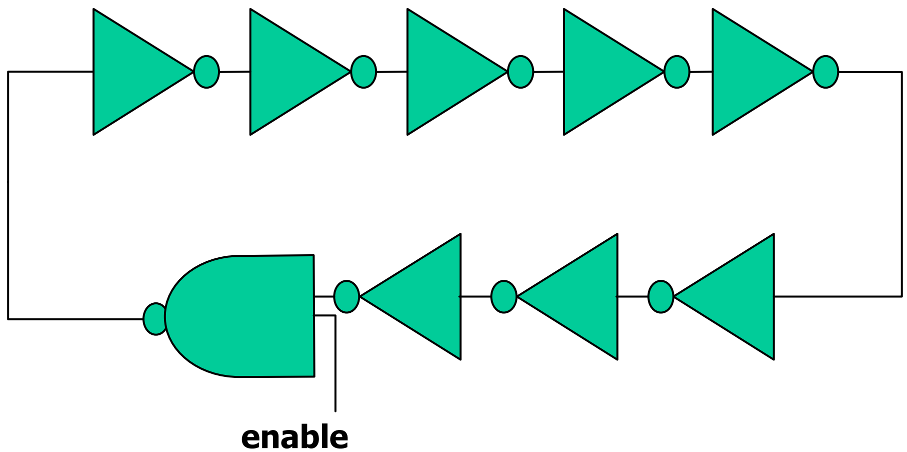
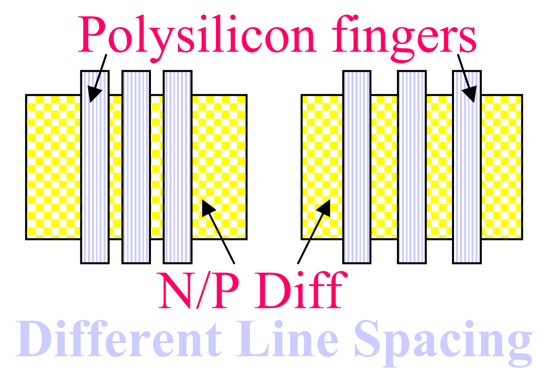
Approach: Use Ring Oscillator (RO) as Core Test Structure

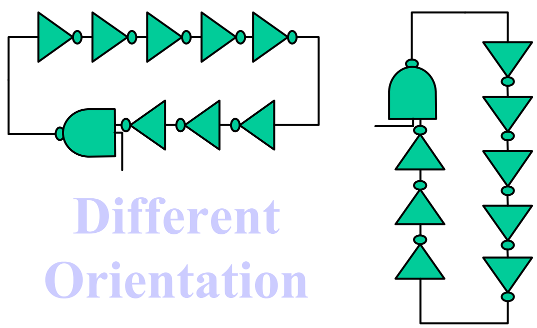
- Ring Oscillator frequency
  - can be made sensitive to device and interconnect parameters
  - is a direct *circuit-level timing parameter* that can be easily measured
- Generate large number of ROs
  - different layout practices to understand variation impact

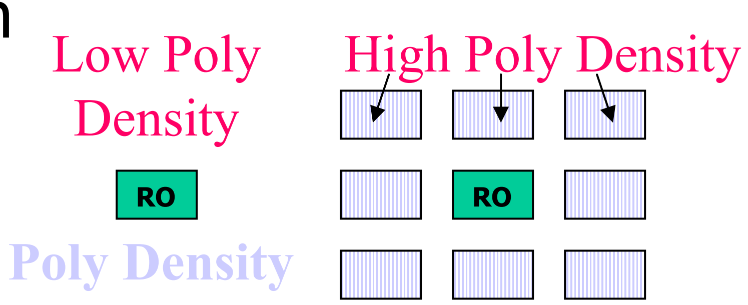


FEOL RO Test Structures

- Device variation structures consist of ROs with only inverters (no additional load between inverter stages)
- Key variations studied:
  - proximity effect – RO finger spacing
  - number of fingers
  - vert/horiz orientation
  - etch loading – local polysilicon pattern density

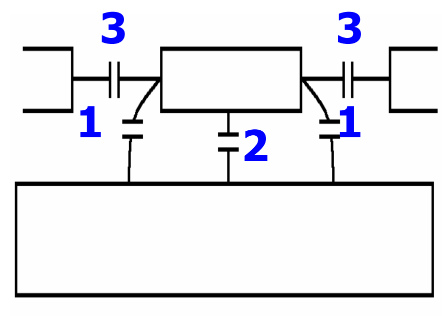


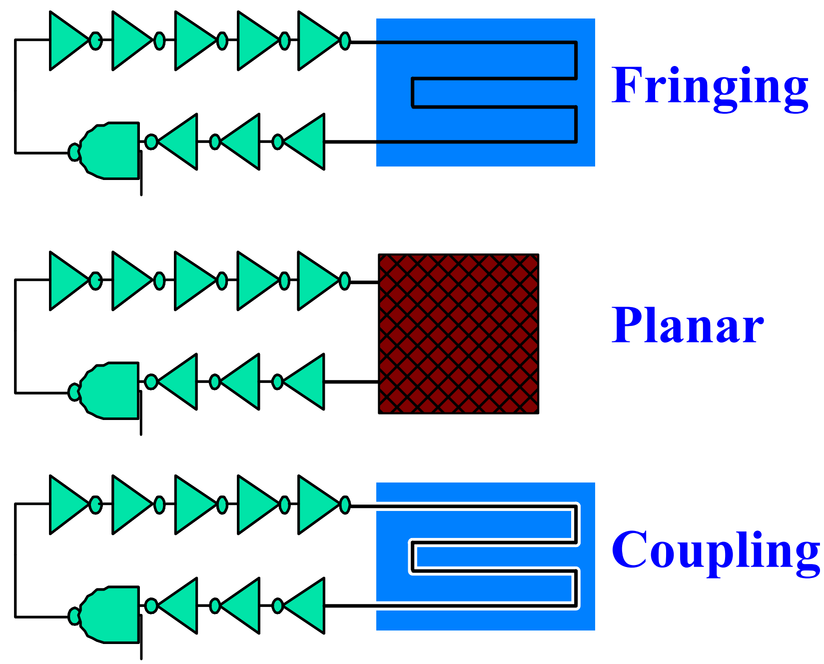




BEOL RO Test Structures

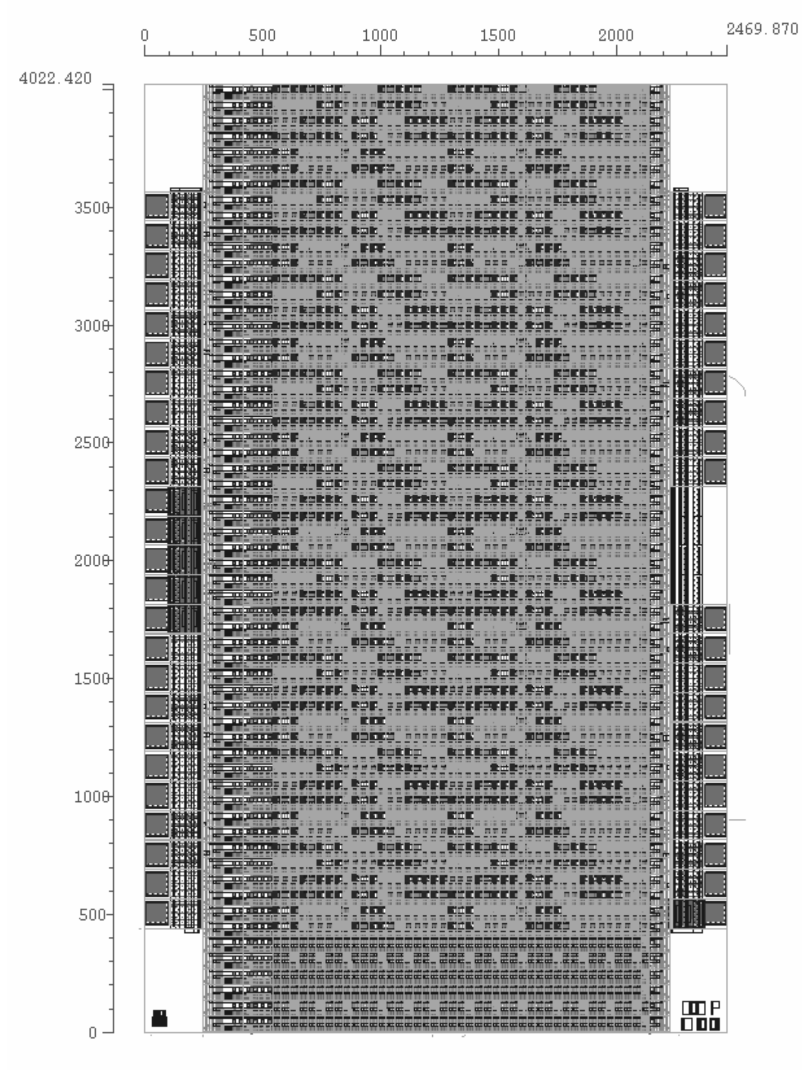
- ROs with metal load which dominates the output frequency
- Interconnect chosen to accentuate a specific variation
- Each emphasizes a different capacitance:
  - Fringing (1)
  - Planar (2)
  - Coupling (3)





Test Chip Approach

- Heavily replicate various RO test structures across chip
  - 60 rows
  - 43 tiles/row
  - 2580 total tiles
- 2.4 mm x 4.0 mm
  - 10 mm^2
  - Standard pads – package chip for simplified measurement
- Fabricated in 0.25 µm MOSIS technology



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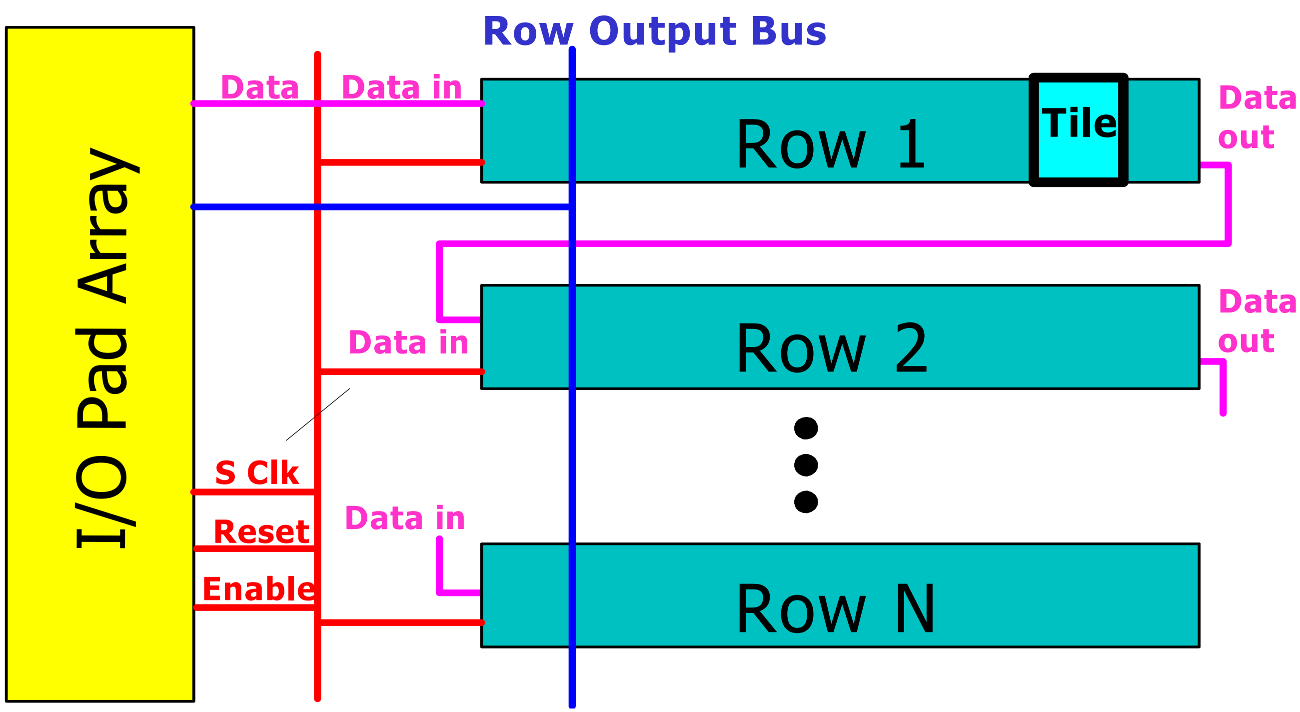
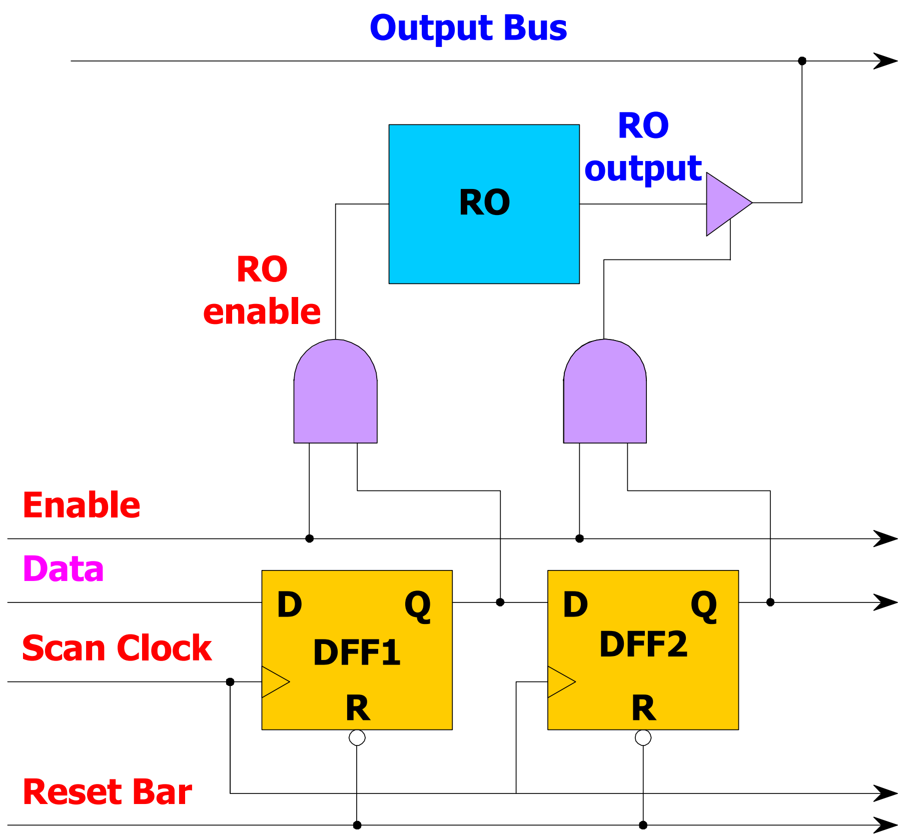
Variation Test Chip Architecture

- Emphasis: hierarchy, regularity, and repetition
- Scan chain for control
- Shared readout



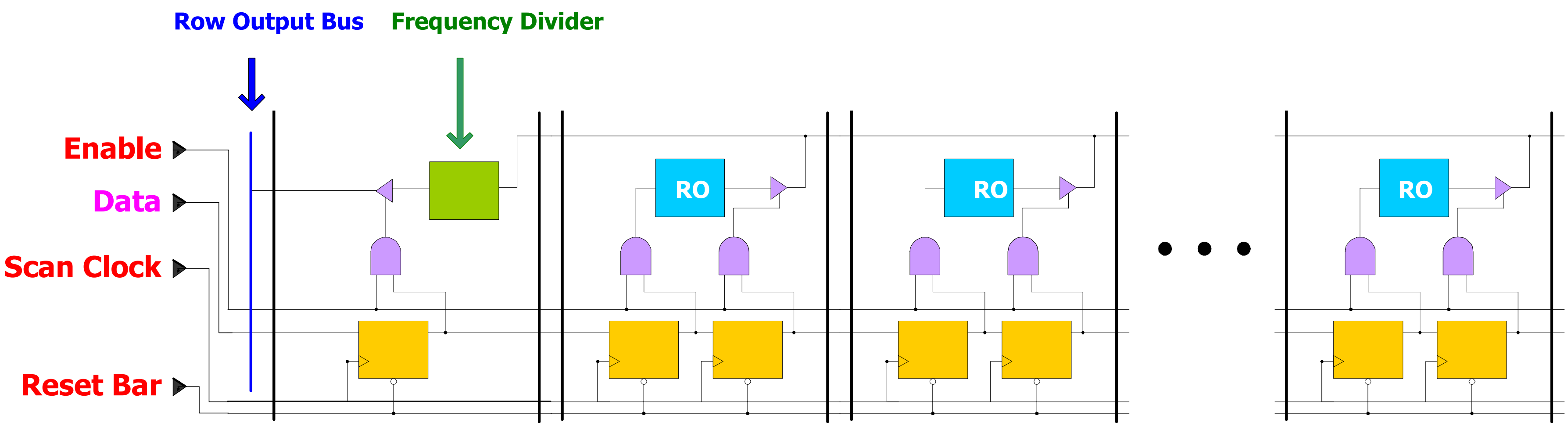
Test Chip Hierarchy – Tile

- Basic building block of chip
- Single RO + control
- Shift registers control ROs:
  - Left: turns on/off the RO
  - Right: gates RO to output bus
- Control signals
  - *scan-clock* (for shift registers)
  - *data* (control for the DFF)
  - *enable* (to enable the RO)
  - *reset* (resets the registers)
- Output signal
  - Shared *output bus*



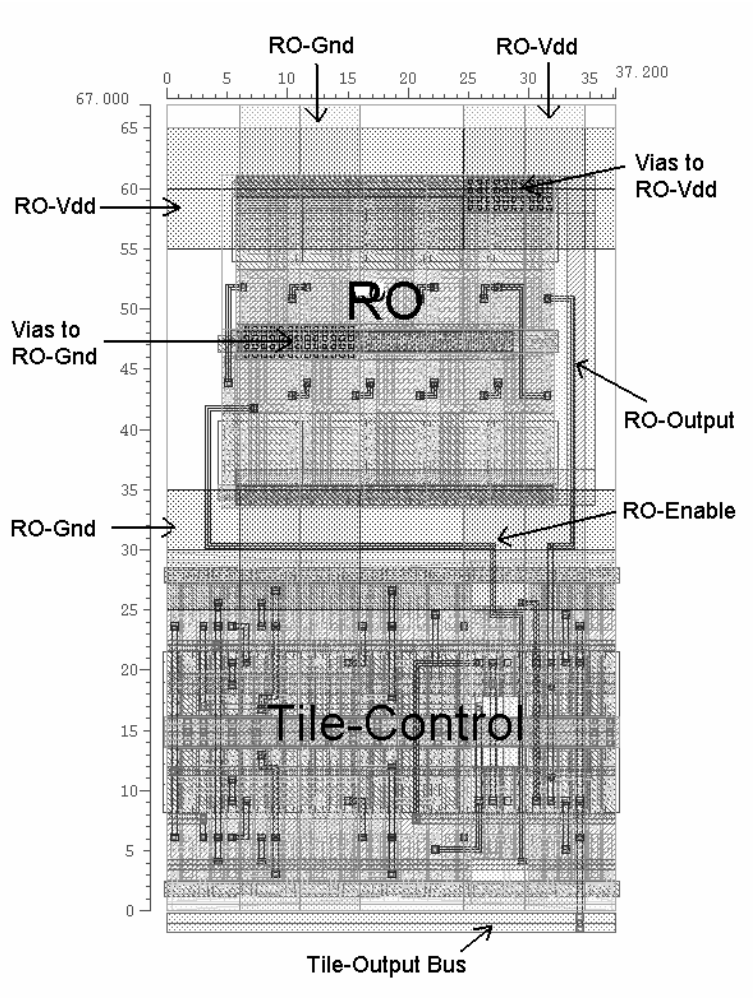
Test Chip Hierarchy – Row

- Horizontal chain of tile blocks
  - Extend across the width of the chip
  - Row buffers drive row tiles
- Divider tile
  - Divides the frequencies of the output bus by $2^6 = 64$ for off-chip measurement: resulting 1-5 MHz signals easily read with digital I/O
  - Divider tile also controls the *row output bus*

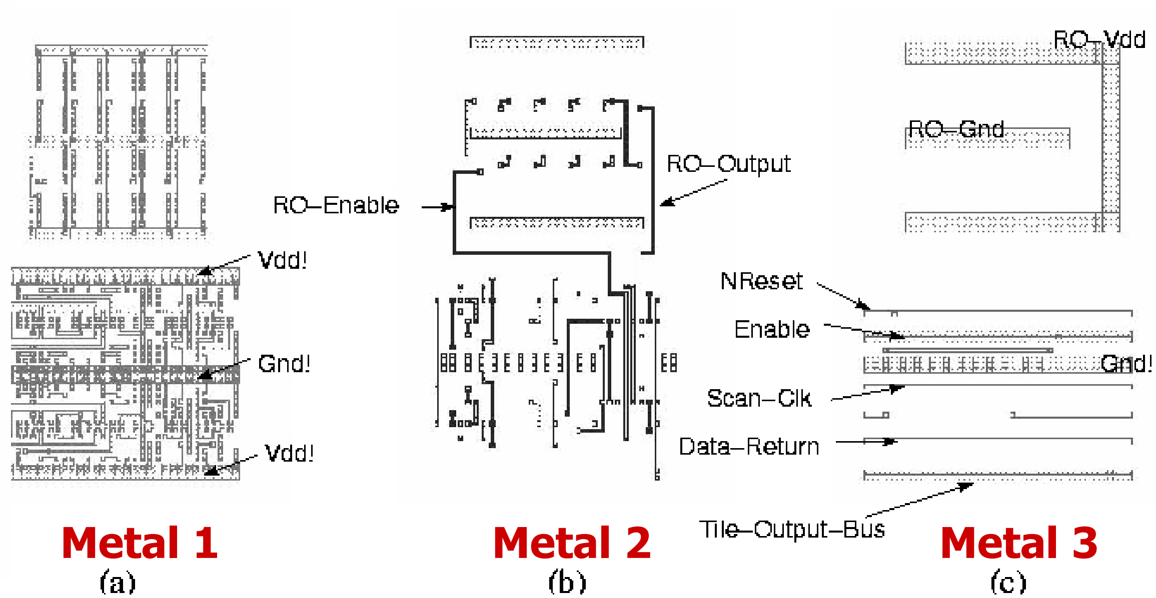


Basic FEOL Tile Layout

- Each tile ~50% RO / 50% control
- Separate power/gnd for RO / logic
- M3 for global wiring, local power
- M4/M5 for power/gnd

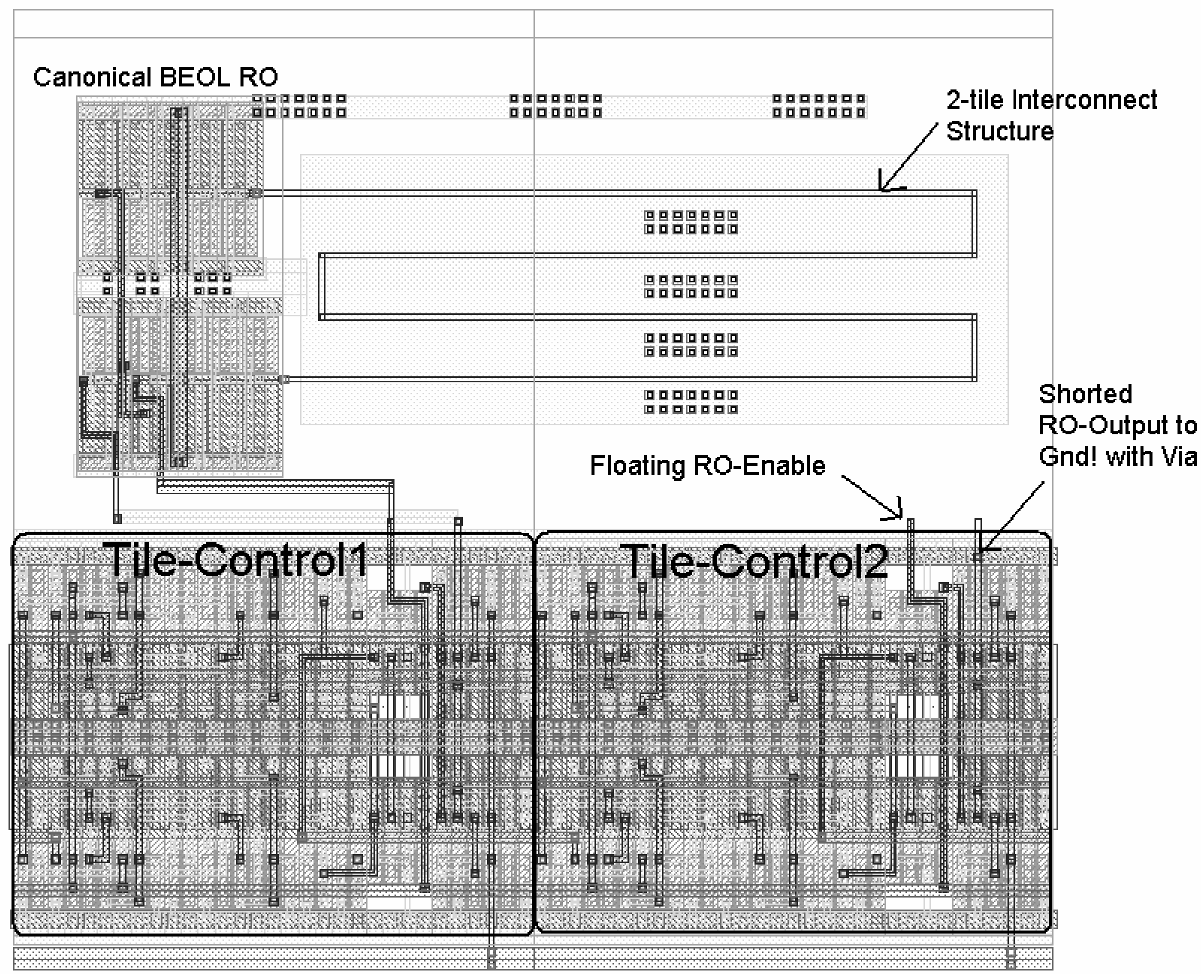


67 µm x 37.2 µm

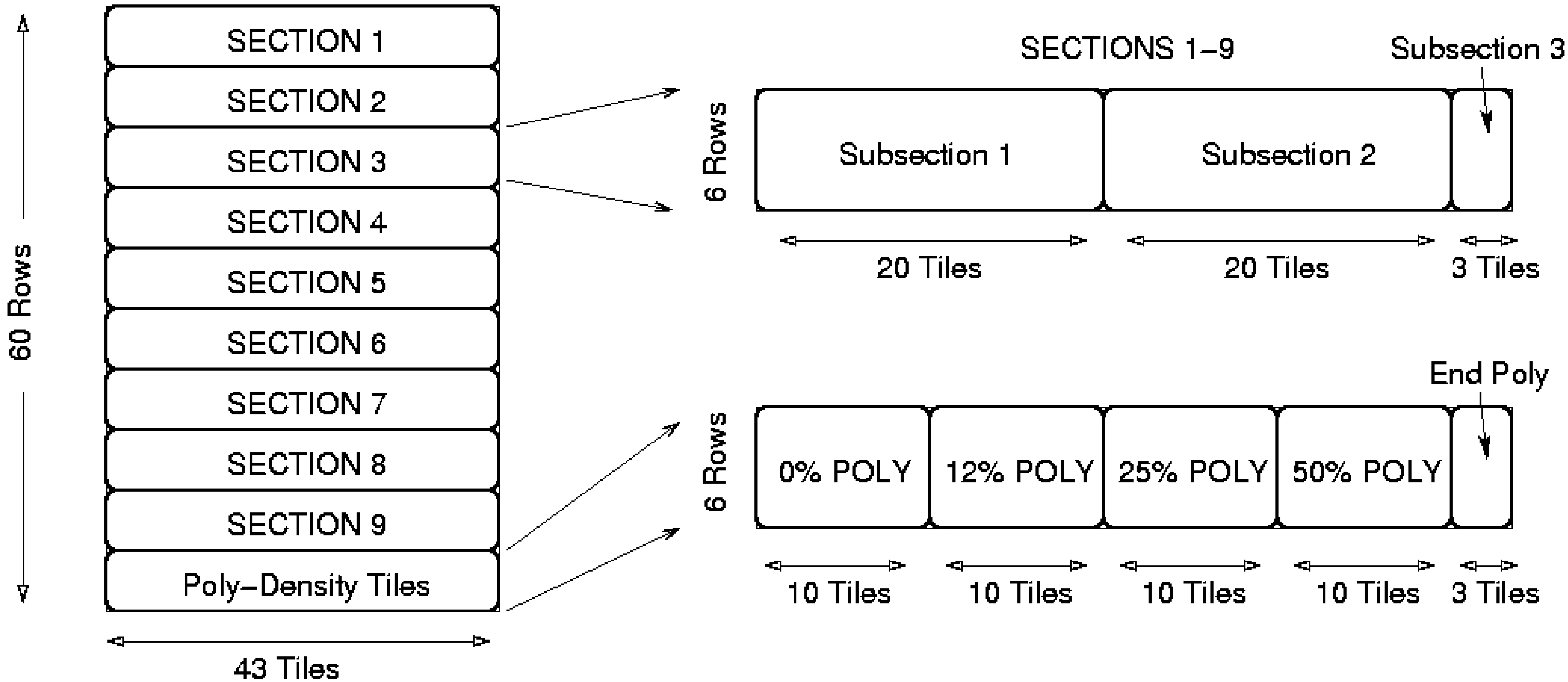


Example BEOL Tile Layout

– Some BEOL structures require two tiles
    - One control block is unused

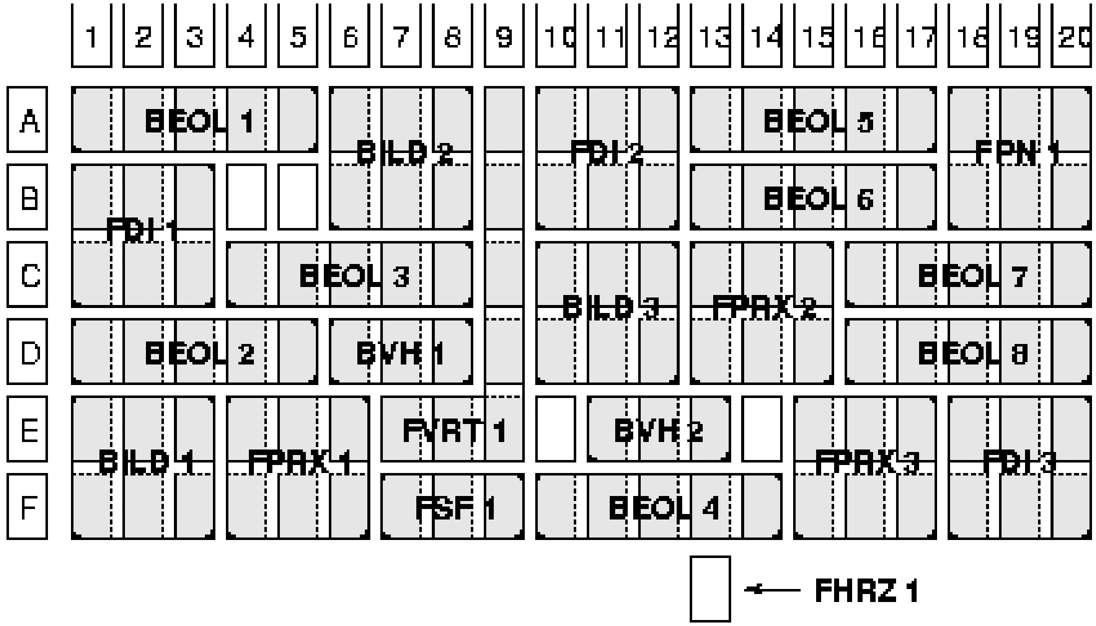


Distribution of ROs on Test Chip



- Available structures: 60 x 43 = 2580 tiles
- Organize in sections & replicate sections
- Poly density structures isolated at bottom of chip

Distribution of ROs on Test Chip



Group Abbreviation	Group Type
BEOL	Planar, Coupling, and Fringing BEOL
BILD	Inter-Layer Dielectric Thickness
BVH	BEOL Vertical vs. Horizontal
FPRX	Proximity (line-spacing) FEOL
FDI	Dense vs. Isolated Fingers FEOL
FPN	PMOS vs. NMOS FEOL
FVRT	Vertical FEOL
FSF	Single-Fingered FEOL
FHRZ	Horizontal (canonical) FEOL

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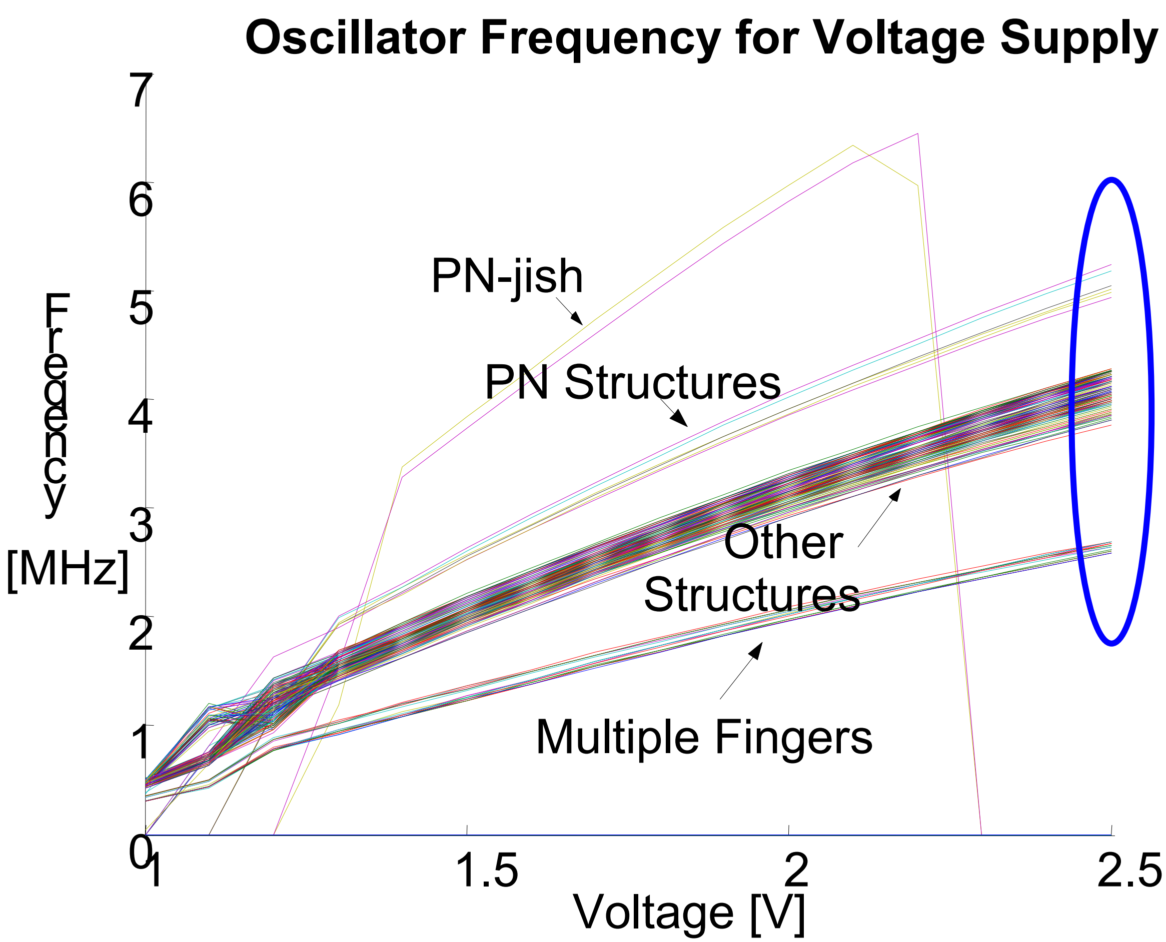
Fabrication & Functionality Test Results

- 0.25 μm MOSIS run
- 35 chips packaged for measurement
  - 40-pin DIP
  - 5 chips left unpackaged – probing/debugging
- Labview-based measurement
  - Simple/low-cost
- Verify Scan Chain Functionality
  - "null tiles" read zero at expected locations
  - divider operation: pre- and post-divider frequencies verified through microprobe measurements on unpackaged devices

RO Frequency Measurements



- RO freq as f(V_{DD})
- Can use V_{DD} dependency to separate V_T/C_{ox} from L variation
- Electrical repeatability good: σ ~ 0.1%
- Data shown in rest of talk is taken at V_{DD} = 2.5V

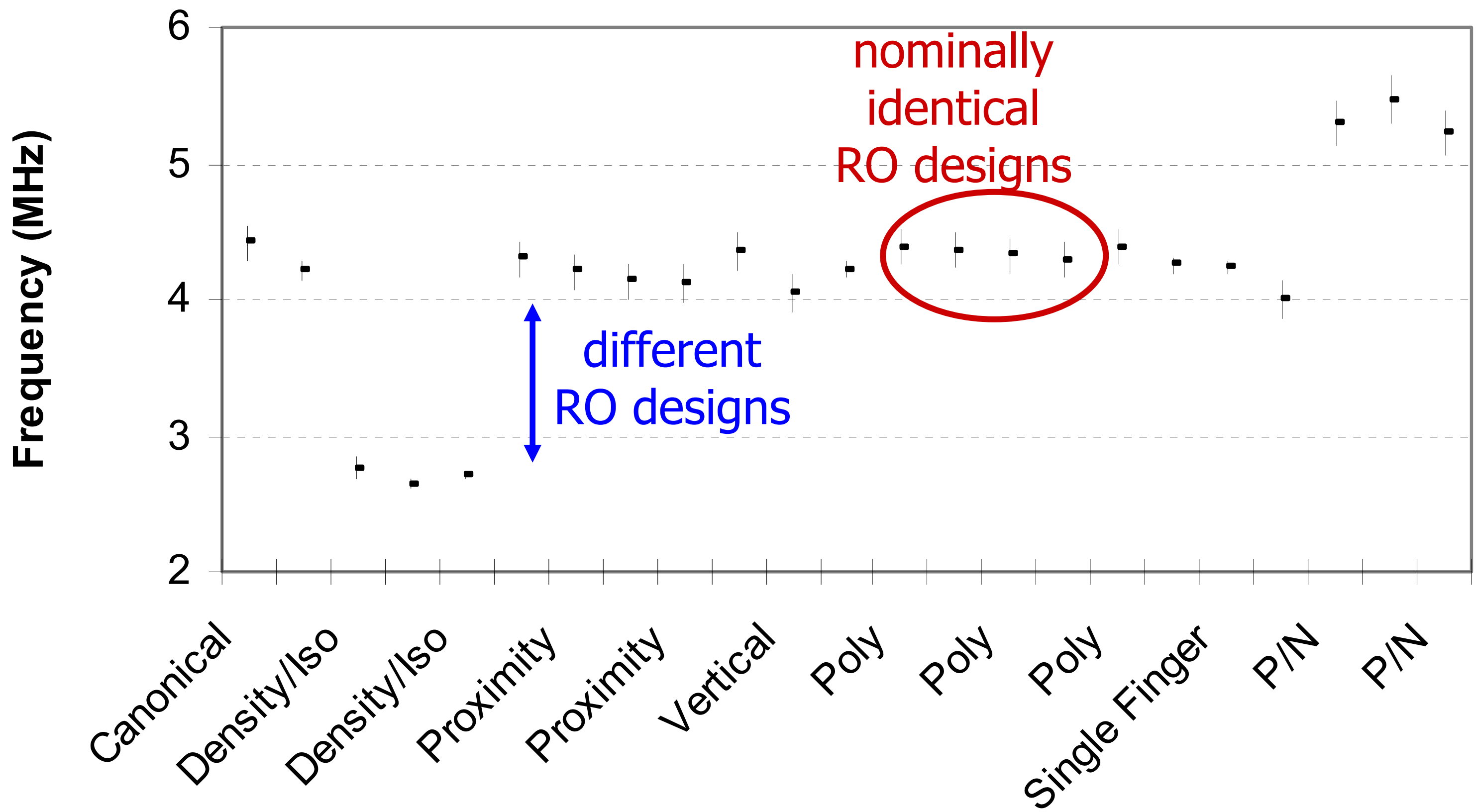
What Variations Are Measured?

- Uncorrelated variations minimized
  - random device to device variations are attenuated: 9 stage RO averages out individual inverter variations

$$\sigma_{RO}^2 = \frac{\sigma_{INV}^2}{9}$$

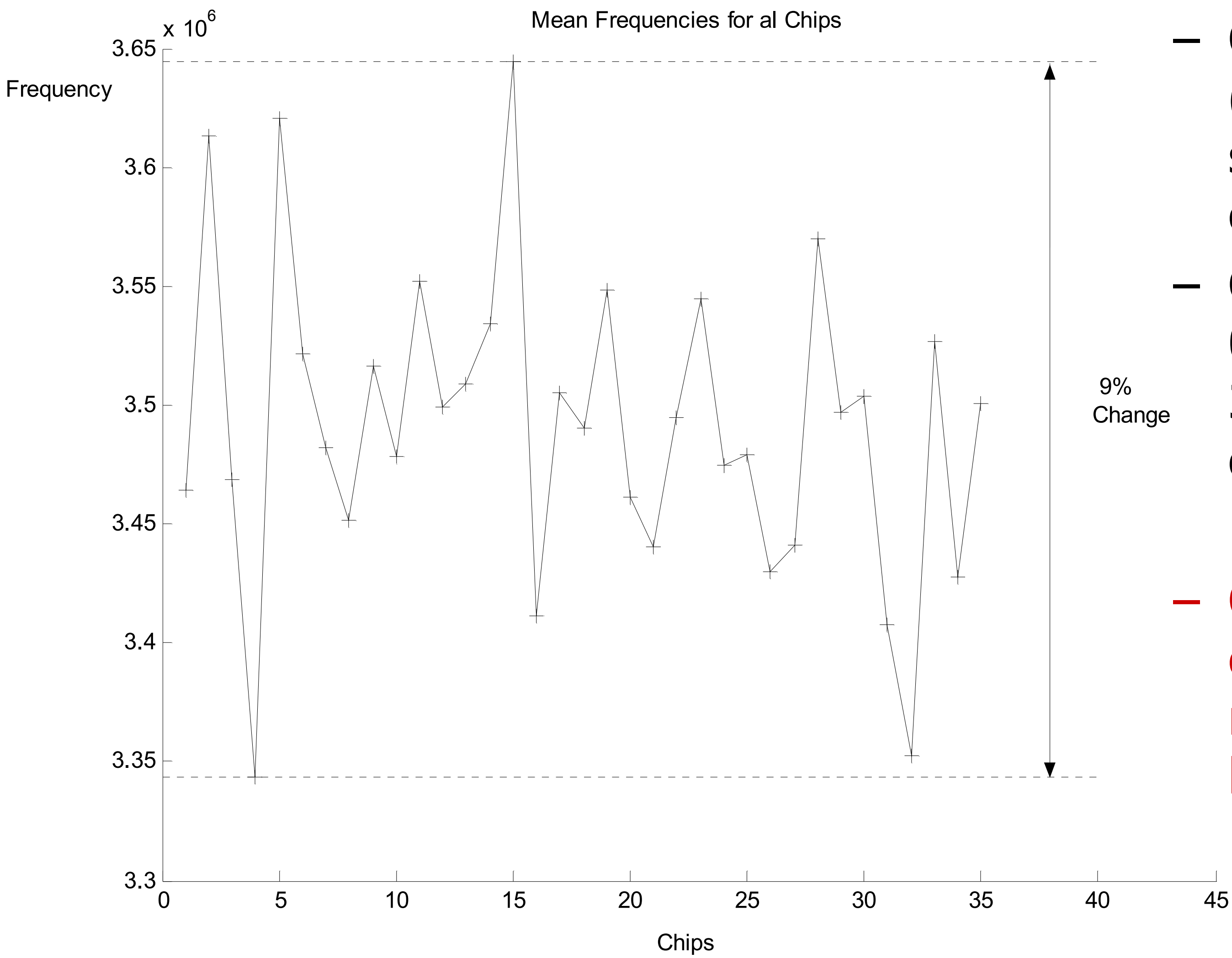
- Correlated variations – those that are common to the devices in a given RO – are enhanced for measurement of
  - Layout effects:
    - study how layout parameters impact RO speed/timing
  - Wafer level effect:
    - chip to chip variation – can be mapped on wafer
  - Within chip effects:
    - spatially dependent – can be mapped on chap
    - random/unmodeled effects

RO Frequency for Different FEOL Structure Types



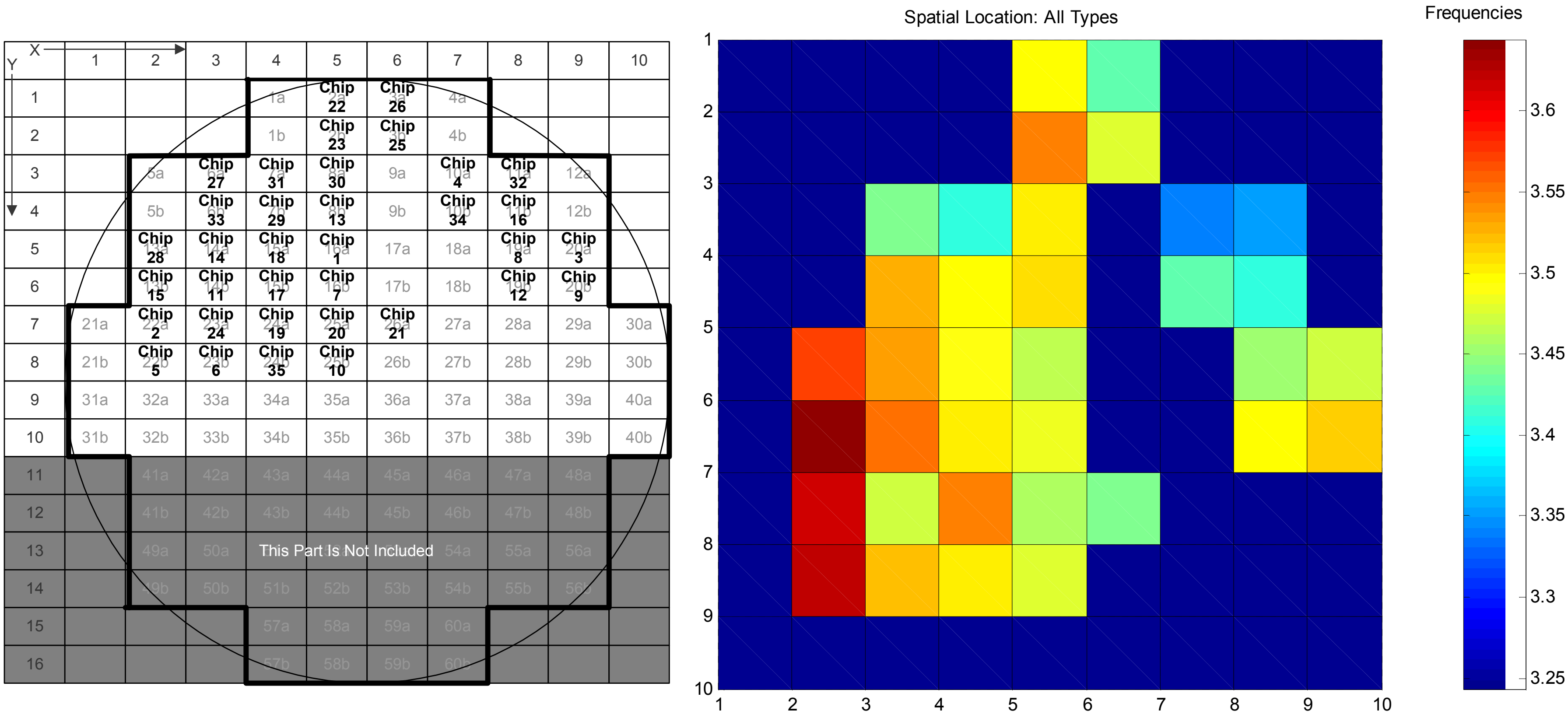
- Plot mean ± 1 σ_f (chip to chip + within chip spatial variation)

Chip to Chip (Wafer Scale)



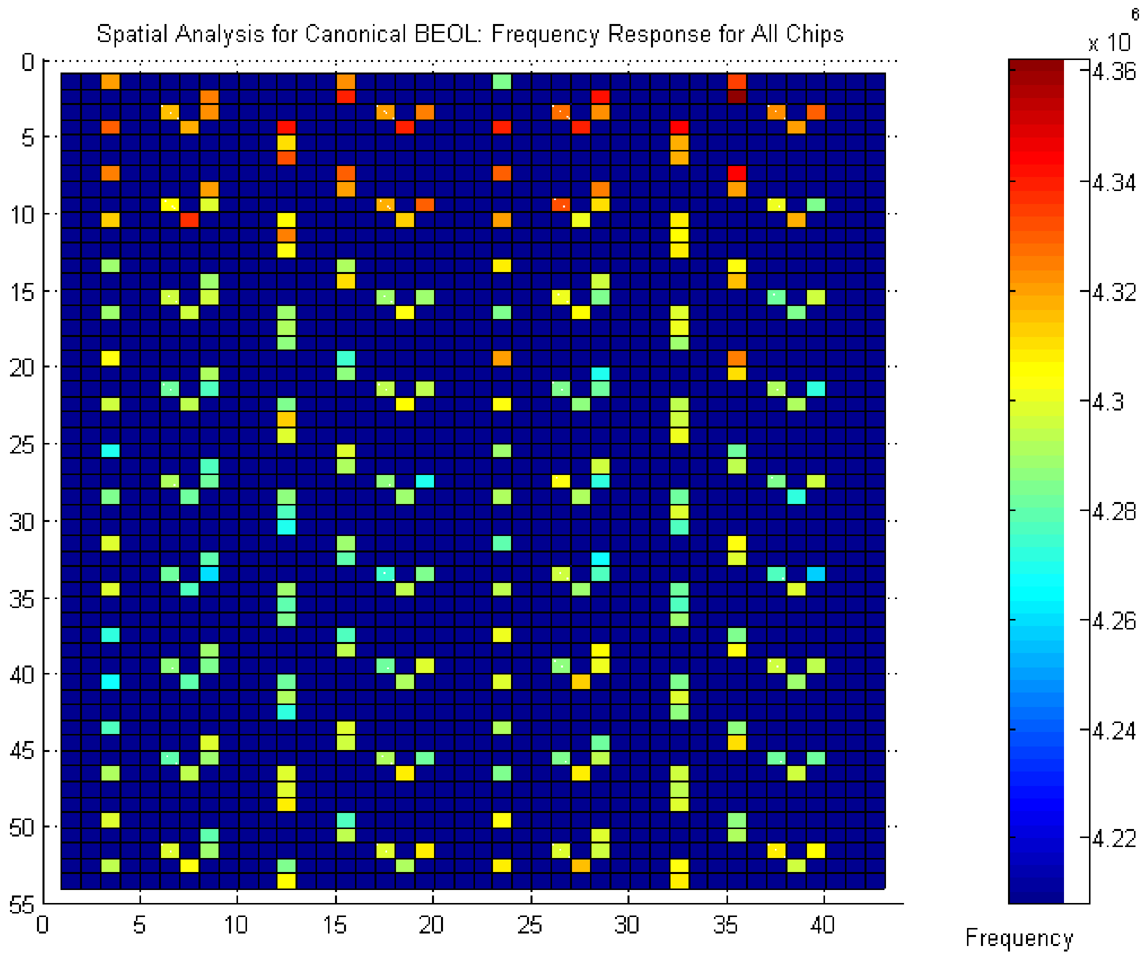
- Chip Mean (average of all structures on each chip)
- Chip to chip range 0.3 MHz: 3.35 to 3.65 MHz, or ~9%
- Observation: chip to chip effect much less than layout effect!

Wafer Scale Variation



- Chip location on wafer obtained
- Display chip average frequency across wafer
  - Observe clear wafer scale trend

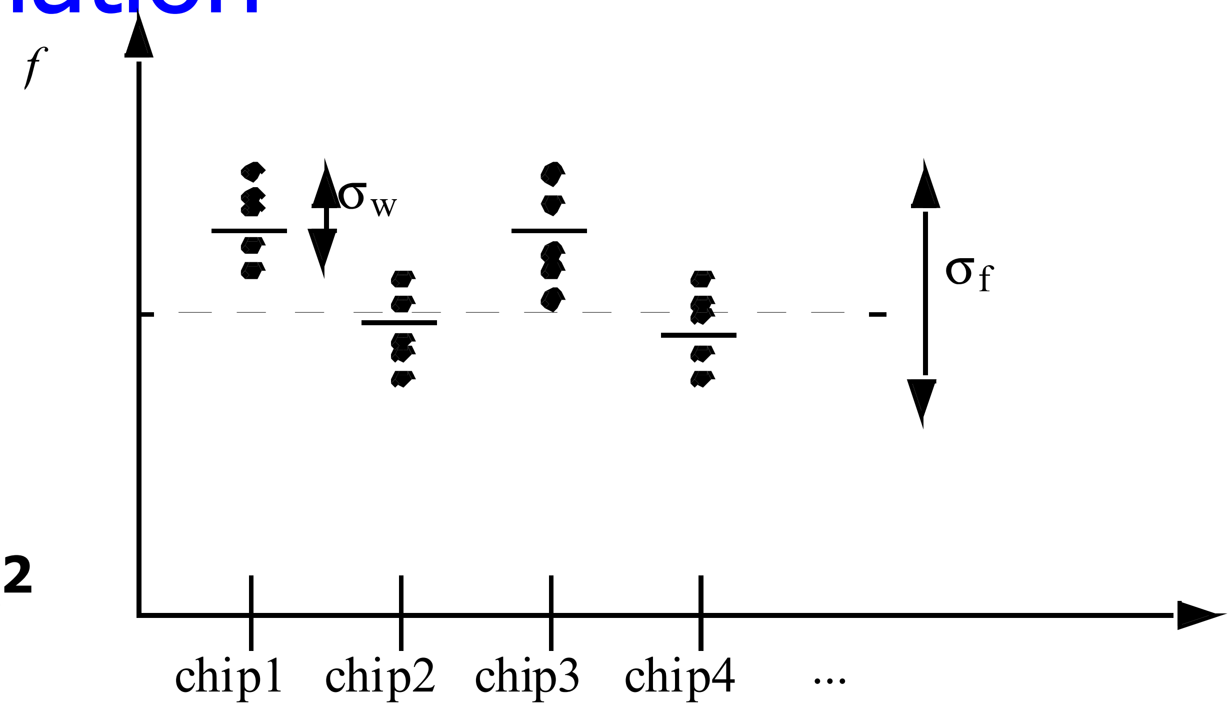
Within-Chip Spatial Trend



- Map *specific* RO type
  - average across all chips plotted
- Canonical BEOL RO
- Top to bottom trend
- Total variation:
  - 4.2 MHz to 4.4 MHz (4%)

- Observation: within chip effect also much less than layout effect

Chip-to-Chip vs. Within-Chip Spatial Variation



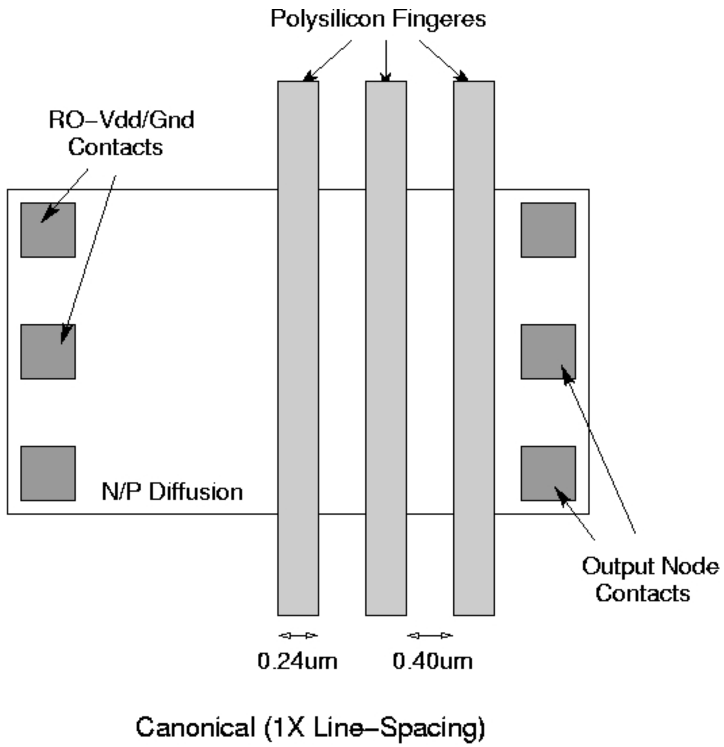
$$\sigma_f^2 = \sigma_c^2 + \sigma_w^2$$

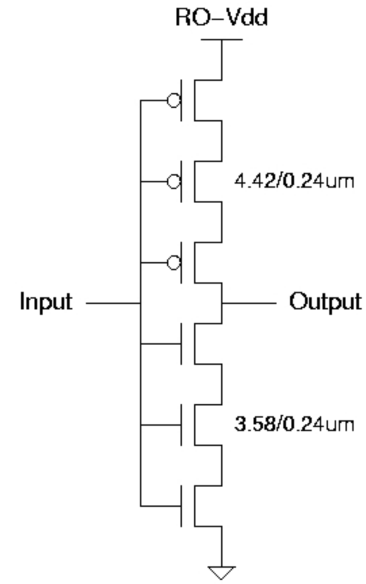
- Total variation observed in specific RO type: σ_f
- Chip-to-chip (wafer scale) variation: σ_c
- Within-chip variation: σ_w

Overall Results FEOL Structures

Description	FEOL RO Types	Mean Freq. [MHz]	σ Total [KHz]	σ wafer [KHz]	σ within-chip [KHz]
Canonical	Canonical FEOL	4.42	130	122	45
Density/Iso	2 Fingers, 1.5x Minimum Length	4.21	76	73	19
	4 Fingers, Minimum Length	2.76	77	71	28
	2 Fingers, 2x Minimum Length	2.64	39	36	15
	Single Finger, 4x Minimum Length	2.70	29	25	13
Proximity	1.2x Spacing Between Poly Lines	4.30	132	123	48
	1.5x Spacing Between Poly Lines	4.20	127	122	34
	2x Spacing Between Poly Lines	4.13	129	120	46
	3x Spacing Between Poly Lines	4.12	135	126	49
Vertical	Vertical Canonical FEOL	4.36	144	135	51
	Vertical, 3x Spacing Between Poly Lines	4.05	143	134	49
	Vertical Single Finger	4.22	59	51	30
Poly	0% Polysilicon Density	4.38	126	124	27
	12% Polysilicon Density	4.36	127	125	23
	25% Polysilicon Density	4.32	129	125	30
	50% Polysilicon Density	4.29	128	124	33
	Canonical at end of Density Structures	4.38	126	120	40
Single Finger	Single Finger	4.25	52	47	22
	Small Single Finger	4.23	51	48	18
P/N	PN Structure, Canonical	4.00	133	126	44
	PN Structure, 2P and 2N	5.29	164	154	56
	PN Structure, N Strong	5.47	172	161	61
	PN Structure, P Strong	5.23	163	153	55

Canonical Inverter RO

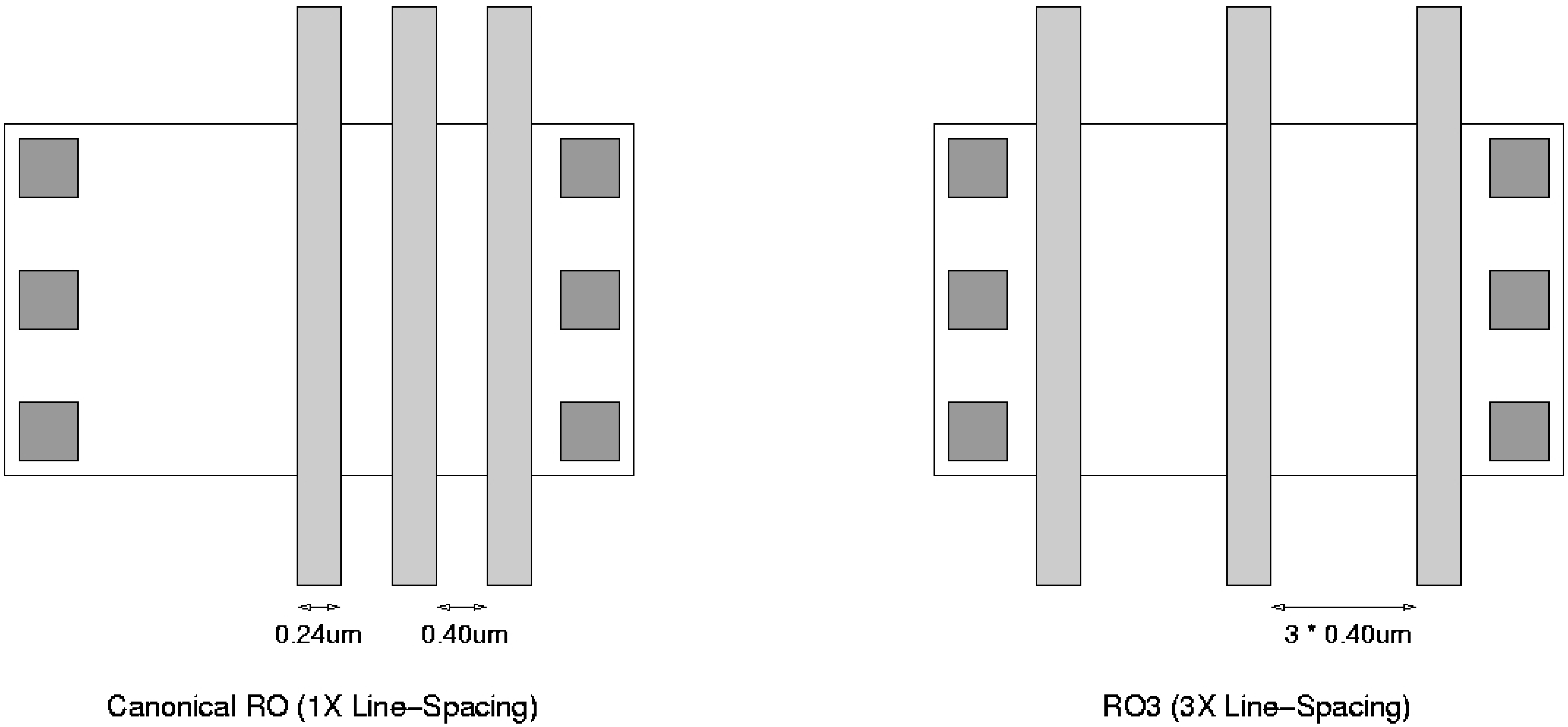




- Three finger P/N devices
- Minimum feature size (0.24 um)
- 1X line spacing (0.40 um)
- Heavily replicated on test chip

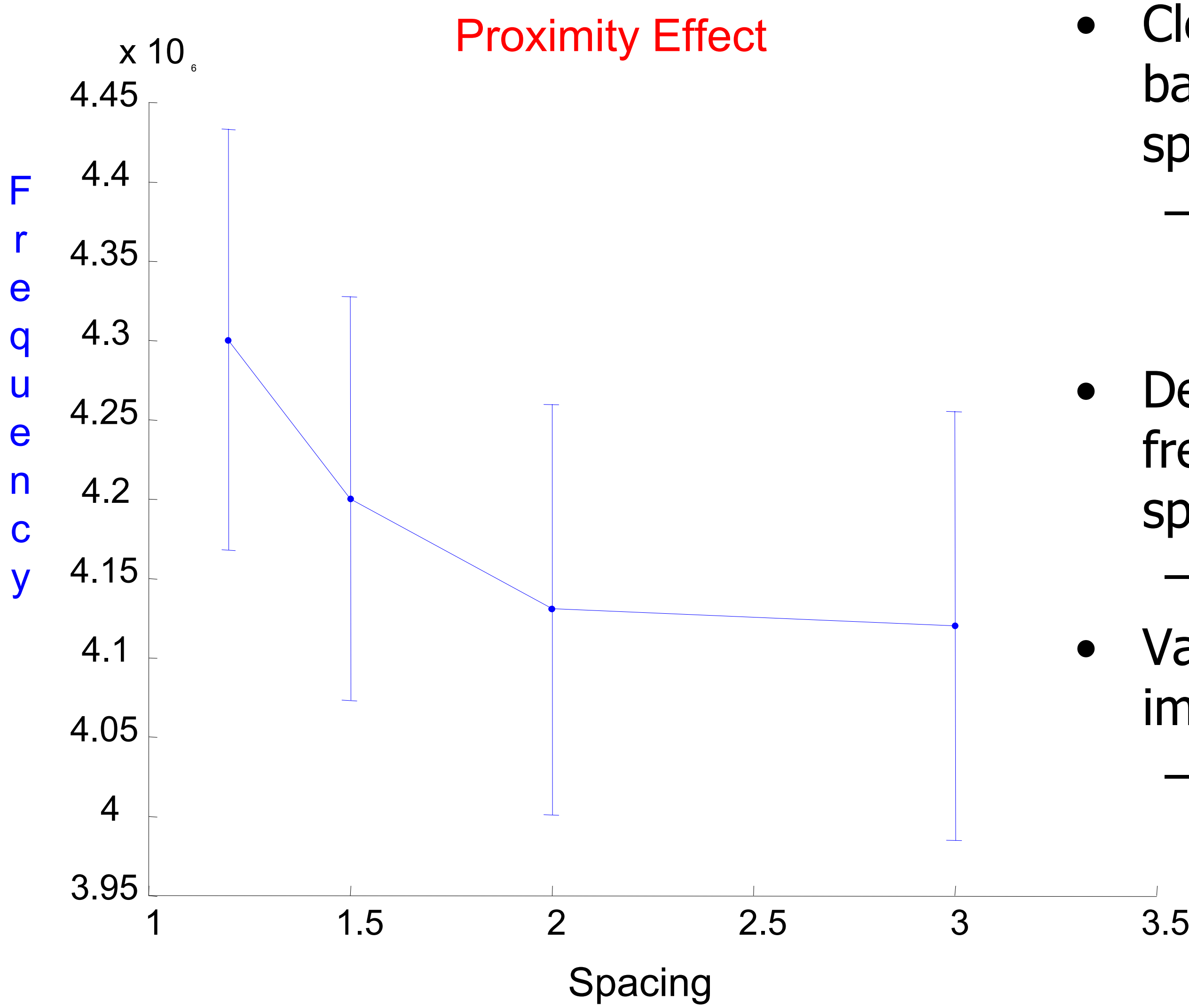
- Mean *f* = 4.42 MHz
- Total var: σ_f = 130 KHz (2.9%)
- Chip to chip var: σ_c = 122 KHz
- Within chip var: σ_w = 45 KHz

Poly Proximity Effect ROs



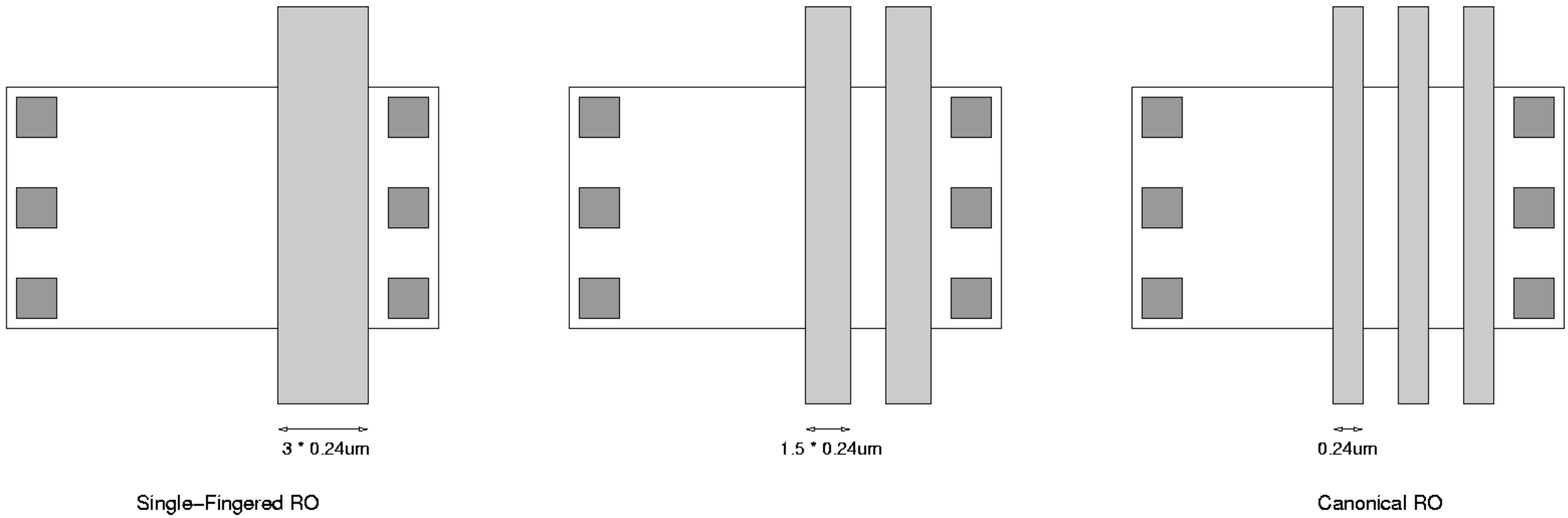
- Three finger P/N devices
- Minimum finger size (0.24 um)
- 1.2X, 1.5X, 2X, and 3X line spacing (0.40 um)

Poly Proximity Effect Results



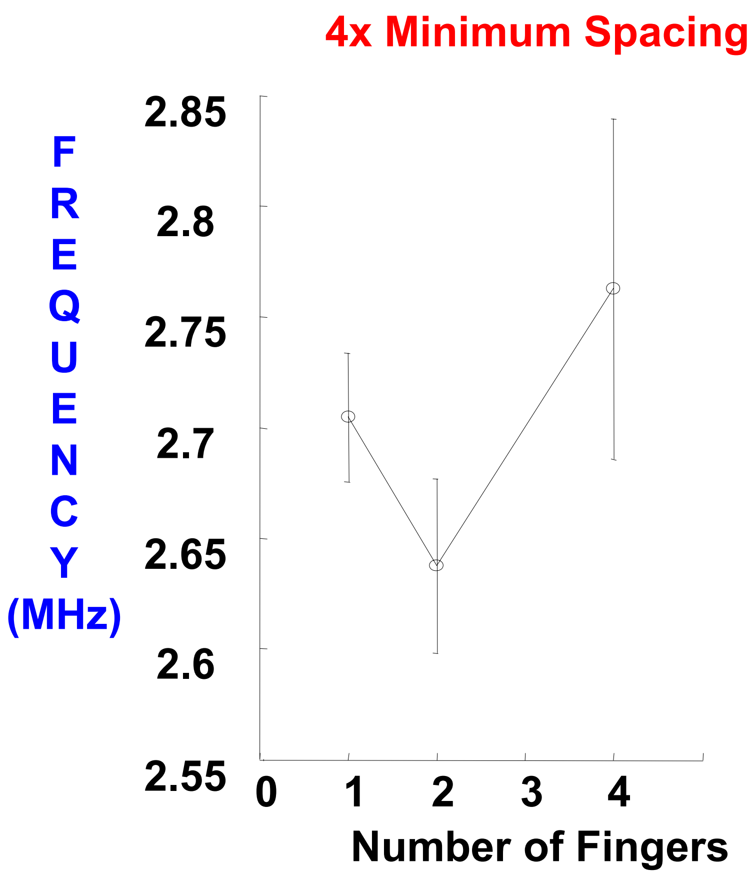
- Clear layout effect based on proximity or spacing between fingers
  - effect comparable to wafer level variation (0.2 vs. 0.3 MHz)
- Decreasing mean frequency as the gate space increases
  - L ↑ as S ↑
- Variance not strongly impacted by line space
  - i.e. within chip variation same for different RO spacing

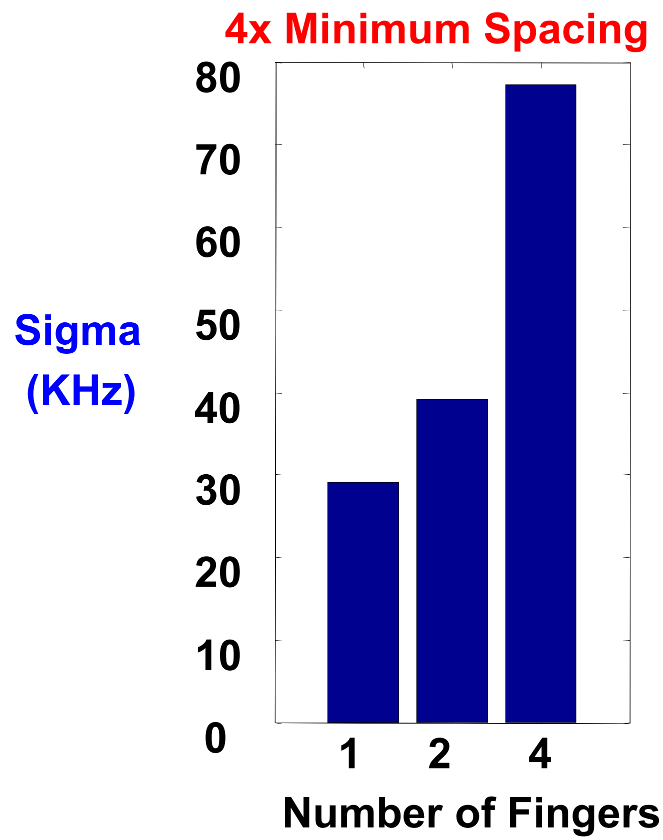
1/2/3 Fingered (Dense vs. Isolated) ROs



- Total L = 0.72 um
- Allocate gate length across 1, 2, or 3 fingers
- Expect single-fingered RO to be most robust to gate length variation

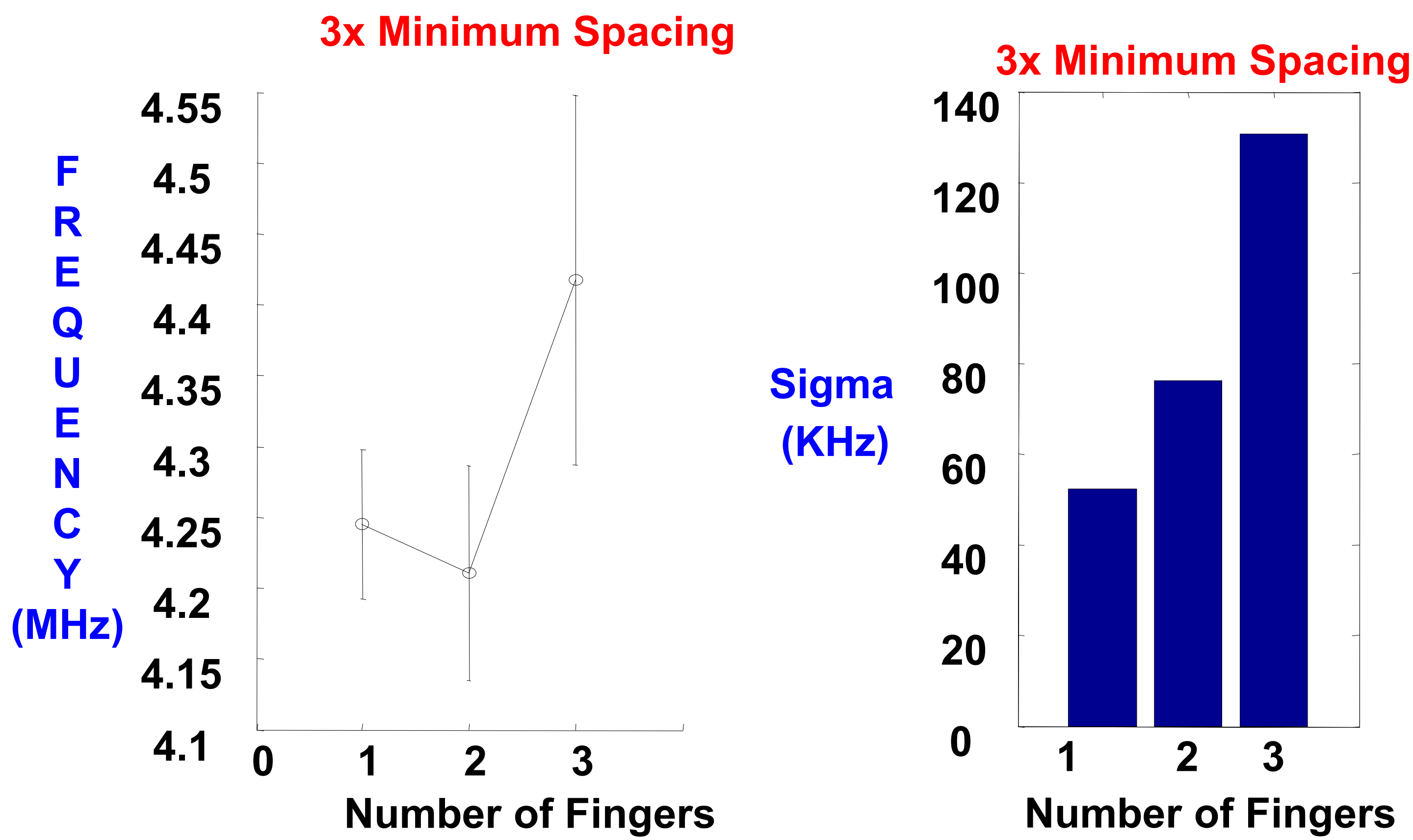
Dense vs. Isolated Structures





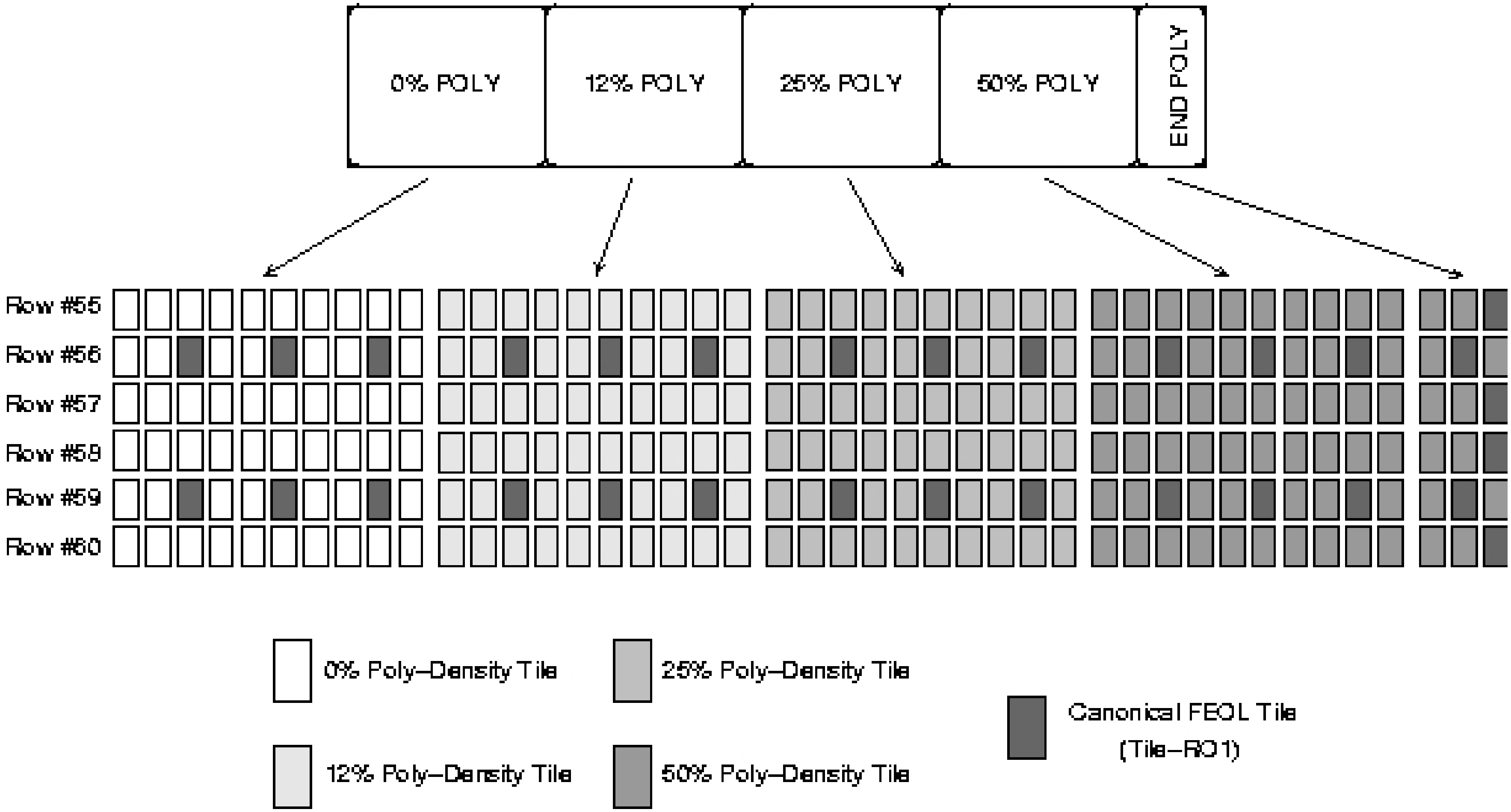
- Average RO frequency affected by # fingers
- Variance proportional to # fingers

Dense vs. Isolated Structures

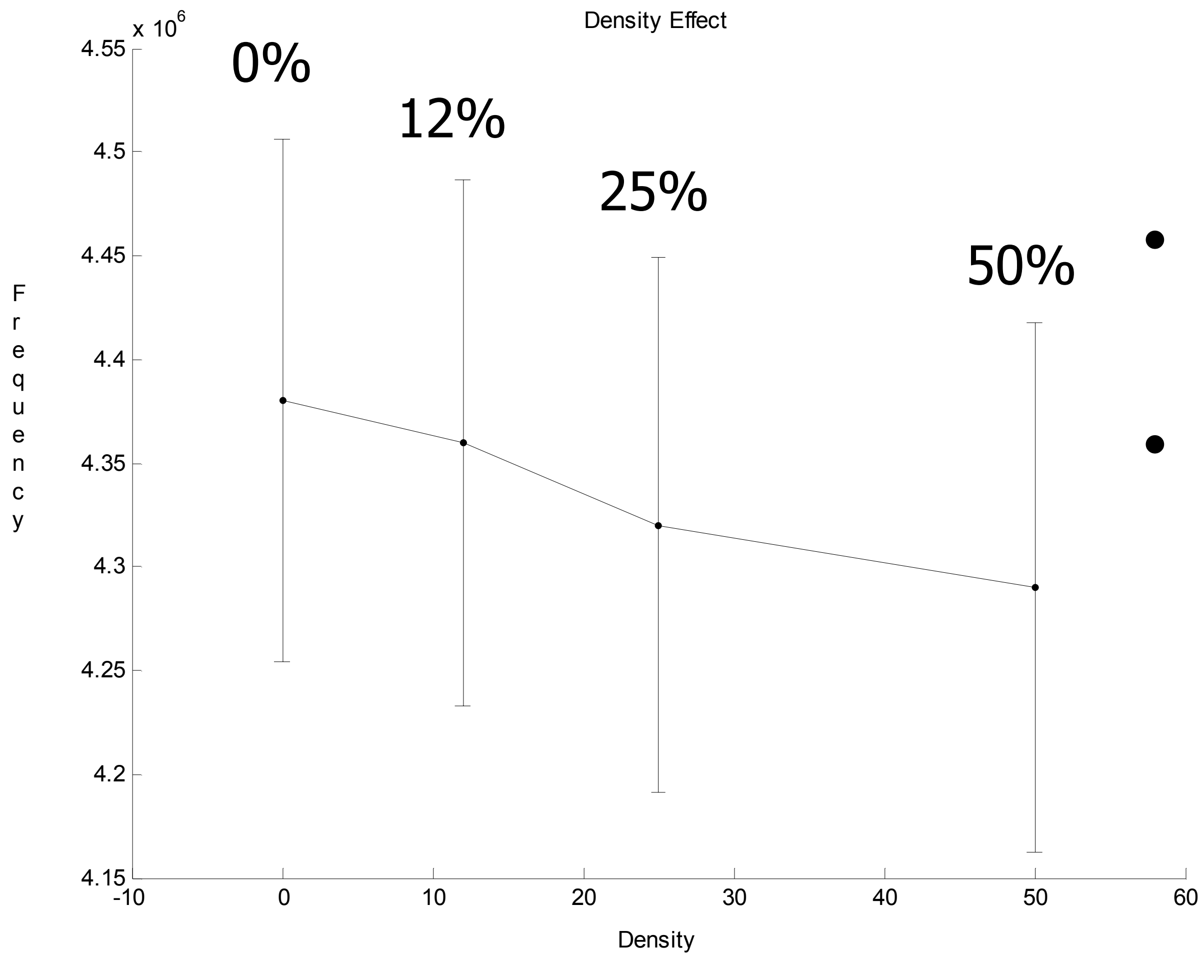


– Same effect seen at 3X minimum spacing
– Not clear: 1 vs. 2 finger effect signifance on *f*

Poly Density ROs

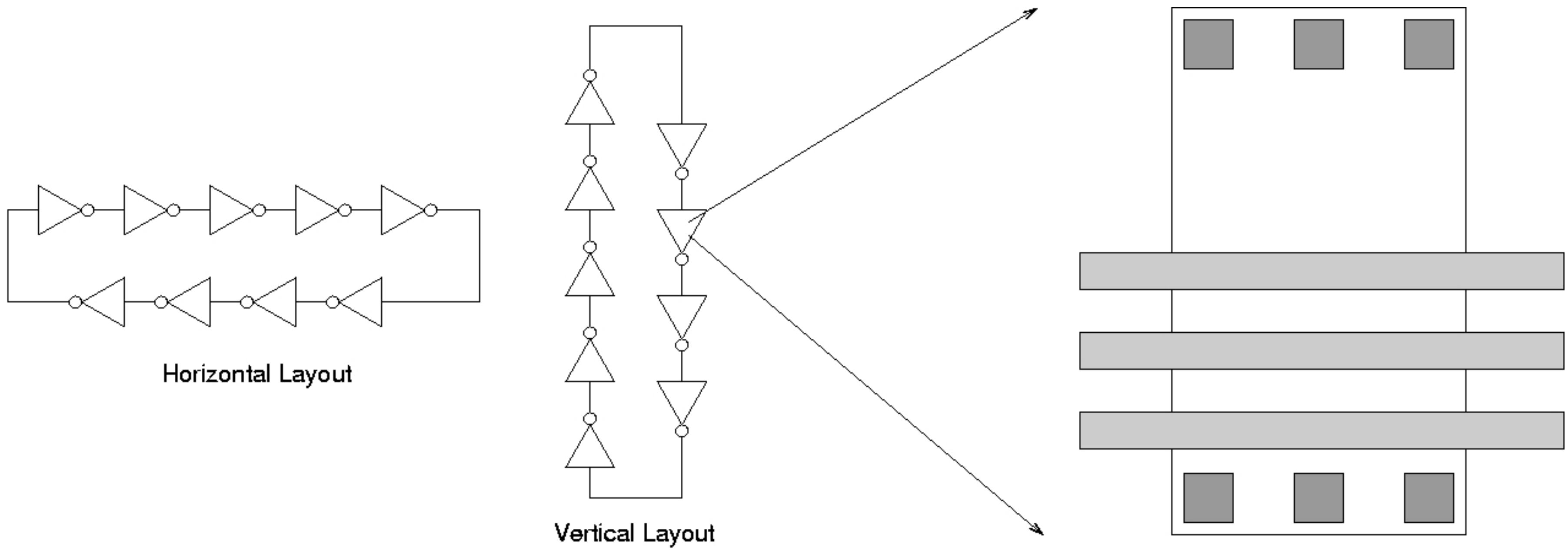


Poly Density RO Results



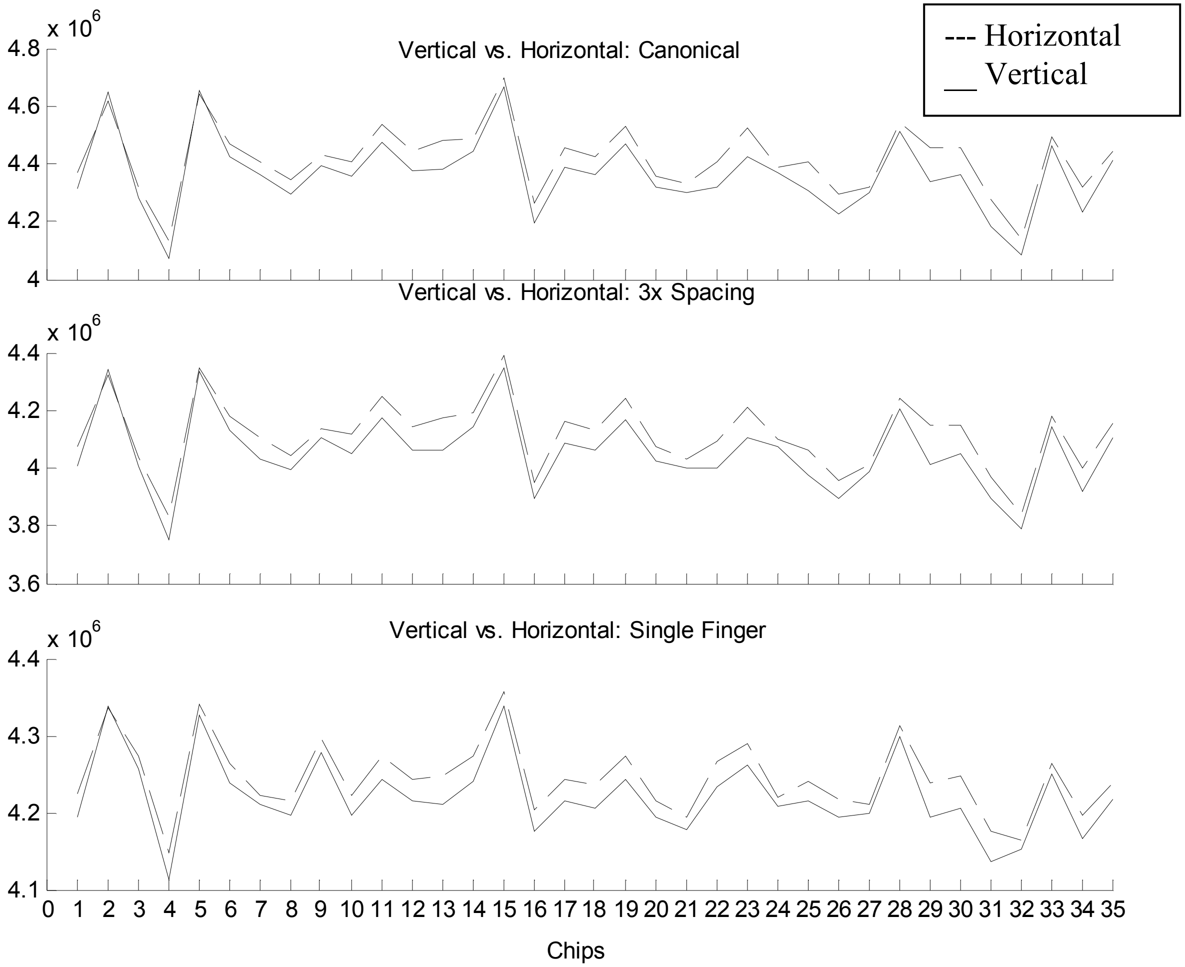
- Higher surrounding global poly density ⇒ slightly lower RO frequency
- Variance not strongly impacted by global poly density
- Effect is substantial: ~ 0.1 MHz

Vertical vs. Horizontal ROs



– Same layout, but RO's oriented vertically vs. horizontally
– Seek to detect any mask or process directionality bias

Orientation Results



Canonical:

f_{vert} = 4.36 MHz

f_{hor} = 4.42 MHz

3X spacing:

f_{vert} = 4.05 MHz

f_{hor} = 4.12 MHz

Single finger:

f_{vert} = 4.22 MHz

f_{hor} = 4.25 MHz

- Small but consistent offset with orientation

Separation of L vs. V_T Variation

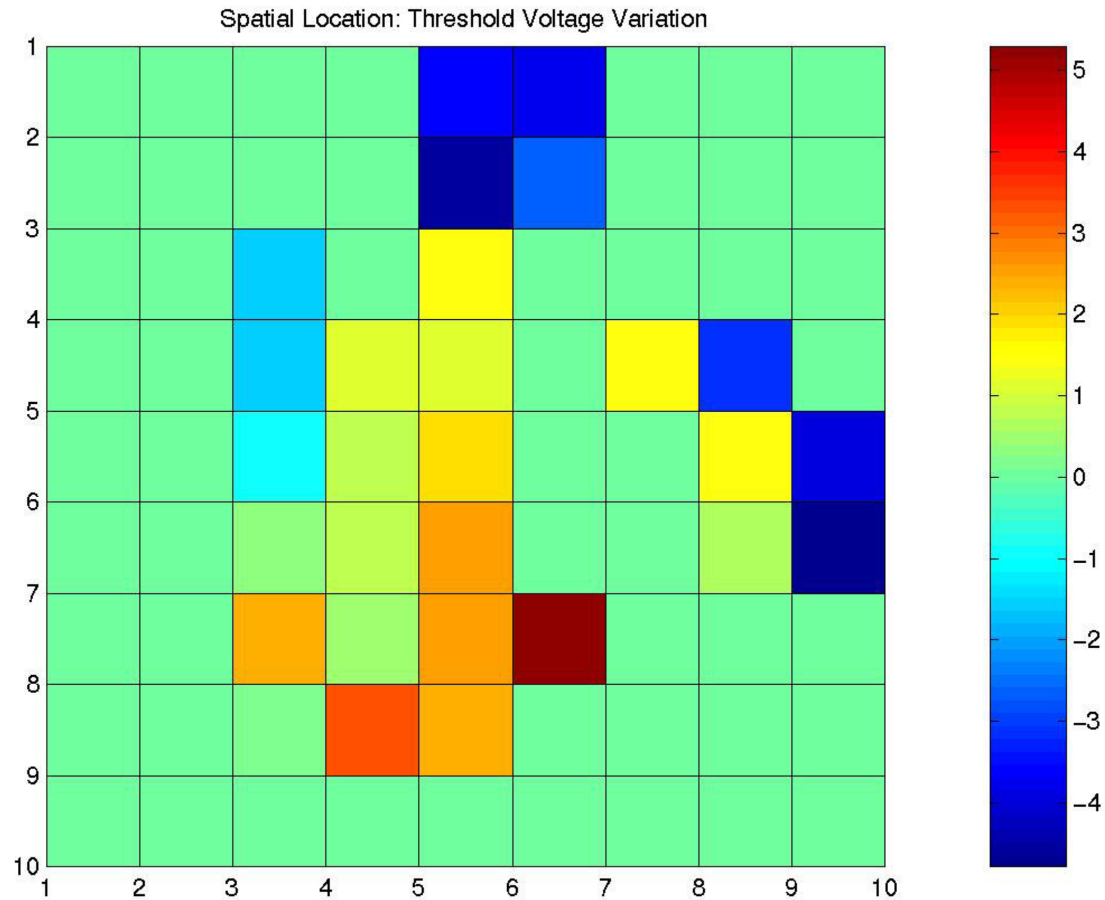
- Goal: identify variation due to channel length (ΔL) and threshold voltage (ΔV_T)
- Approach: Use RO frequency data at V_{DD} = 1V and V_{DD} = 2.5 V and recognize $f_{RO} \sim R_{on}$

$$R_{on} \sim \frac{1}{V_{gs} - V_T} \mu C_{ox} \frac{W}{L} \approx \frac{1}{V_{gs} - V_T - \Delta V_T} \mu C_{ox} \left(\frac{W}{L + \Delta L}\right)$$

  - At V_{DD} = 2.5 V, V_T variation small compared to V_{gs} so most variation is due to ΔL
  - At V_{DD} = 1 V, V_T variation more important, but ΔL variation is fixed to that observed at 2.5 V

V_T Variation Across Wafer

- Further simplification:
  - pick canonical devices with matched f_{RO} at $V_{DD} = 2.5V$
  - these RO's should have approximately equal ΔL's
- V_T vs. C_{ox} variation not clear

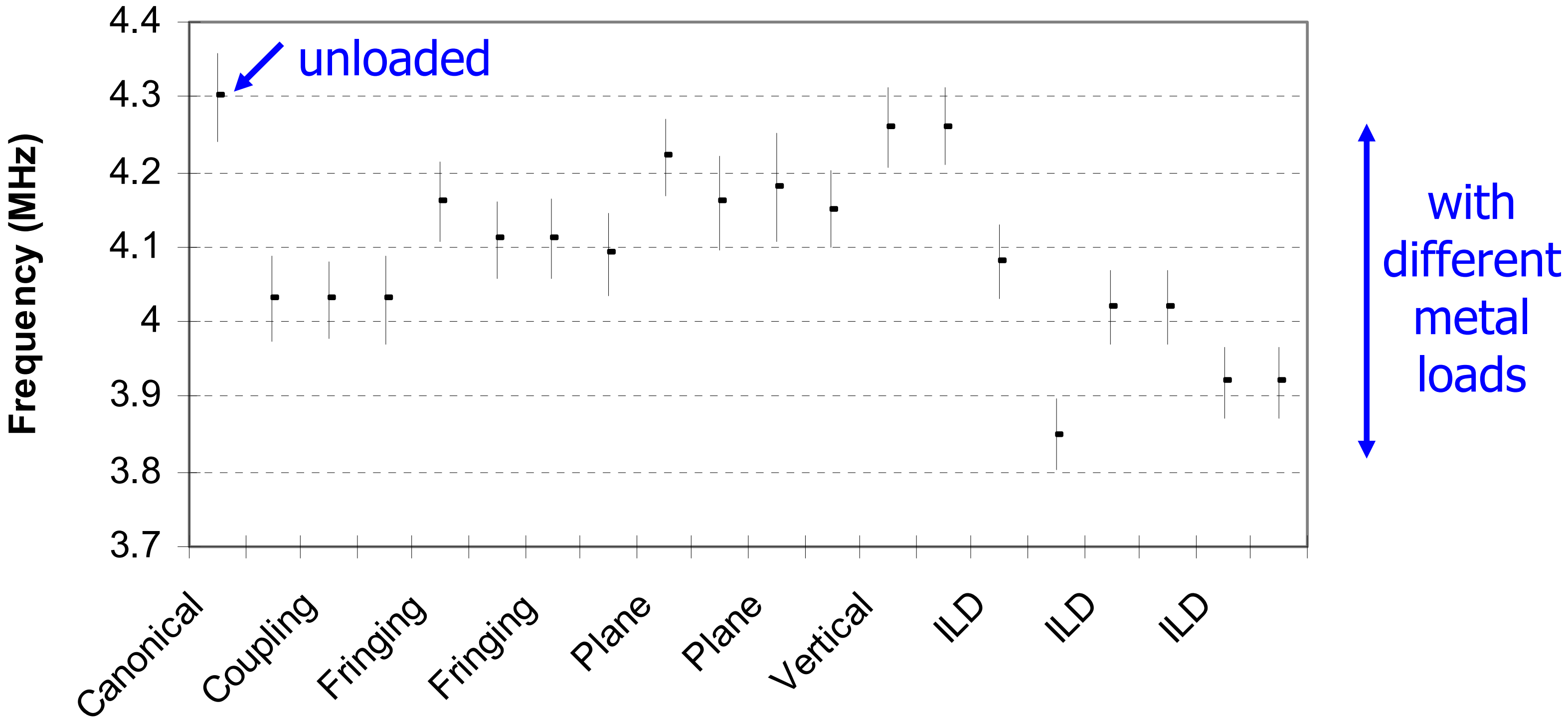


Chip % Variation in V_T

Overall Results BEOL Structures

CapType	Describption	Mean [MHz]	σ Total [KHz]	σ wafer [KHz]	σ within-chip [KHz]
Canonical	BEOL Canonical	4.30	58.3	49.3	31.2
Coupling	Coupling, M1	4.03	57.0	48.5	30.0
	Coupling, M2	4.03	51.6	46.8	21.8
	Coupling, M3	4.03	59.2	48.5	34.0
Fringing	M1 over Substrate	4.16	52.6	47.9	21.7
	M1 over Poly Ground	4.11	51.1	47.3	19.3
	M2 over M1 Ground	4.11	53.0	46.4	25.7
	M3 over M2 Ground	4.09	55.9	46.7	30.7
Plane	Plane M1 over Substrate	4.22	51.7	48.9	17.0
	Plane M1 over Poly	4.16	62.8	48.7	39.8
	Plane M2 M1 Ground	4.18	72.5	46.5	55.5
	Plan M3 M2 Ground	4.15	50.3	46.8	18.3
Vertical	Vertical BEOL	4.26	53.3	48.5	22.1
vs. Horiz	Horizontal BEOL	4.26	50.9	48.4	15.6
ILD	ILD1	4.08	50.6	47.2	18.4
	ILD2	3.85	46.3	44.3	13.5
	Large M1 Plane, Square	4.02	49.6	47.2	15.3
	Large M1 Plane, Rectangle	4.02	50.8	45.8	22.2
	Large M2 Plane, Square	3.92	47.7	45.6	14.0
	Large M2 Plane, Rectangle	3.92	47.2	45.2	13.5

RO Frequency for Different BEOL Structure Types



- Plot mean ± 1 σ_f (chip to chip + within chip spatial variation)
- Can measure mean for structure (e.g. M1 vs. M2 plane caps)
- Detecting variability due to metal structures more difficult

BEOL Variation

- Observability of BEOL capacitance variation ~1/10th that of FEOL variation:
  - BEOL canonical (unloaded): f = 4.30 MHz
  - BEOL square plane (loaded): f = 4.02 MHz
  - So "full range" of loading effect is ~0.30 MHz
  - Variation within that range smaller (e.g. ~10 kHz)

- Additional challenge in separating geometric variation sources from overlap, fringing, and coupling caps frequency measurements

Conclusions

- Variation test chip approach can detect susceptibility to variations related to layout
- Scan-chain control architecture can be used to obtain replicated information to extract sources of variation
- Key variation sources can be identified:
  - Device channel length – number of fingers, finger orientation, finger spacing
  - Both chip to chip (wafer scale) and within chip spatial trends can be mapped
  - Interconnect variations are challenging to detect