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Pattern Dependent Modeling of Electroplated Copper Profiles

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Abstract

Copper electroplated profiles exhibit pattern dependent topography. We propose a methodology for the characterization and modeling of feature scale copper step heights and the height of copper array regions, as a function of layout parameters. The resulting empirical models with parameters extracted from conventional and super fill plating processes capture several key trends important in electroplating, and are the first step toward an integrated chip-scale copper plating/CMP simulation capability.

Introduction

Electroplating is a key process in advanced copper metallization. Due to the layout patterns of the underlying trenches to be filled, non-uniform topography exists after plating. The resulting topography can be characterized by two parameters: a feature scale step height (SH) and an array height (AH) -- either recess or bulge -- as shown in Fig. 1. Case 1 shows a conventional fill profile while case 2 shows a super fill in which the plated copper above the isolated line and in the array region are both higher than in the surrounding field region. AH is measured with respect to the flat copper field region over wide oxide, and SH is the distance upward from the middle of the copper surface above a single copper line to the middle of the copper surface above a neighboring oxide space.

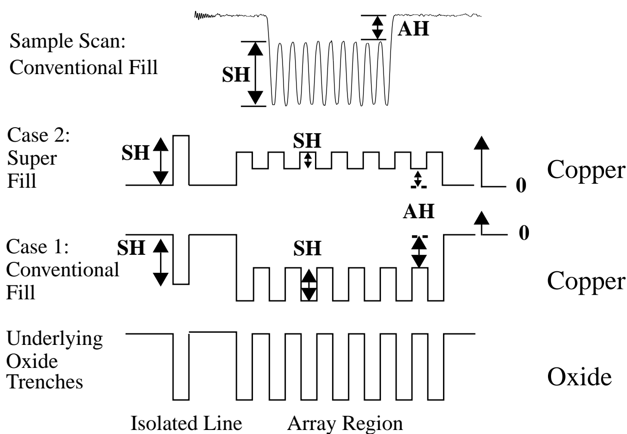

Figure 1. Electroplated Copper Profiles

To characterize these plating pattern dependencies, we propose the following methodology summarized in Fig. 2. We prepare wafers using a test mask having various pattern features, electroplate the patterned wafers with copper, and measure the line step height and the array height. An empirical model is proposed to capture the dependency on layout pattern factors; the model is fitted to the data for extraction of the model parameters. Once these model parameters are obtained, the model can be used to predict the surface non-uniformity of other layouts, enabling chip-level plating simulation.

In the subsequent chemical mechanical polishing (CMP) of electroplated copper wafers, pattern dependencies are well known to exist. The CMP of plated profiles depends not only on the layout patterns, but also on global and local step heights, including the pre-CMP non-uniform topography [1, 2]. The electroplating deposition model proposed here can be integrated with a copper CMP model to account for the initial non-uniform topography and its influence in polishing.

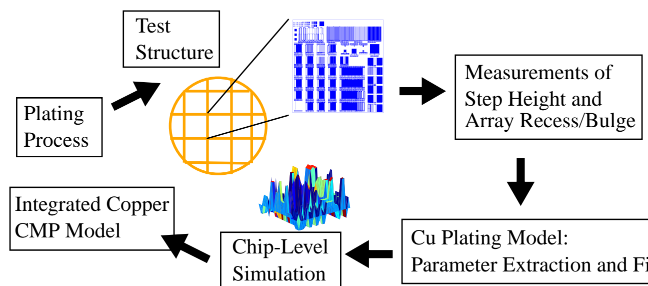

Figure 2. Copper Deposition Model and Integration with CMP Model

Test Pattern Description and Experimental Conditions

Test wafers previously used for the study of copper CMP are applied here to understand pattern dependencies of electroplated copper topography. The fundamental test structure consists of an isolated line and an array region as shown in Fig. 3. The “isolated line” on the left is used to study the plated profile for a line that is not influenced by nearby lines or patterns. The “array” region gives information about neighbor structure interactions for both the local feature scale copper step height as well as the array recess or bulge.

The entire array structure is relatively large in size (~1000 x 1000µm or more), and is separated from the isolated line by 200µm or more and from the next test structure by substantial oxide spacing of 500µm to decouple interactions among structures and provide a large field oxide area to serve as a measured surface profile reference point.

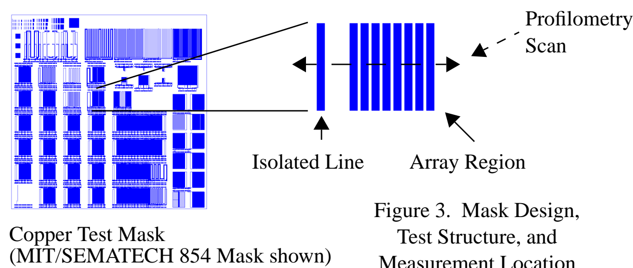

Figure 3. Mask Design, Test Structure, and Measurement Location

These test structures are laid out on a mask with various line width and line space combinations ranging from submi-

cron to several hundred micron wide geometries. In this study, we have used three different mask patterns, MIT/SEMATECH 954 and 854, and SKW6-2, plated using a variety of processes as summarized in Table 1. Our purpose is not to compare and contrast different plating processes, but rather to develop a single modeling framework that can capture the pattern dependencies across a wide range of plating processes. The center die for plated wafers are measured with a Veeco Vx Atomic Force Profiler for the 854 wafers and with a KLA-Tencor P10 for 954 and SKW6-2 wafers.

TABLE 1. Copper Electroplated Wafer Types

Wafer Type	Plating Tool	Recipe
A: SKW6-2	Semitool	Conventional Fill
B: MIT/SEMATECH 954	Semitool	Conventional Fill
C: MIT/SEMATECH 854	Novellus	Super Fill 1
D: MIT/SEMATECH 854	Novellus	Super Fill 2

Pattern Dependencies

As defined earlier, the pattern induced step height (SH) and array height (AH) are examined against key pattern factors of line width, line space, ratio of line and space, density of metal lines, and pitch, to determine the key layout parameter of influence. We have found that both are primarily dependent on feature size parameters: SH is most strongly influenced by line width, and AH by line space as shown in Fig. 5 for the 954 wafer. We note a critical line width L_S^* and critical line space L_A^*, beyond which SH and AH become the initial oxide trench step height and 0Å, respectively; these are summarized in Table 2. Electroplating pattern effects seem to occur on a relatively short range (below ~5-10µm). Similar trends are shown in Fig. 6 and Fig. 7 for the 854 wafers with super fill. In the case of super fill, the SH for small lines is positive and has a maximum at around 1µm line width and decreases with wider lines where SH then behaves as in the conventional fill. Similarly, in the super fill case the AH is positive for small line spaces and then becomes negative before it saturates to 0Å as the line spaces increase.

TABLE 2. Critical Line Width and Line Space for SH and AH

Wafer Type	Critical Line Width for SH (L_S^*)	Critical Line Space for AH (L_A^*)
A	5µm	1.5µm
B	5µm	2.5µm
C	10µm	3µm
D	10µm	5µm

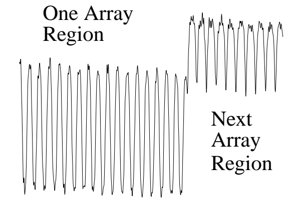

Figure 4. Nearest Neighbor Effect

The electroplating depends on more than just the dimension of the line being filled; rather, there is some interaction with other nearby structures. This is clearly captured in Fig. 7b where a range of SH values for a fixed line width of 1µm are shown as a function of line space: as the line space increases, SH increases and saturates at about 2400Å which is close to the isolated line SH. This neighbor interaction is also shown in the array line SH (in Fig. 7a) for the 50µm and 100µm line width: the SH is different for line spaces of 1µm and 100µm.The same observation is also seen in Fig. 6a.

The profile data seem to indicate comparable results for array height for a single space (between two lines) as for a whole array of lines. The fill may only depend on the "nearest neighbor" rather than on a longer range neighborhood; this is seen by the rapid transition between different patterned regions in Fig. 4. Further study is needed to confirm this lack of longer range array height dependency.

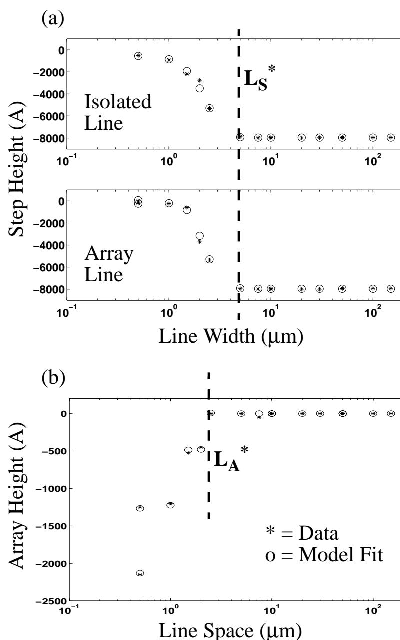

Figure 5. Wafer B: 954 Patterns with Conventional Fill

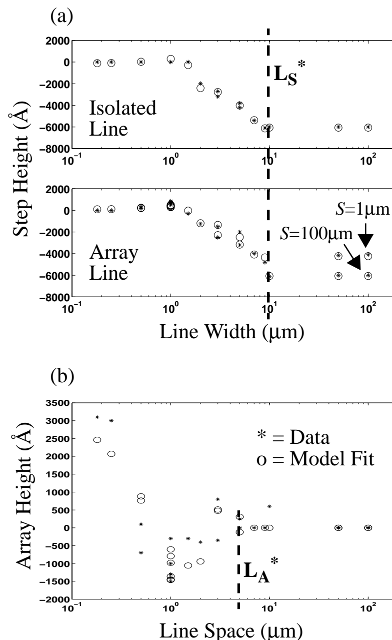

Figure 6. Wafer D: 854 Patterns with Super Fill 2

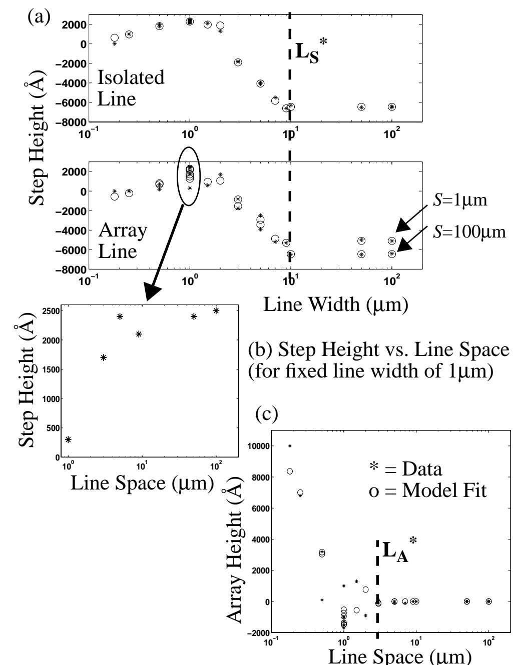

Figure 7. Wafer C: 854 Patterns with Super Fill 1

Model Formulation and Fit

In previous pattern dependent studies for spin-on resist deposition thickness by Wilson et al. [3], and for film thickness in CMP by Stine et al. [4], a strong "pattern density" dependence (calculated over some characteristic length) was observed. Such a pattern density dependent model does not appear suitable for electroplating. Instead, an empirical model structure is used to fit the electroplating data as described in Eq. 1 and Eq. 2 for SH and AH, with a polynomial dependence on line width (*W*) and line space (*S*) with terms up to third order. The higher order terms are needed to capture non-linear trends, and the (*W*x*S*) term captures line width and space interactions.

For the conventional fill, the model framework captures the overall trends of SH and AH well as seen in Fig. 5. As the t statistics indicate, *W* is the most significant factor for SH, and both *W* and *S* terms (and their interaction) are highly significant for AH. For the super fill, step height is reasonably captured with both *W* and *S* terms being significant (SH data are fitted separately in two regions: positive step height and negative step height). However, the array height is not fully captured by our polynomial structure (although *S* and higher order terms are significant as expected). There may be other factors such as $(1/S)$ or α^S terms that might better capture the trends. Further research into the physics of electroplating such as presented in [5] or [6] is needed to further refine the chip-scale empirical model presented here.

$$\text{SH} = a_S W + b_S S + c_S W^2 + d_S W^3 + e_S W \times S + Const_S \quad \text{(Eq. 1)}$$

$$\text{AH} = a_A W + b_A S + c_A S^2 + d_A S^3 + e_A W \times S + Const_A \quad \text{(Eq. 2)}$$

TABLE 3. Model Parameters and Fit

Coeff.	Value	Std. Error	t value	Pr(>|t|)
Wafer B: 954 Step Height, R^2 = 0.9908, RMS Error = 350Å				
a_S	3330.5468	1138.4028	2.9256	0.0191
b_S	-194.1732	321.1198	-0.6047	0.5621
c_S	-2648.8828	683.4601	-3.8757	0.0047
d_S	367.6420	87.3179	4.2104	0.0030
e_S	-240.4325	294.6044	-0.8161	0.4381
$Const_S$	-815.4056	699.7888	-1.1652	0.2775
Wafer B: 954 Array Height, R^2 = 0.9988, RMS Error = 60Å				
a_A	-1060.5263	95.9512	-11.0528	0.0574
b_A	478.9474	364.8078	1.3129	0.4144
c_A	52.6316	171.7546	0.3064	0.8107
d_A	Not Used:			
e_A	389.4737	49.2147	7.9138	0.0800
$Const_A$	-1084.2105	201.5092	-5.3805	0.1170
Wafer C: 854 Step Height, R^2 = 0.8852, RMS Error = 371Å				
For Positive Step Height: $W <= 2\mu m$				
a_{S1}	7099.5612	2349.2004	3.0221	0.0073
b_{S1}	123.3652	41.7846	2.9524	0.0085
c_{S1}	-5595.3881	2601.4726	-2.1509	0.0453
d_{S1}	1342.3557	799.9280	1.6781	0.1106
e_{S1}	-10.8618	41.6222	-0.2610	0.7971
$Const_{S1}$	-1692.2545	575.3562	-2.9412	0.0087

TABLE 3. Model Parameters and Fit

Coeff.	Value	Std. Error	t value	Pr(>|t|)
For Negative Step Height: $W > 2\mu m$				
a_{S2}	-603.8774	897.3893	-0.6729	0.5162
b_{S2}	-101.9551	44.2355	-2.3048	0.0439
c_{S2}	-126.4638	152.2688	-0.8305	0.4256
d_{S2}	11.8412	7.9479	1.4899	0.1671
e_{S2}	-4.8234	5.8907	-0.8188	0.4320
$Const_{S2}$	1895.1137	1633.9947	1.1598	0.2731
Wafer C: 854 Array Height, R^2 = 0.8583, RMS Error = 1645Å				
a_A	-155.8631	315.0456	-0.4947	0.6341
b_A	-25544.3223	6990.4198	-3.6542	0.0065
c_A	15364.8498	5490.0936	2.7986	0.0232
d_A	-2750.2056	1150.3734	-2.3907	0.0438
e_A	50.1974	211.7486	0.2371	0.8186
$Const_A$	12508.0770	2089.8967	5.9850	0.0003
Wafer A: SKW6-2 Step Height, R^2 = 0.9944, RMS Error = 234Å Wafer A: SKW6-2 Array Height, R^2 = 0.8864, RMS Error = 30Å				
Wafer D: 854 Step Height, R^2 = 0.6412, RMS Error = 292.5Å Wafer D: 854 Array Height, R^2 = 0.7735, RMS Error = 807Å				

Conclusion

We have shown step height and array height pattern dependencies for copper electroplated test structures. Primary data trends can be captured with line width and line space parameters for step height and array height, respectively. A polynomial model framework works well for step height of both conventional and super fill, but further extensions are needed to more fully capture array height/bulge dependencies for super fill. Characterization and model parameter extraction using patterned test masks are proposed as a step toward chip-scale modeling of electroplated pattern effects, leading to the integrated modeling of copper deposition and polishing processes.

Acknowledgements

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References

[1] T. Tugbawa, et al., "A Mathematical Model of Pattern Dependencies of Cu CMP Processes," Electrochem. Society Meeting, Hawaii, Oct. 1999.

[2] S. Hymes et al., "Evolution of Topography During First Step CMP of Cu-Plated Damascene Structures," CMP Symposium, Electrochemical Society Meeting, Honolulu, HA, Oct. 1999.

[3] R. H. Wilson and P. A. Piacente, "Effect of Circuit Structure on Planarization Resist Thickness," J. Electrochem. Society., Vol. 138, No. 2, Feb. 1991.

[4] B. Stine, et al., "Rapid Characterization and Modeling of Pattern-Dependent Variation in Chemical-Mechanical Polishing," IEEE Trans. on Semiconductor Manufacturing, Vol. 11, No. 1, Feb. 1998.

[5] H. Deligianni, et al., "A Model of Superfilling in Damascene Electroplating," ECS Meeting Abstracts, Vol. MA 99-1, pp. 267, 1999.

[6] K. Kobayashi, et al., "Trench and Via Filling Profile Simulations for Copper Electroplating Process," Proceedings of the IEEE Int'l Interconnect Technology Conf., pp. 34-36, June 2000.