Pattern Dependent Characterization of Copper Interconnect

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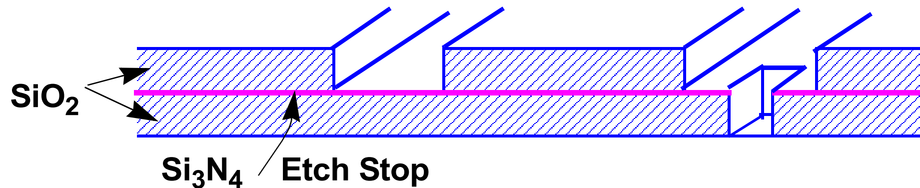
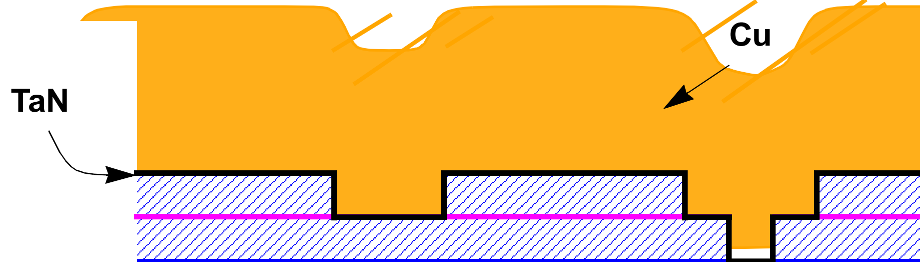
Copper Interconnect Dual Damascene Process

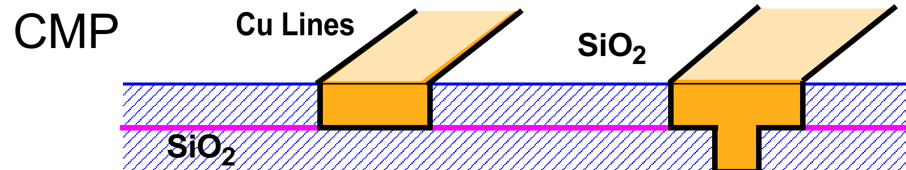
Deposit dielectric stack; Pattern trenches & vias



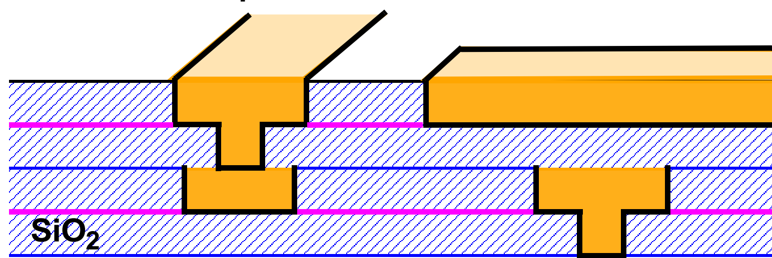
Barrier deposition; copper electroplating



CMP



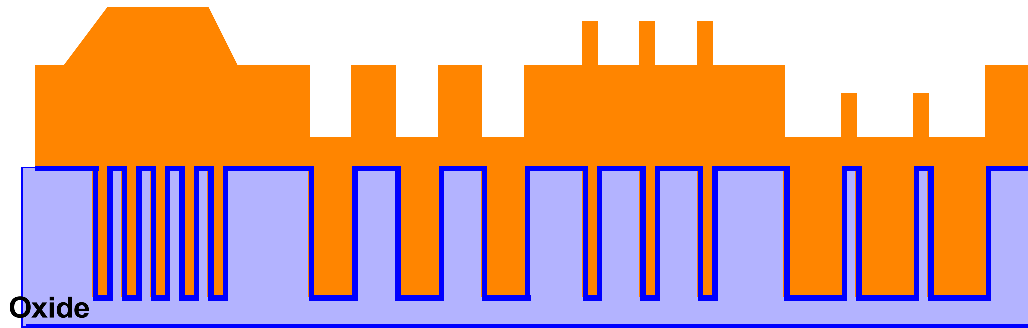
Repeat for multiple levels of metal



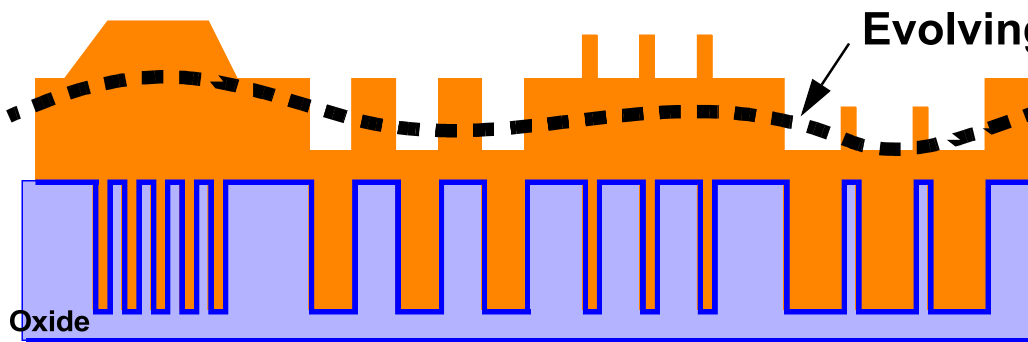
- Electroplating
  - "Superfill" used to fill narrow trenches and vias
  - Ideally: plated surface nearly flat
- Copper CMP
  - Multistep process to remove bulk copper and barrier metal
  - Ideally: polished surface nearly flat
    - no loss in copper wire thickness
    - flat for next level

Copper Interconnect Problems

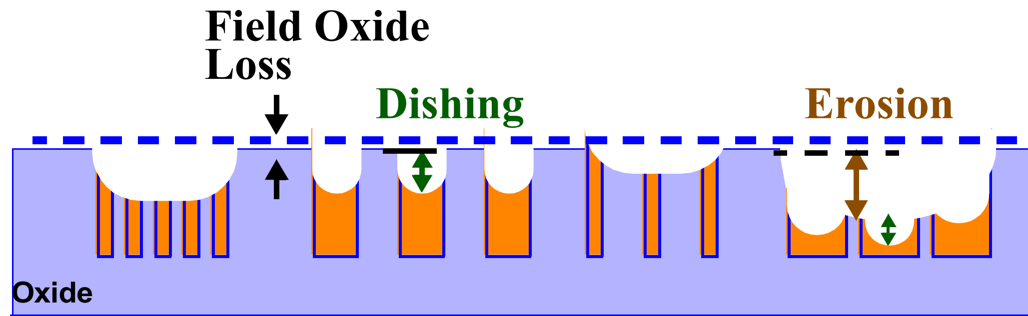
- Polishing stages: bulk polish, barrier polish, and overpolish



Non-uniform plating



CMP



Overpolish

CMP Process and Problems

Electroplating/CMP Characterization Methodology

Electroplating/CMP Test Wafers

- Plating: Measure step height, array bulge/recess and field copper thickness
- CMP: Measure dishing, erosion and field copper thickness

Model Parameter Extraction

Calibrated ECD Pattern Dependent Model

Calibrated Copper Pattern Dependent Model

Product Chip Layout

Electroplating Process

- Fixed plating recipe

CMP Process

- Fixed pad, slurry, process settings (pressure, speed, etc)
- Variable polish times

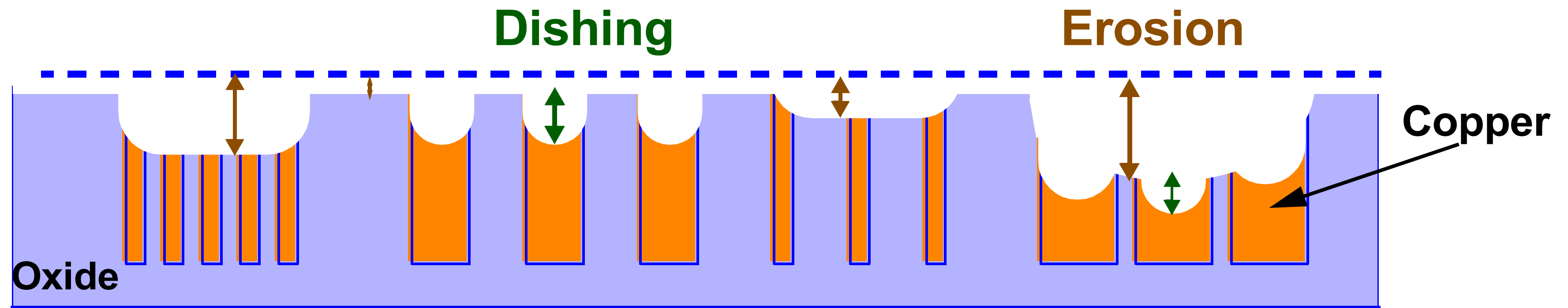
Chip-Level Simulation

- Plating: prediction of step height, array height, copper thickness and local pattern density
- CMP: prediction of clearing time, dishing and erosion, final copper line thicknesses

Outline

- Background
  - Pattern dependent effects in plating and CMP
- Copper CMP Characterization
  - Polishing Length Scales
  - Test Structure and Mask Design
    - Single Layer Test Structures and Mask Design
    - Multilevel Test Structures and Mask Design
  - Measurements and Analysis
  - Design Rule Generation
  - Chip Scale Modeling
- Copper Electroplating Characterization
- Conclusions

Copper CMP Pattern Dependent Effects



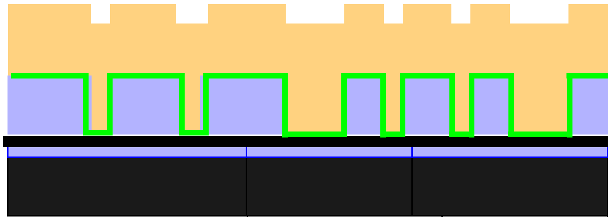
Sample Profilometer Scans

Line width = 1 μm
Line space = 1 μm

Line width = 9 μm
Line space = 1 μm

Polishing Length Scales

mm Range

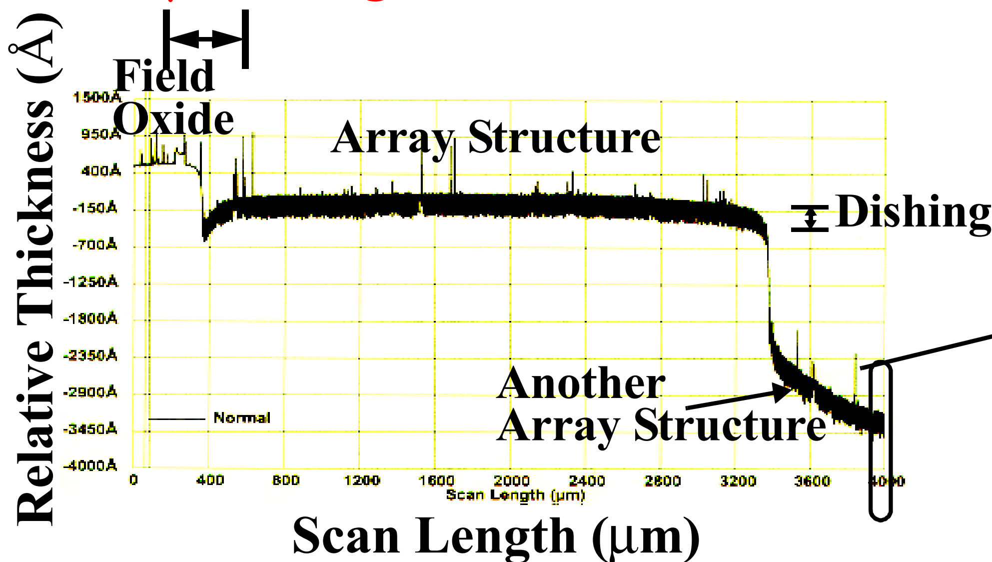


Initial Copper Polish

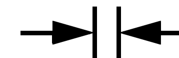
- Three Polishing Length Scales:
  - ~2mm range: copper bulk polish
  - ~100µm range: erosion profile
  - ~1µm range: dishing profile

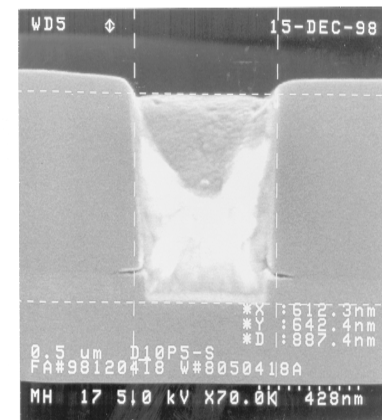
Barrier/Overpolish

~100µm Range



~1µm Range





SEM Cross Section
(0.5µm wide line)

Dishing and Erosion Test Structures

Typical erosion profilometry scan

Isolated Line

Array Region

50mm

2mm

500mm

500mm

2mm

1.0

1.0/2.0

Line width/line space mark

Physical Test Structure

Electrical Measurement

ΔV

0.5/4.5

Isolated Line

Dummy Line Region

2160mm

50mm

2200mm

ΔV

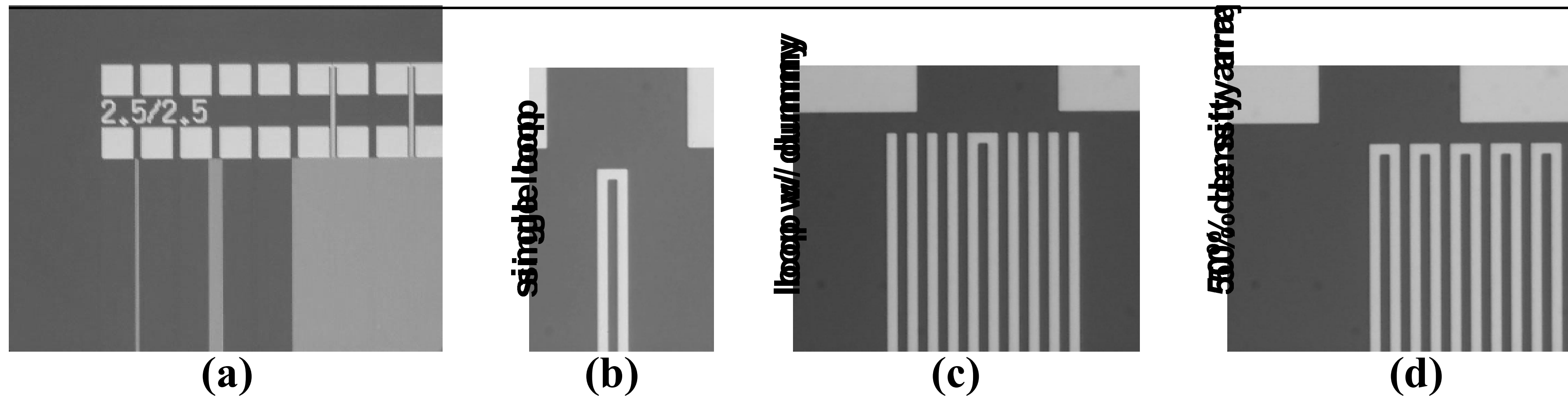
Array Region

Electrical Measurement

Electrical Test Structure

- Profilometry: captures surface height over long scans
- Electrical measurements: extract line thickness by probing

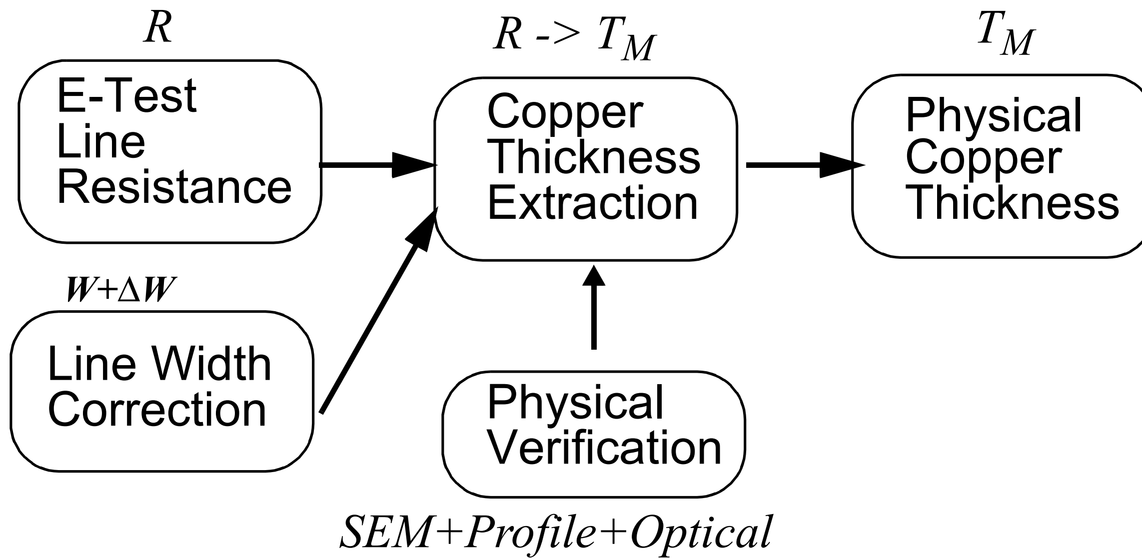
Dishing/Erosion Array Test Structures

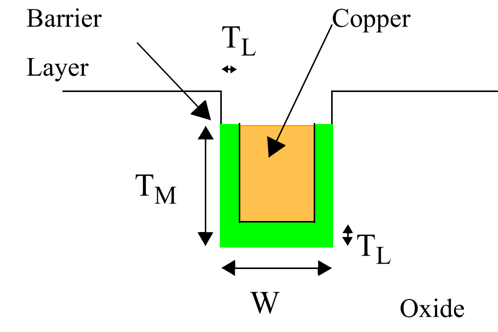


(a) (b) (c) (d)

- Three Regions:
  - b) Single loop: isolated line
  - c) Small array: loop with surrounding dummy lines
  - d) Large array: multiple taps along length of the array
- Electrical Sampling:
  - Each tap is a Van der Pauw structure: measure resistance
  - Uniform sampling: e.g. every 100 μm
  - Edge sampling: place more taps near the transition region

Copper Thickness Extraction Procedure





Simplified Profile

- R is measured line resistance
- ***Rs*** **(ρ/*t*)** is sheet resistance
- t is the thickness of a line
- ρ is the resistivity of copper
- L is the length of a line
- W is the width of a line.
- R_{Cu} is resistance due to copper
- R_L is resistance due to liner
- ρ_L is the resistivity of liner

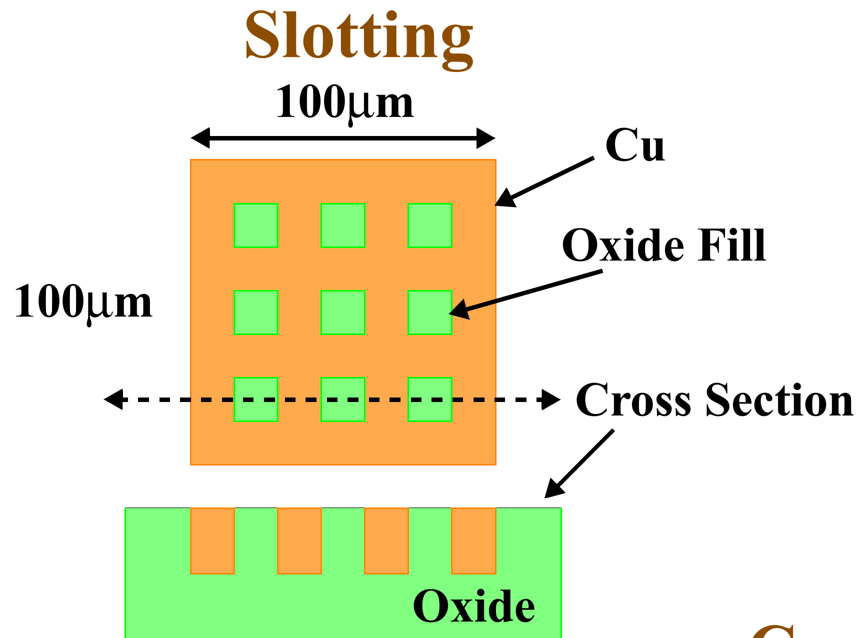
$$R = Rs \times \frac{L}{W} \quad \text{or by re-arranging variables} \quad t = \frac{\rho}{R} \times \frac{L}{W} \qquad (1)$$

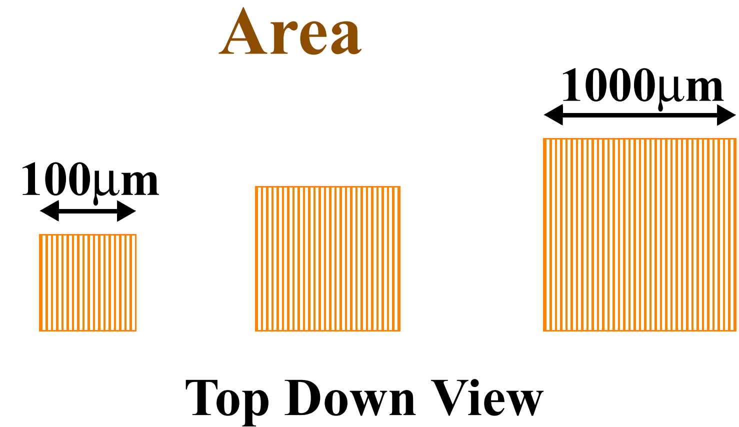
$$R_{Cu} = \frac{\rho_{Cu} \times L}{(T_M - T_L) \times (W - 2T_L)} \quad \text{and}$$

$$R_L = \frac{\rho_L \times L}{(2T_M \times T_L) + ((W - 2T_L) \times T_L)} \qquad (2)$$

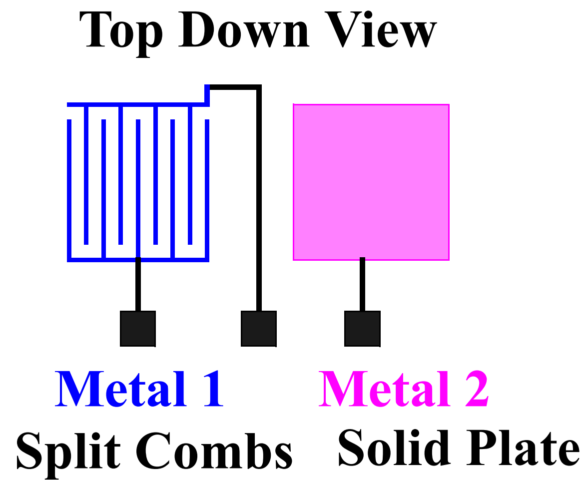
$$T_M = \frac{\rho_{Cu}}{R} \times \frac{L}{(W - 2T_L)} + T_L \qquad (3)$$

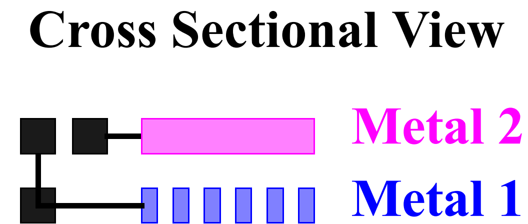
Additional Structures



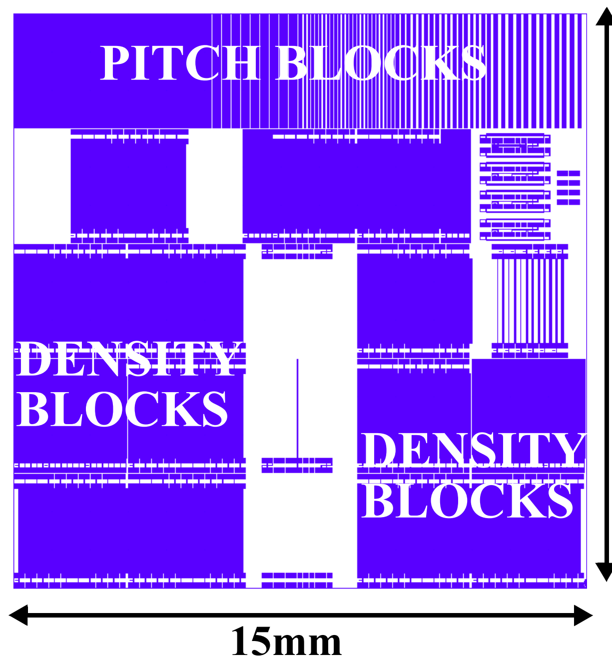


Capacitance

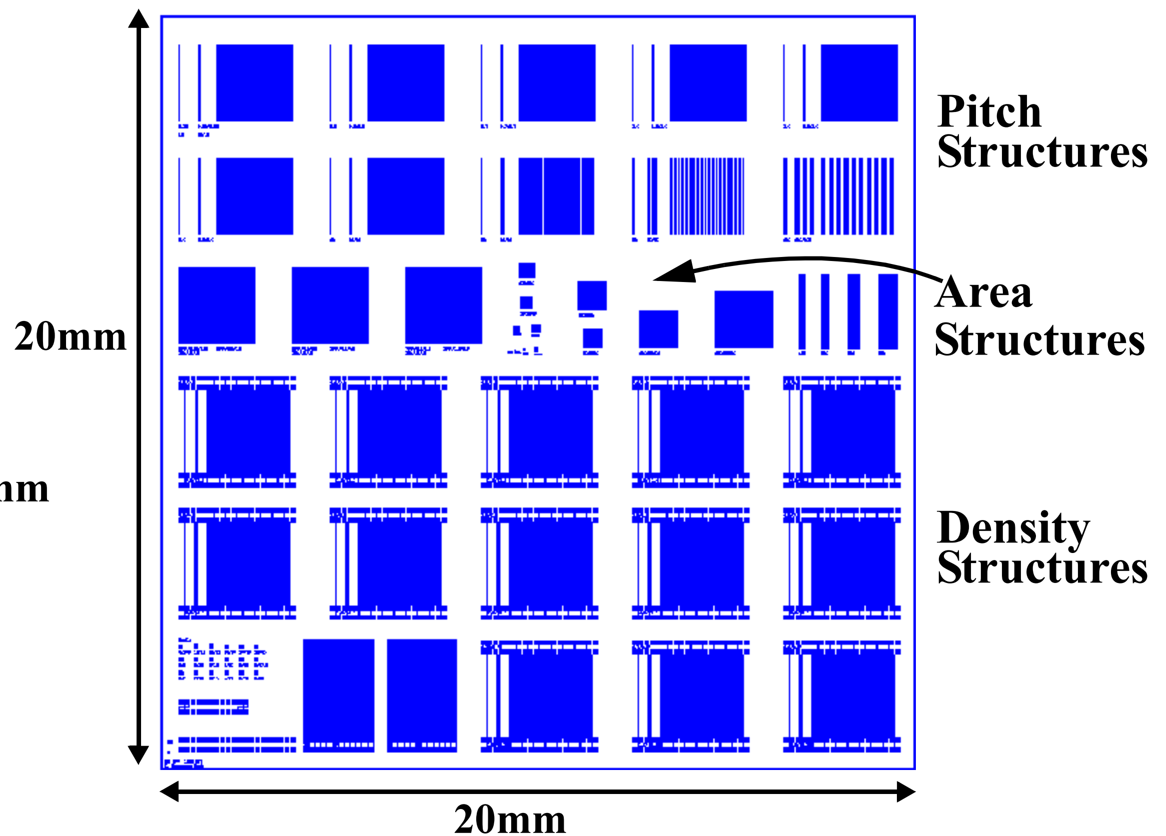




Single Layer Mask Designs



A. First Generation Mask
("SEMATECH 931 Mask")



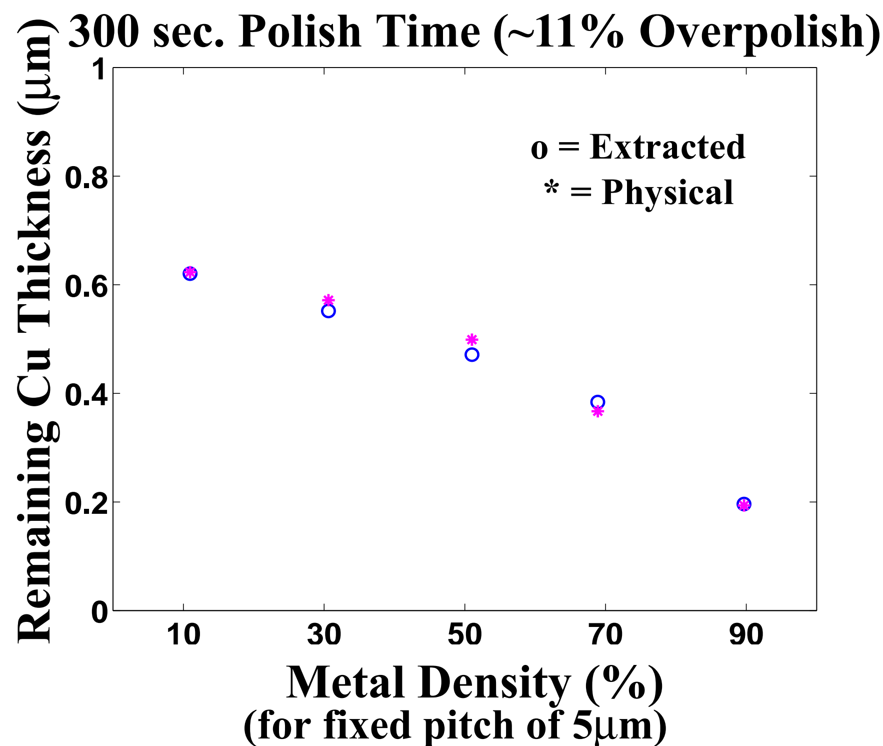
B. Second Generation Mask

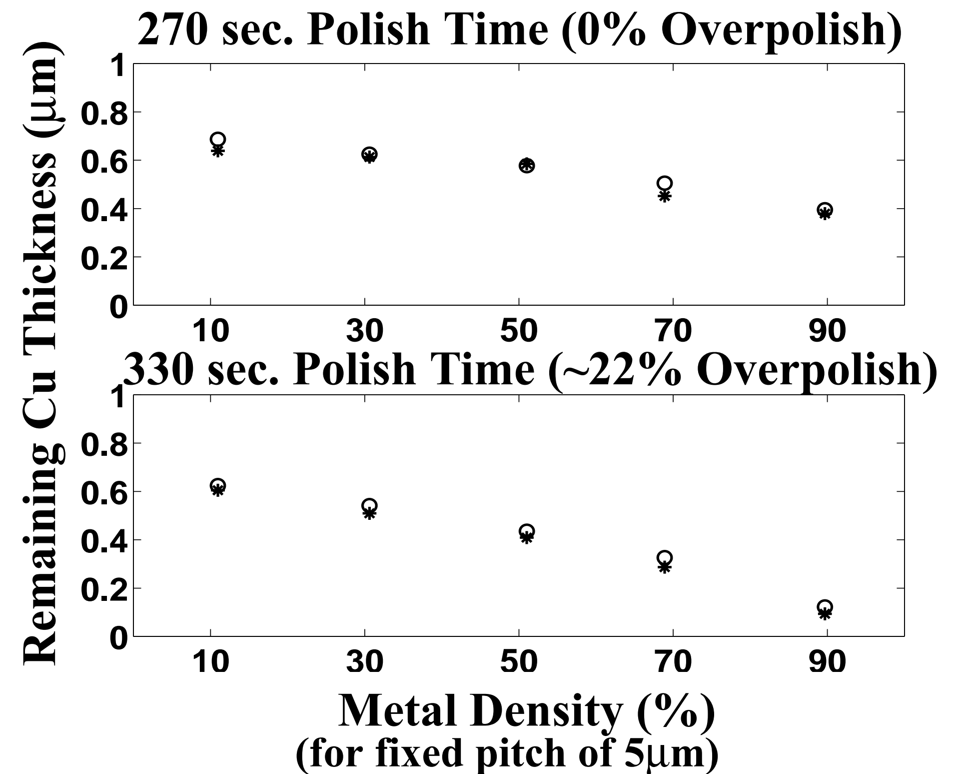
- Single-level mask: electrical and physical test structures.
- Key pattern factors: density and pitch and/or linewidth and linespace.
- Structure Interaction: structure size and floor planning.

Single Layer Surface Profiles and Trends

Surface Profiles (in Å)

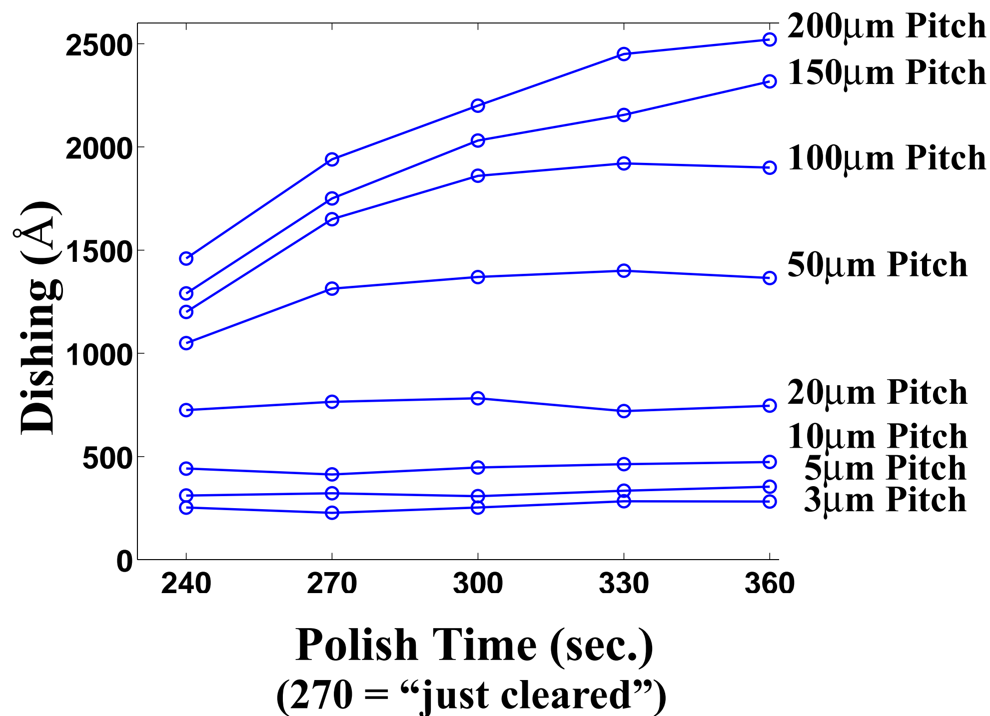
Extracted and Physical Copper Thickness

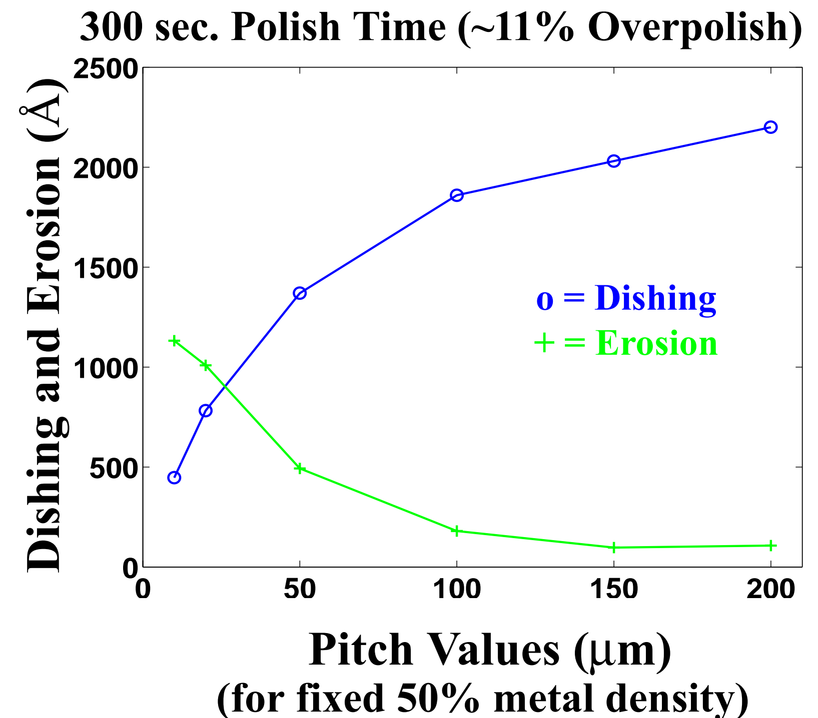




- Good correlation between extracted thickness and physical data.
- Clear trend of total remaining thickness is shown from the electrical data.

Analysis: Dishing and Erosion in Copper CMP

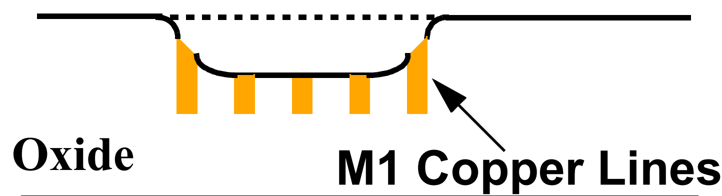




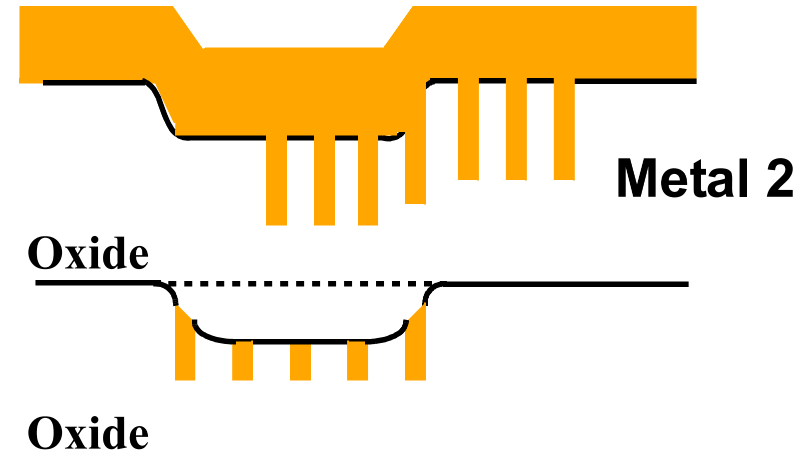
Dishing and Erosion Dependencies on Polish Time and Pitch

- Profilometry surface scan for dishing and oxide thickness measurement for erosion.
- Constant dishing after initial transition for smaller pitch structures.

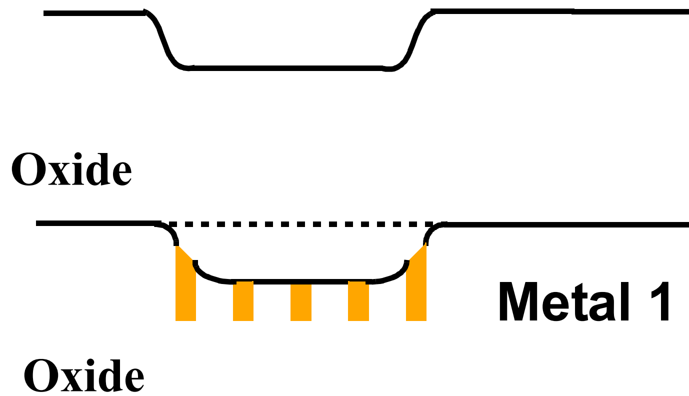
Multilevel Process Sequence and Pattern Problems



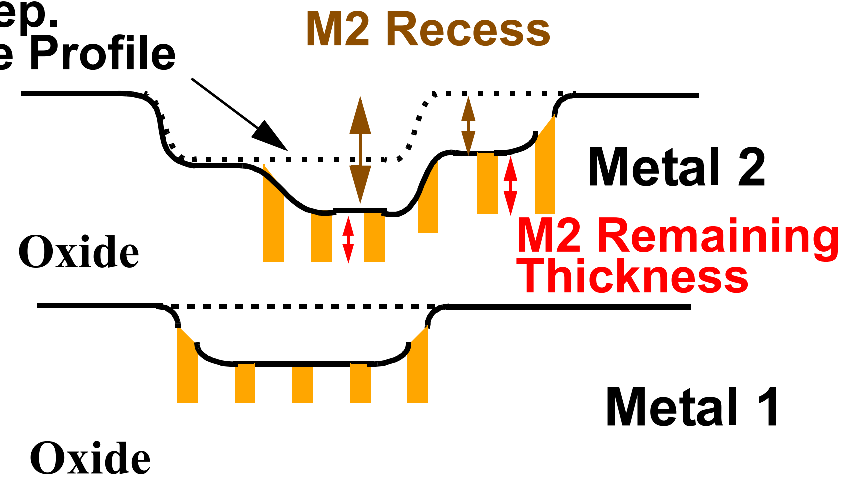
1. M1 Polish



3. M2 Cu Deposition

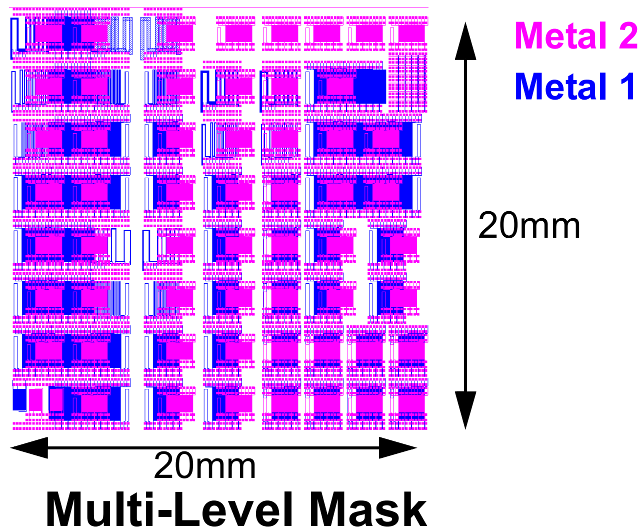


2. M2 Oxide Deposition



4. M2 Polish

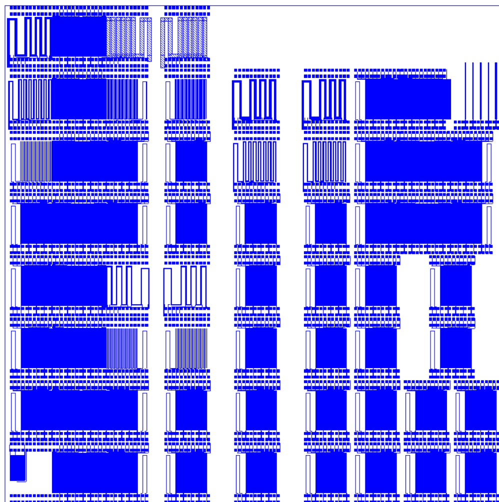
Multilevel Copper CMP Test Mask Design



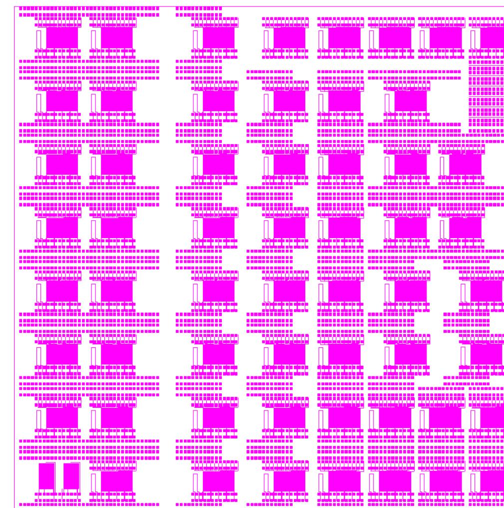
Multi-Level Mask

- Multi-level mask: M1, Via, and M2
  - electrical and physical test structures
- Single level effects: Layout factors on M1 to study creation of topography
  - Density
  - Pitch (Line Width & Line Space)
- Multiple metal level effects: Overlay M2 structures to study topography impact

Metal 1



Metal 2



M1 Structure Design Space

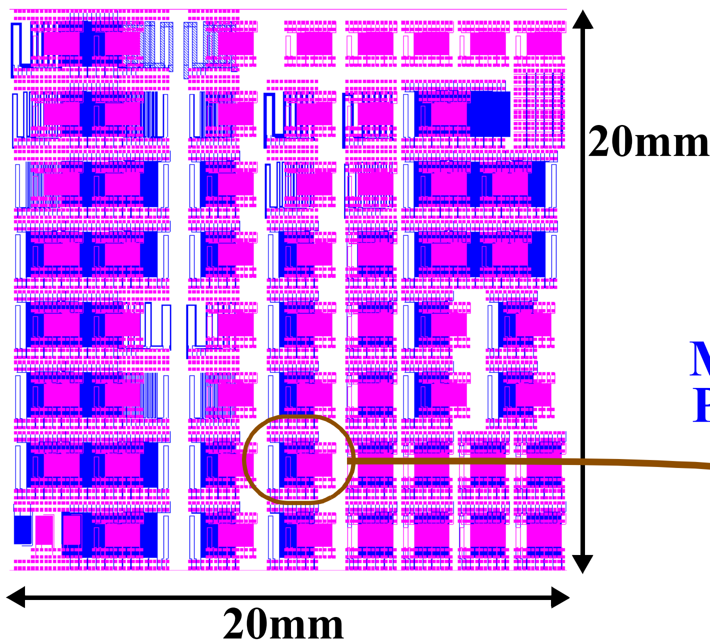
M1 Structure Design Space (in μm): < P2D50 = Pitch of 2 and Density of 50% >

	LW															
LS	0	0.18	0.25	0.5	1	1.5	2	3	4	5	7	9	10	50	90	100
0													**D100 Solid**			
0.18		**P0.36 D50**														
0.25			**P0.5 D50**													
0.5				**P1 D50**		**P2 D67**										
1					**P2 D50**			**P4 D75**		**P6 D83**		**P10 D90**		**P51 D98**		**P101 D99**
1.5				**P2 D33**												
2							**P4 D50**									
3					**P4 D25**						**P10 D70**					
4																
5					**P6 D17**					**P10 D50**						
7								**P10 D30**								
9					**P10 D10**											
10													**P20 D50**		**P100 D90**	
50					**P51 D2**									**P100 D50**		
90													**P100 D10**			
100					**P101 D1**											**P200 D50**

Multilevel CMP Test Structure Design

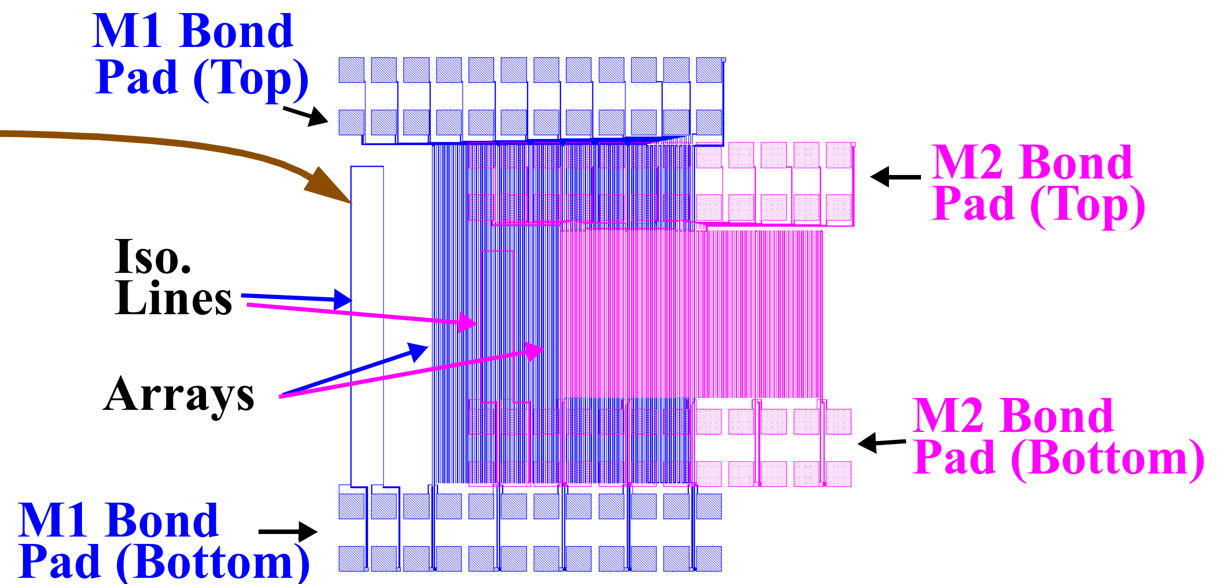
- Multi-level mask: M1, Via, and M2 with electrical and physical test structures.
- Layout factors: Line width/line space combinations
- Focus: Multi-level pattern effects
- Overlap structures: direct, half, and dual

Mask Layout
("SEMATECH 954 Mask")



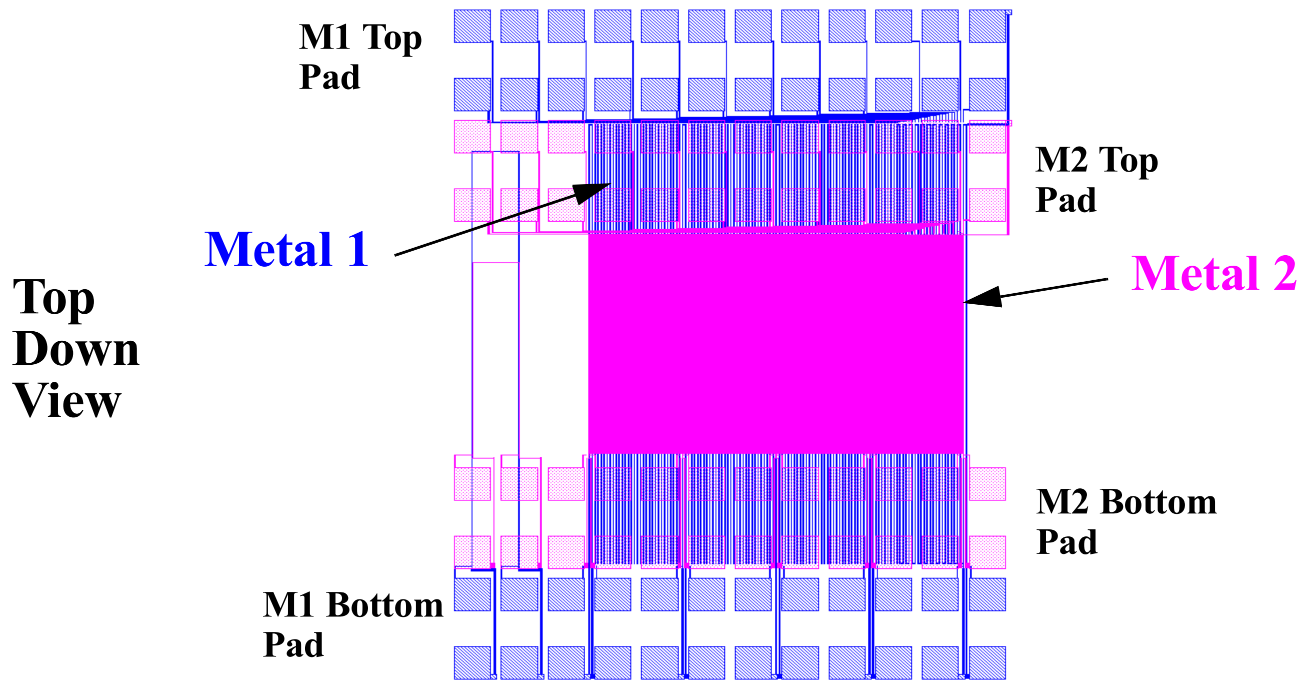
Metal 1: Blue
Metal 2: Magenta

Half Overlap Structure

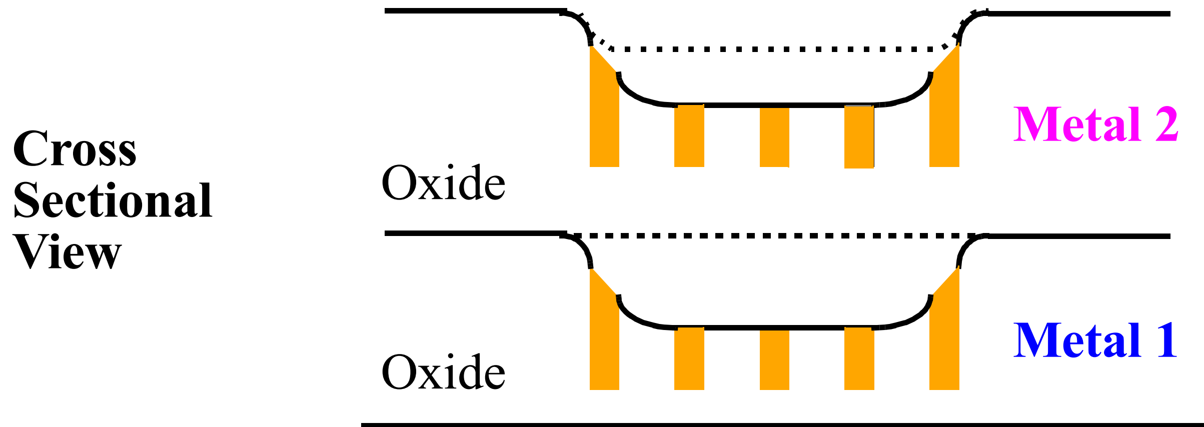


Direct Overlap: Structure

Top Down View



Cross Sectional View



Direct Overlap: Data Analysis

Iso. Lines

M2: Electrically Extracted

M2 Remain. Thick. (μm)

0.8
0.7
0.6
0.5

Overlap

No Overlap

M2: Surface Scan

M2 Recess (Å)

0
−1000
−2000

Iso. Lines

M1 Remain. Thick. (μm)

0.8
0.7
0.6
0.5

M1: Electrically Extracted

−500 0 500 1000 1500 2000 μm

As Dep. Oxide Profile

Oxide

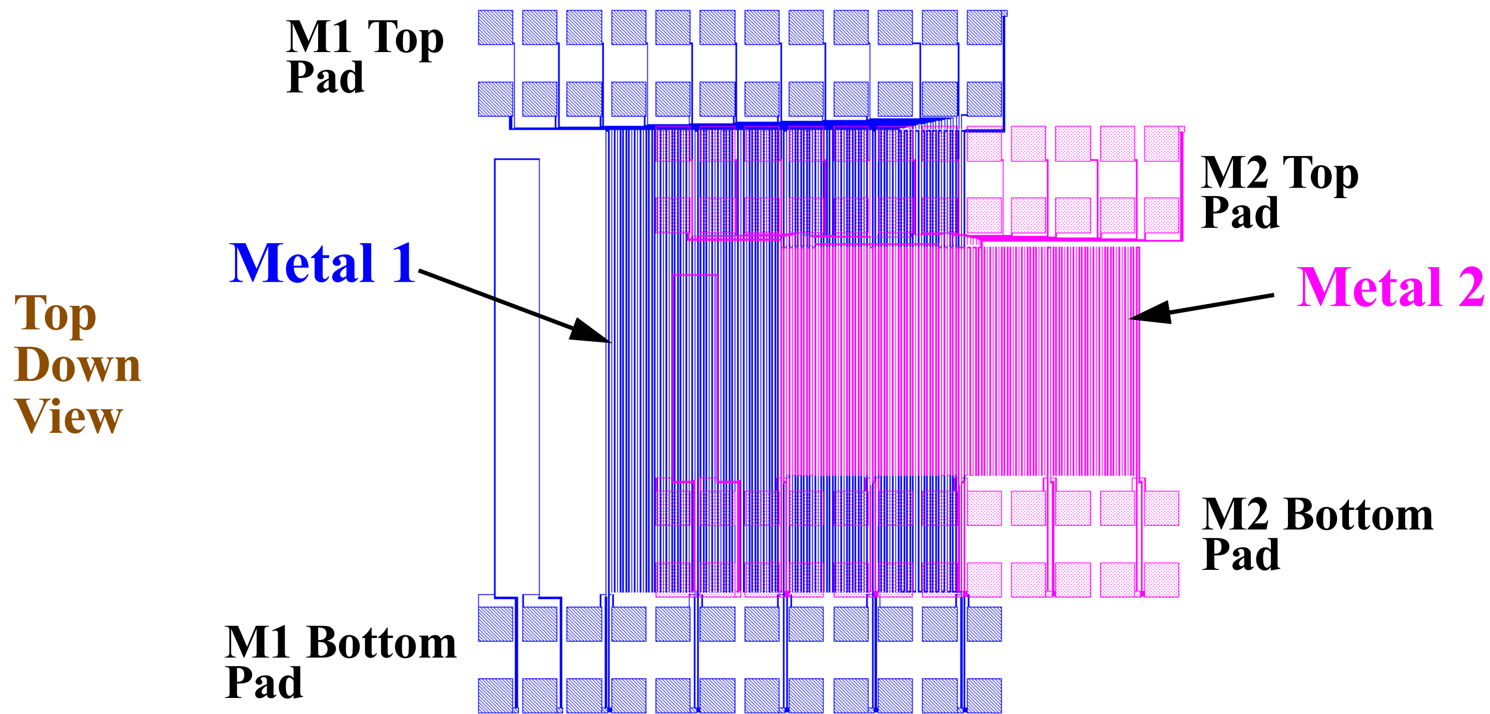
Metal 2

Oxide

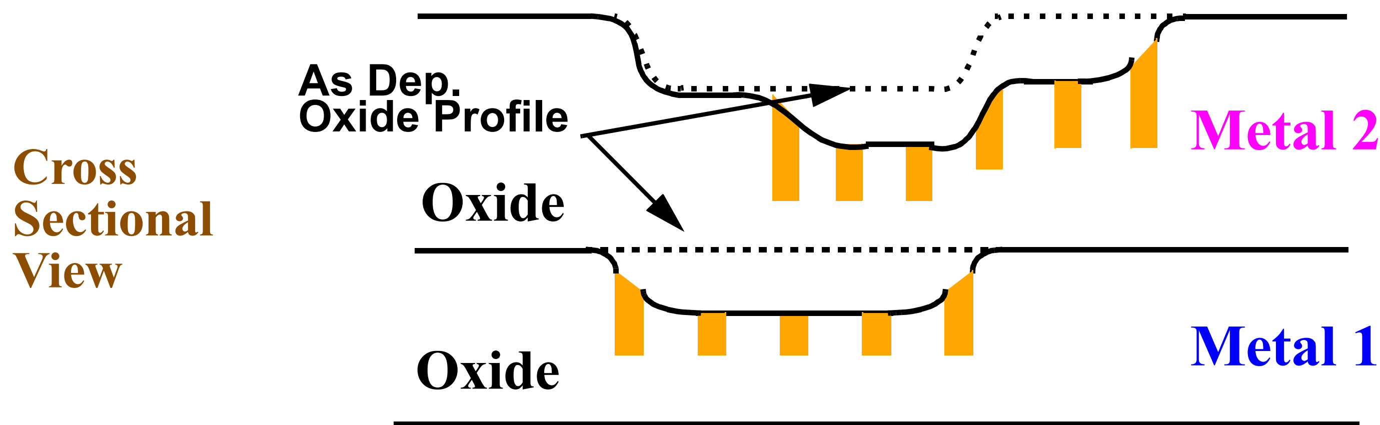
Metal 1

Multilevel Half Overlap Structure

Top Down View



Cross Sectional View



Half Overlap: Erosion to Erosion

M2: Electrically Extracted

M2 Remain. Thick. (μm)

0.8 0.7 0.6 0.5

← Ref.

M2: Surface Scan

M2 Recess (Å)

0 −1000 −2000

Over Struct.

Over Oxide

Iso. Lines

M1: Electrically Extracted

M1 Remain. Thick. (μm)

0.8 0.7 0.6 0.5

0 500 1000 1500 2000 2500 μm

As Dep. Oxide Profile

Oxide

Metal 2

Oxide

Metal 1

Half Overlap: Dishing to Erosion

M2 Profile (Å)

0.5μm Lw/
0.5μm Ls

M2 Array

No Overlap Region

Over Struct.

Over Oxide

0
–500
–1000
–1500
–2000

0 500 1000 1500 2000 2500 3000

M1 Profile (Å)

50μm Lw/
50μm Ls

Dishing Dominant

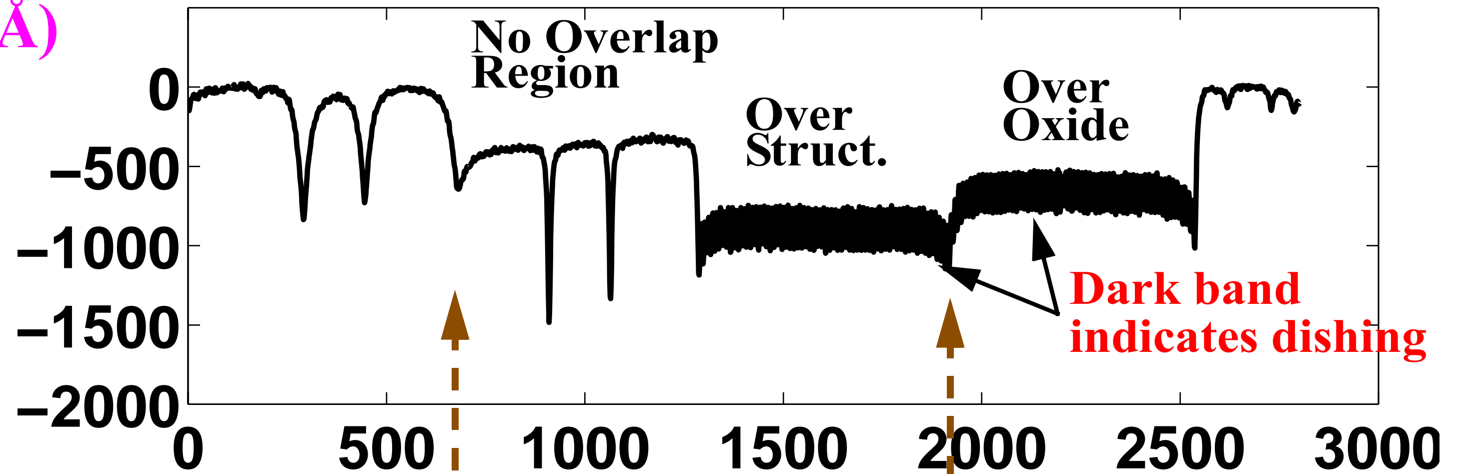
0
–500
–1000
–1500
–2000

0 500 1000 1500 2000 2500 3000

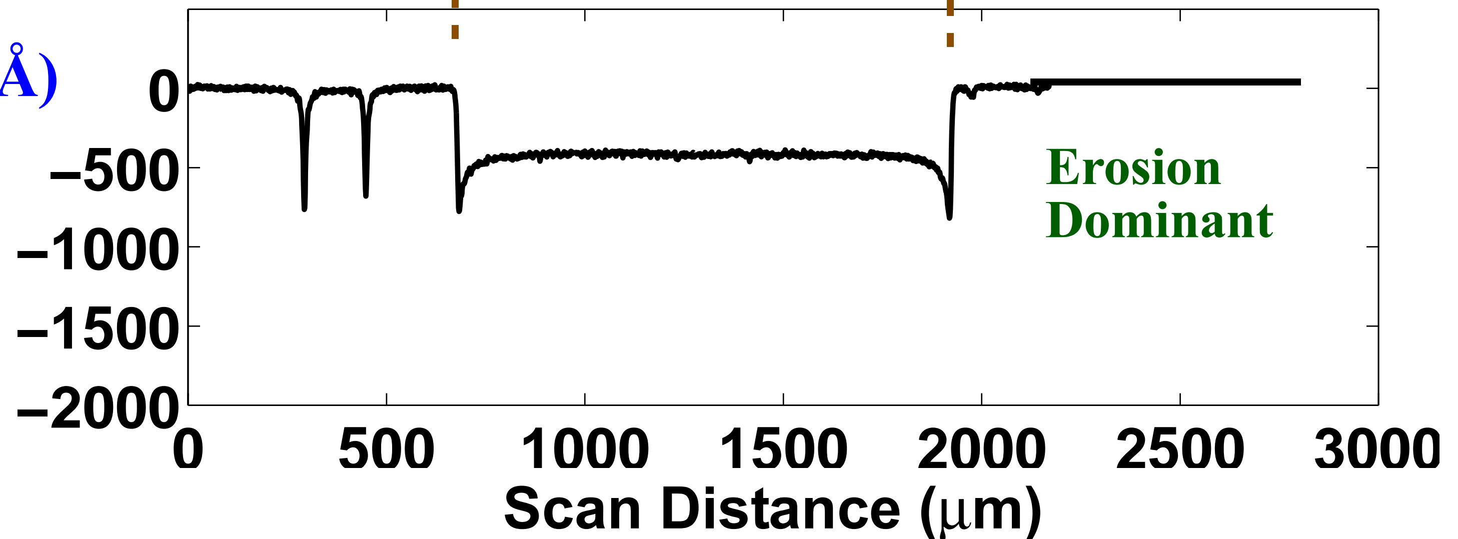
Scan Distance (μm)

Half Overlap: Erosion to Dishing/Erosion

M2 Profile (Å)
5μm Lw/
5μm Ls



M1 Profile (Å)
1μm Lw/
1μm Ls



Dual Overlap: Structure

M1 Top Pad

Metal 1

Top Down View

M2 Top Pad

Metal 2

M2 Bottom Pad

M1 Bottom Pad

Oxide

Metal 2

As Dep. Oxide Profile

Cross Sectional View

Oxide

Metal 1

Dual Overlap: Data Analysis

M2 Electrically Extracted

M2 Remain. Thick. (μm)

0.8
0.7
0.6
0.5

Ref.

Iso. Lines

M2: Surface Scan

M2 Recess (Å)

0
−1000
−2000

Over Struct.1

Over Struct.2

M1: Electrically Extracted

M1 Remain. Thick. (μm)

0.8
0.7
0.6
0.5

0 500 1000 1500 2000 2500 3000 μm

Oxide

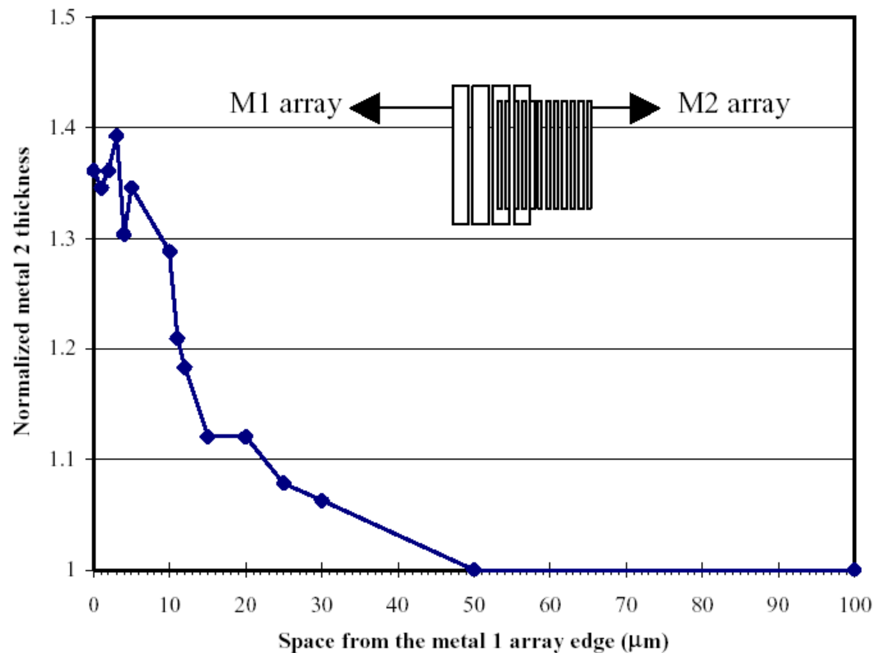
As Dep. Oxide Profile

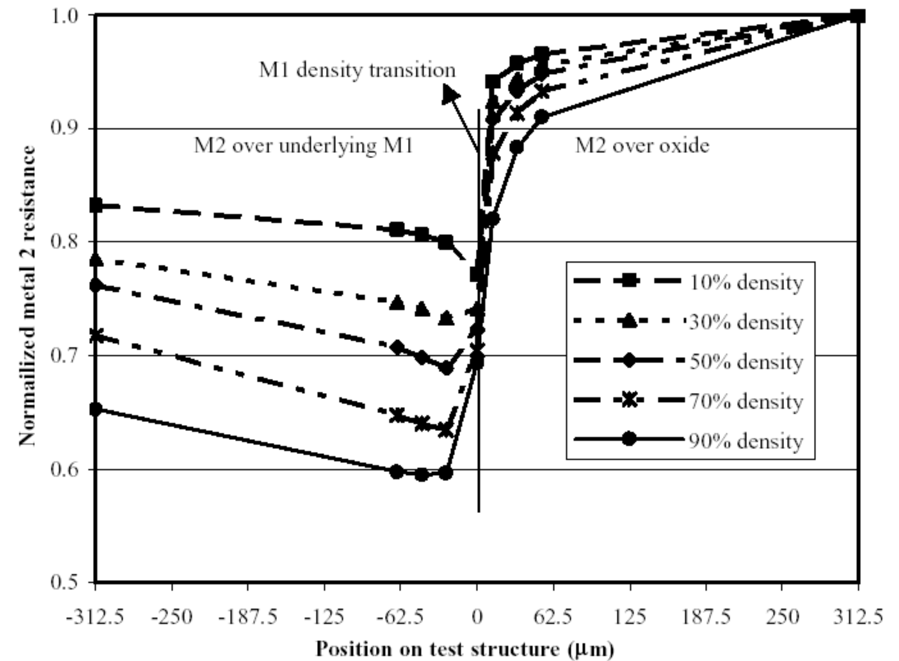
Metal 2

Oxide

Metal 1

Multilevel Electrical Impact: M2 Line Thickness





- Metal 2 thickness (0.5 μm line/space) as function of space from the edge of the metal 1 array (3 μm line/1mm sapce)
- Change in resistance of a 0.5 μm mtetal 2 line/space structure at a transition in metal 1 density

Lakshminarayanan et al. (LSI Logic), IITC 2002.

Design Rule Generation

Lakshminarayanan et al.
(LSI Logic), IITC 2002.

Modeling of Pattern Effects in Copper CMP

- Approach: Apply density/ step-height model to each stage in the copper polish process

Stage 1 bulk copper removal

Stage 2 barrier removal

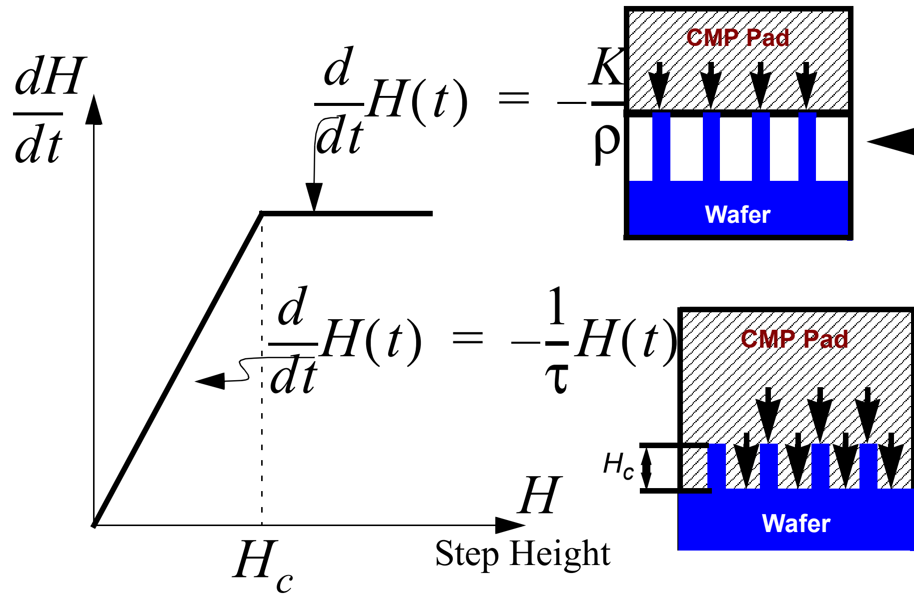
Stage 3 over-polish

Oxide Erosion

Metal Dishing

- "Removal Rate" Diagrams:
  - Track RR for metal and oxide during each phase
- Approximation: neglect barrier removal phase

Pattern-Density / Step-Height Effects

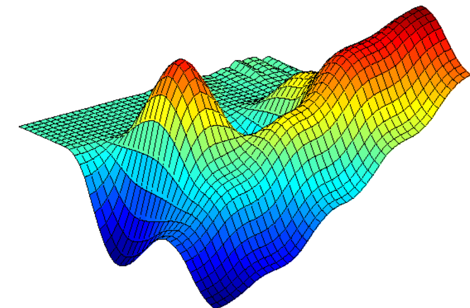


- For large step heights:
  - step height reduction goes as 1/pattern-density
- For small step heights (less than the "contact height"):
  - height reduction proportional to height
  - height decays with time constant τ:

$$H(t) = H_0 e^{-t/\tau}$$

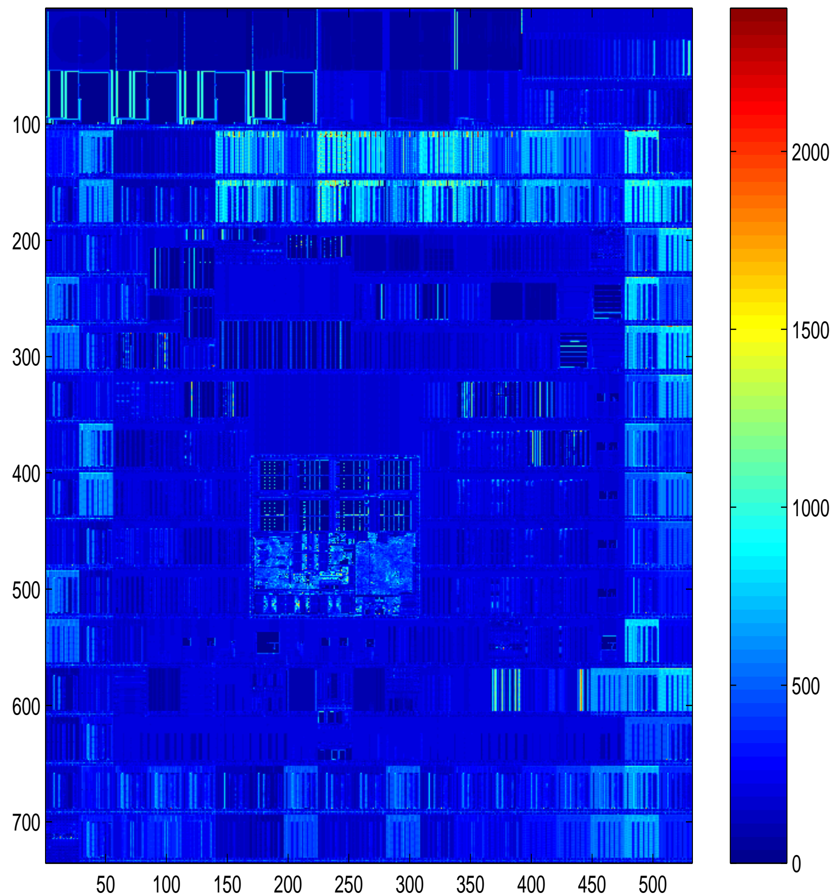
- Calculate *effective density* by averaging local pattern densities over some window/ weighting function

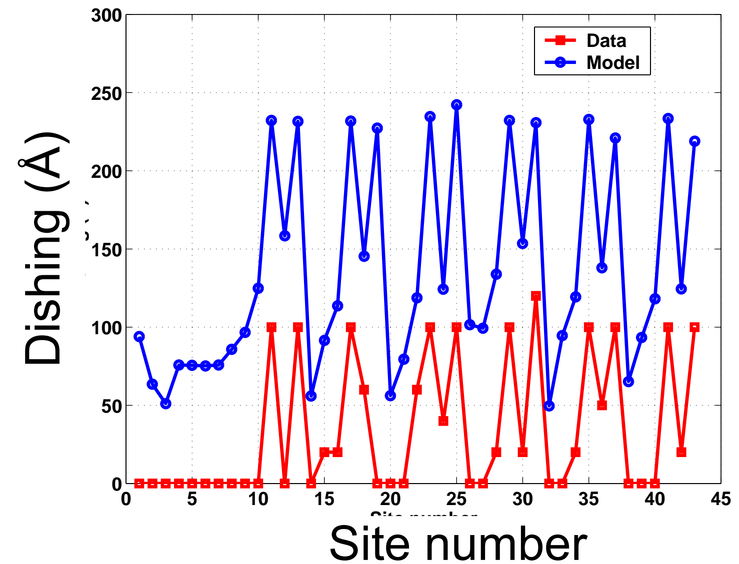
Effective Density Map Over Chip



Ouma et al., *IITC '98*;
Smith et al., *CMPMIC '99*
Grillaert et al., *CMP-MIC '98.*

Chip-Scale CMP Simulation





Dishing after step two

RMS Error = 155 Å

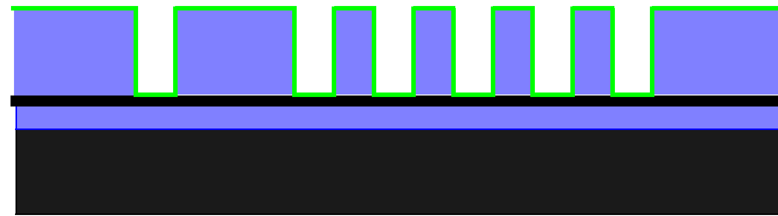
Outline

- Background
- Copper CMP Characterization
- Copper Electroplating Characterization
  - Definitions
  - Test Structure and Measurement Plan
  - Trend Analysis
  - Chip Scale Modeling
  - Integrated Plating/CMP Chip-Scale Modeling
- Conclusions

Copper Electroplating Non-Uniformities

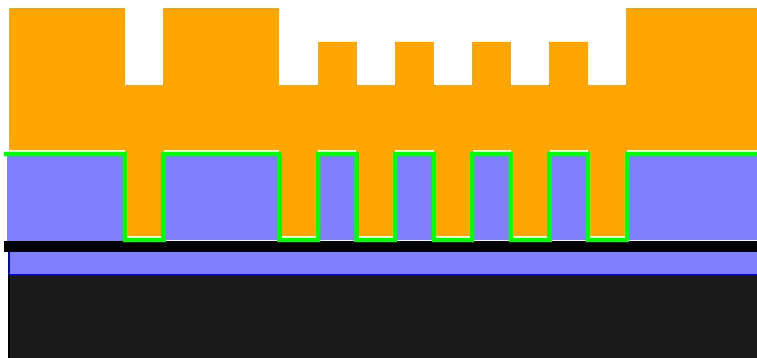
Isolated Line

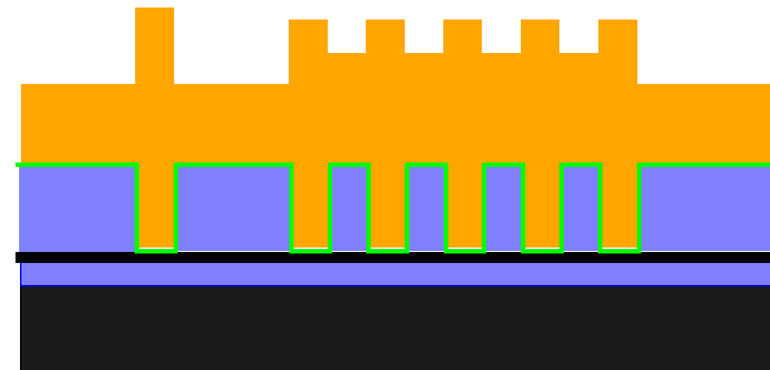
Array Region



Conventional Fill

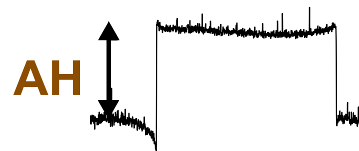
Super Fill (Bottom-Up Fill)



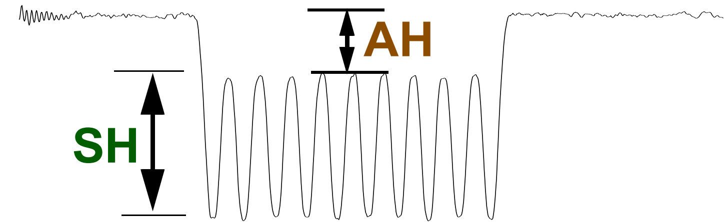


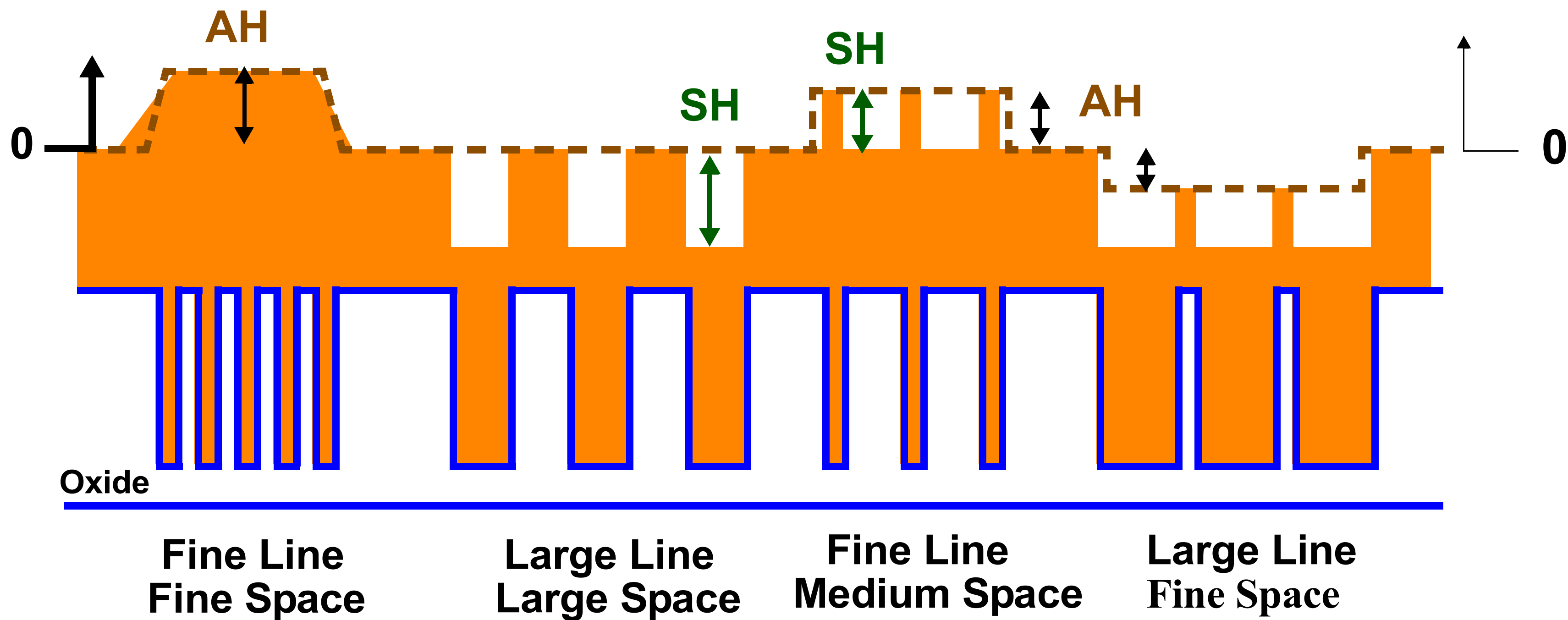
- Isolated line and array region are recessed
- Isolated line sticks up and array region is bulged

Electroplating Pattern Dependent Effects



Sample Profilometer Scans





Fine Line Fine Space

Large Line Large Space

Fine Line Medium Space

Large Line Fine Space

AH: Array Height

SH: Step Height

Measurement Plan and Sample Profile Scan

- Profile scans taken across each line/array structure

Profile Scan

X X

Thickness Measurement

Isolated Line

Array Region

Test Mask

Step Height
(Isolated Line)

Bulge

Superfill

Step Height
(Array Line)

Recess

Step Height
(Isolated Line)

Conformal Fill

Zoom
into array

Electroplated Profile Trends: Pitch Structures

Height (Å)

0.25/0.25μm

0.3/0.3μm

0.35/0.35μm

Lw/Ls

0.5/0.5μm

0.7/0.7μm

1/1μm

Trace Length (μm)

Superfill Behavior

Conformal Behavior

2/2μm

5/5μm

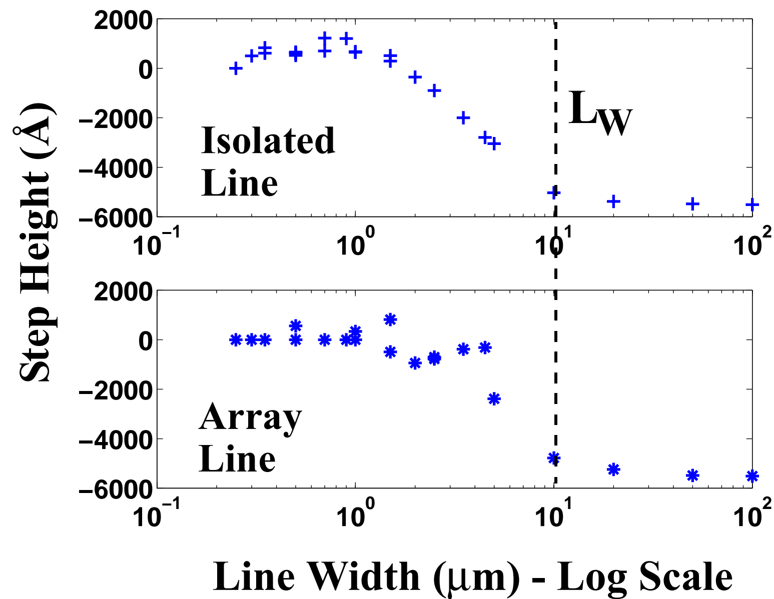
10/10μm

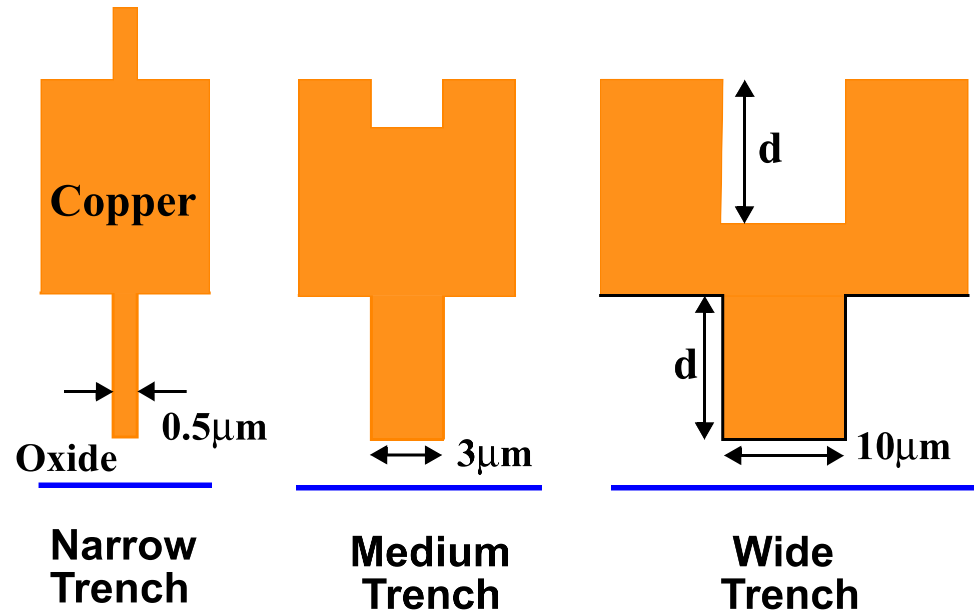
20/20μm

50/50μm

100/100μm

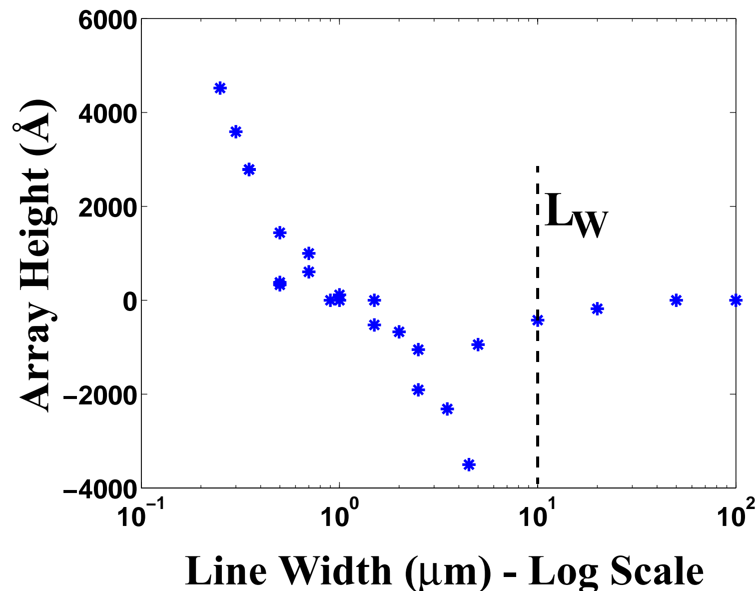
Step Height Data Analysis

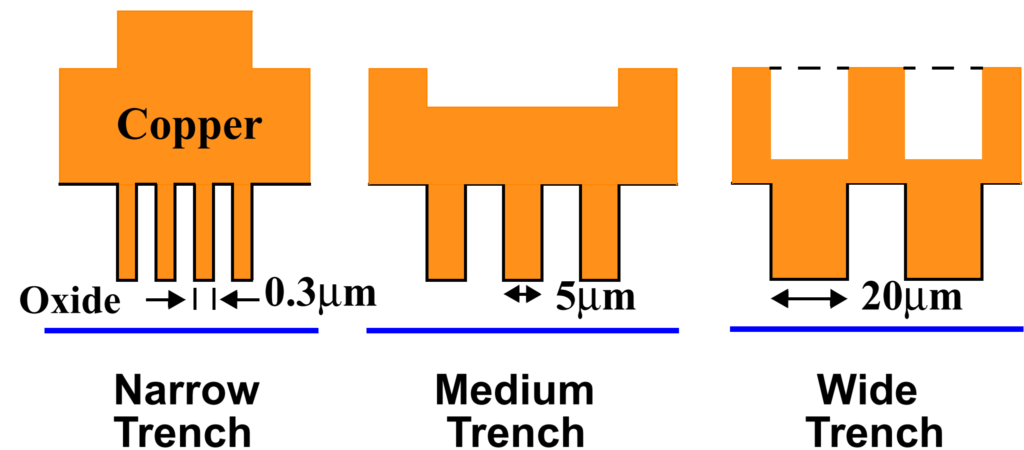




- Trends
  - SH depends on line width: near zero or positive (superfill) for small features and becomes more conformal as line width increases
- Saturation Length: fill becomes fully conformal and SH = Trench Depth
  - Line width L_W = 10µm

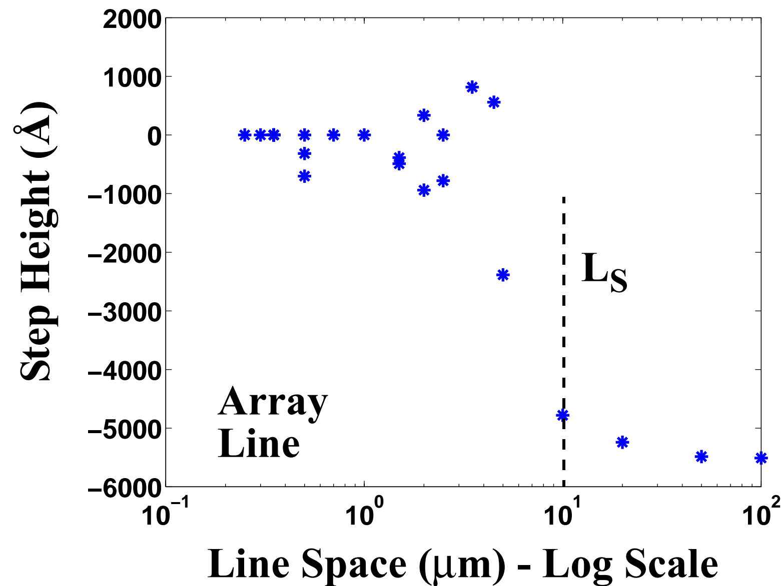
Array Height Data Analysis

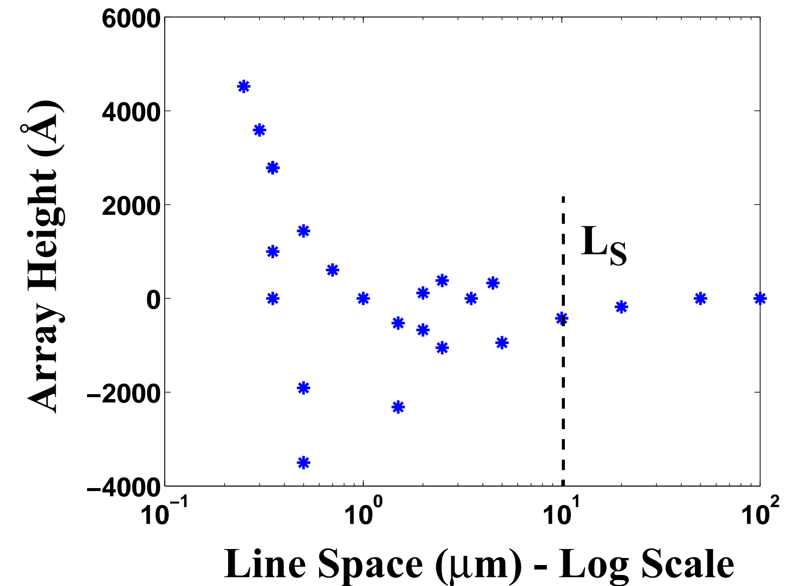




- Trends
  - Positive (superfill) for small features, and becomes negative (conformal), and saturates to field level as line width increases
- Saturation length: fill becomes fully conformal and AH = 0Å
  - Line width L_W = 10μm

SH and AH vs. Line Space



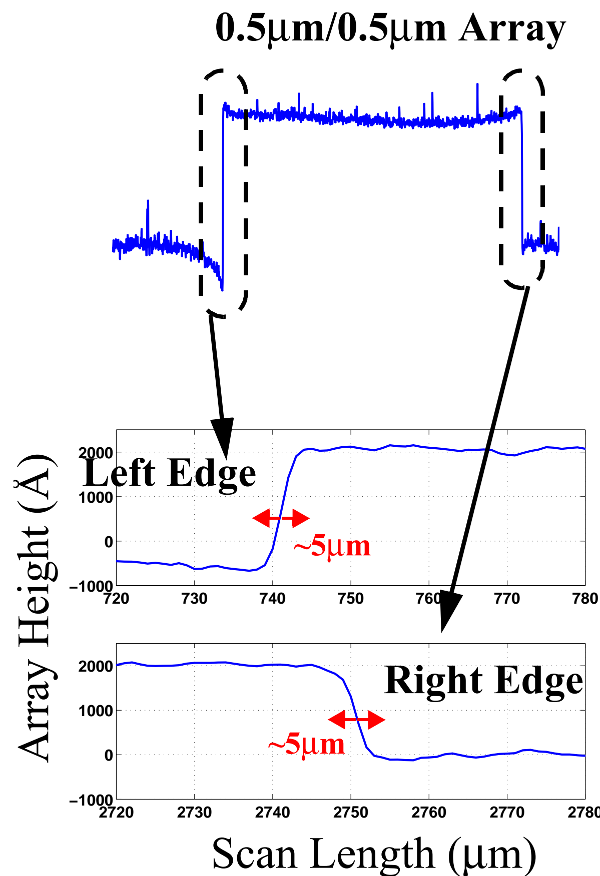


- Trends
  - Line space dependency for SH and AH is similar to line width dependency
- Saturation length: similar value is observed for line space
  - Line space L_S = 10μm

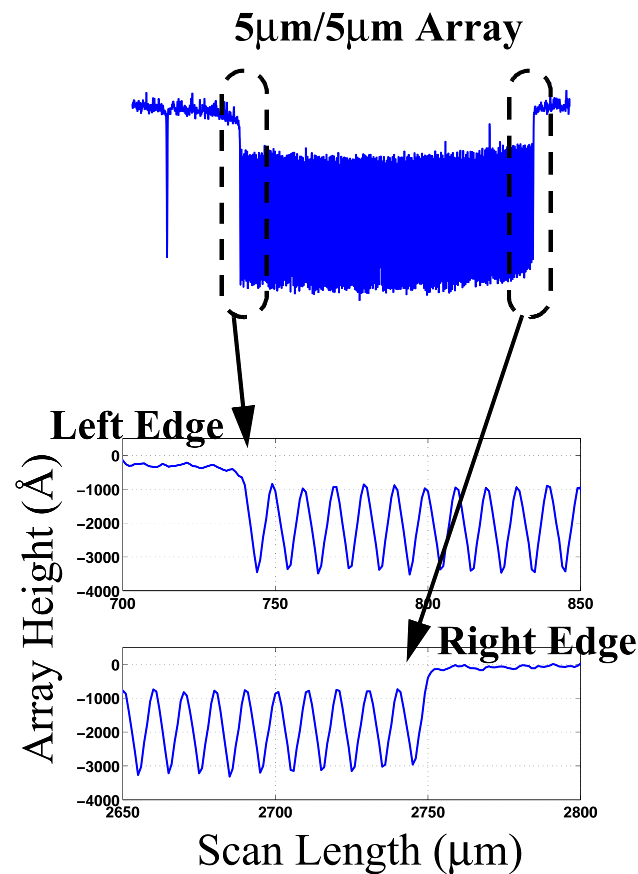
Transition Length Scale in Electroplating

- Plating depends on local feature (feature scale) and nearest neighbors within 2-5μm range

Array Height Profile Scans

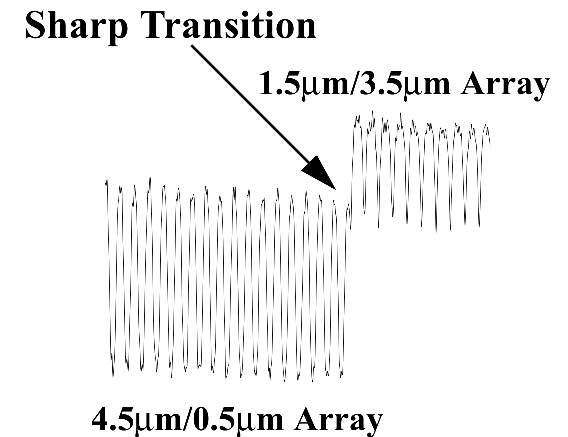


Superfill



Conventional fill

Array to Array Transition



Semi-Empirical Model for Topography Variation

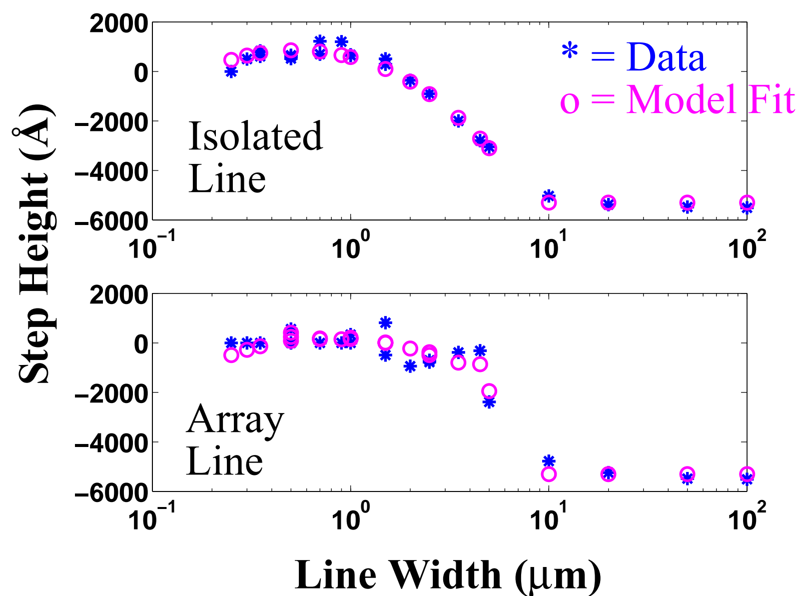
- Physically Motivated Model Variables:
  - Width, Space, 1/Width, and Width*Space
- Semi-Empirical Model Development
  - Capture both conformal regime and superfill regime in one model frame
  - $1/W^2$ and W^2 terms explored as well
- Model Form
  - Array Height:

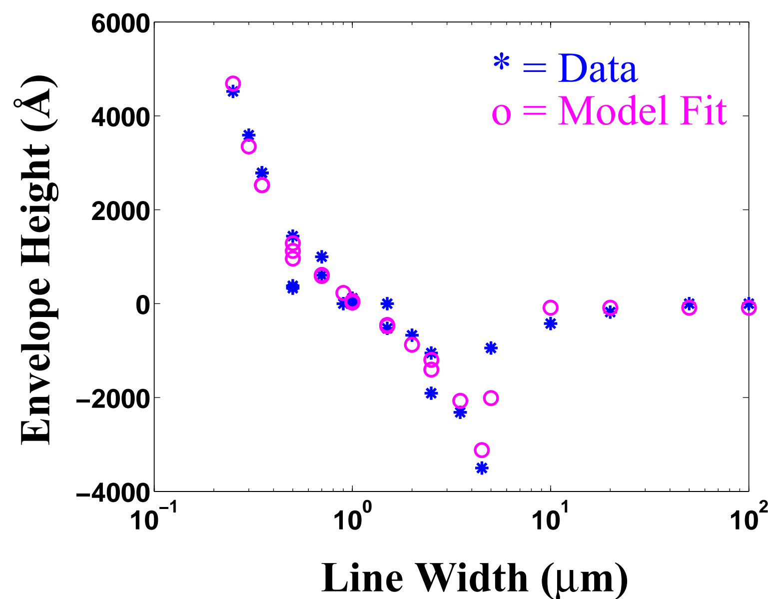
$$AH = a_E W + b_E W^{-1} + c_E W^{-2} + d_E S + e_E W \times S + Const_E$$

  - Step Height:

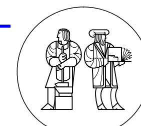
$$SH = a_S W + b_S W^{-1} + c_S W^2 + d_S S + e_S W \times S + Const_S$$

Model Fit: Step Height and Array Height



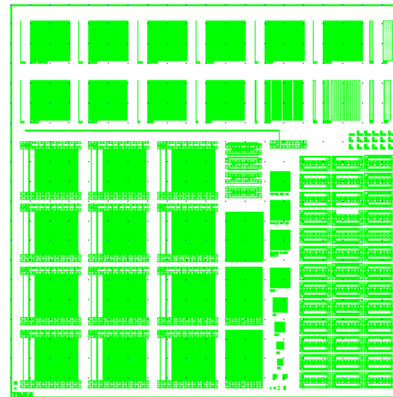


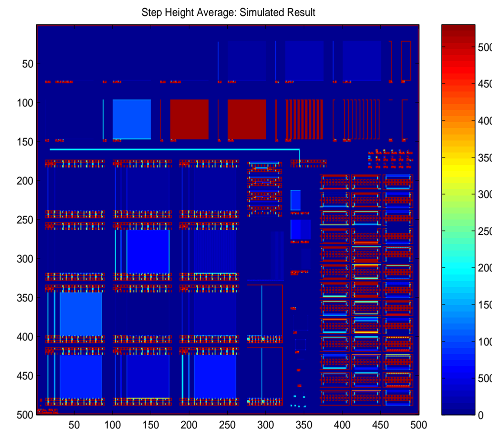
- The models capture both trends well
  - Step Height RMS error = 327 Å
  - Array Height RMS error = 424 Å
- Model coefficients are calibrated and used for chip-scale simulations



Chip-Scale Simulation Calibration Results

Test Mask

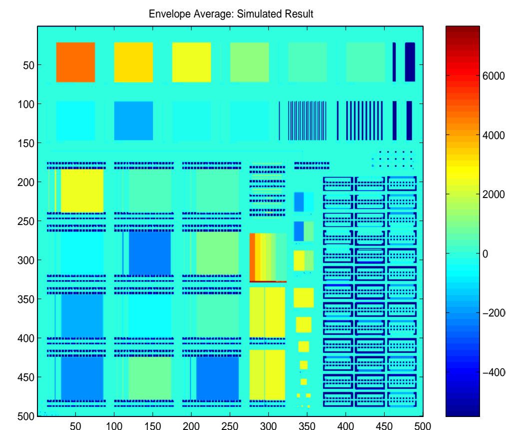


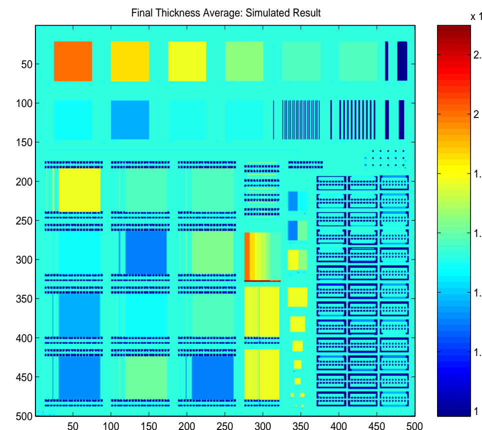


Step Height

RMS Error=420Å

Array Height





Final Thickness

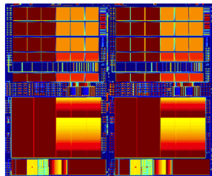
RMS Error=440Å

- Simulated over the entire test mask used to calibrate the model
- RMS errors are slightly greater (about 90Å and 10Å more) than fitting RMS errors since distribution values are used

Integration of Electroplating and CMP Models

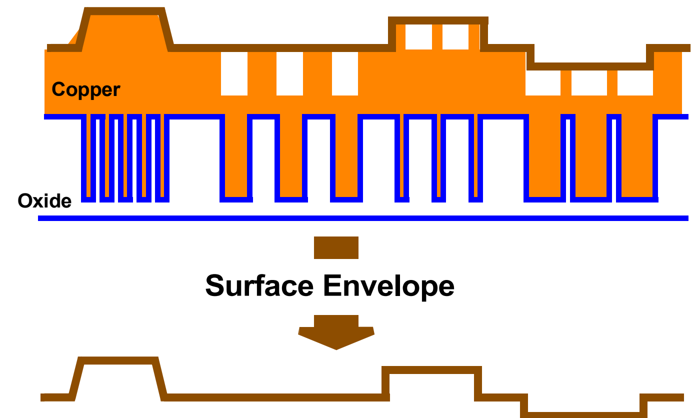
- Integration is done by feeding forward the simulated result from electroplating to copper CMP simulation

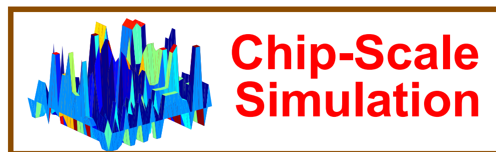
Product Chip Layout



Layout Parameter Extraction

- Electroplating Simulation:
  - Array Height
  - Step Height
  - Topography Pattern Density





Chip-Scale Simulation

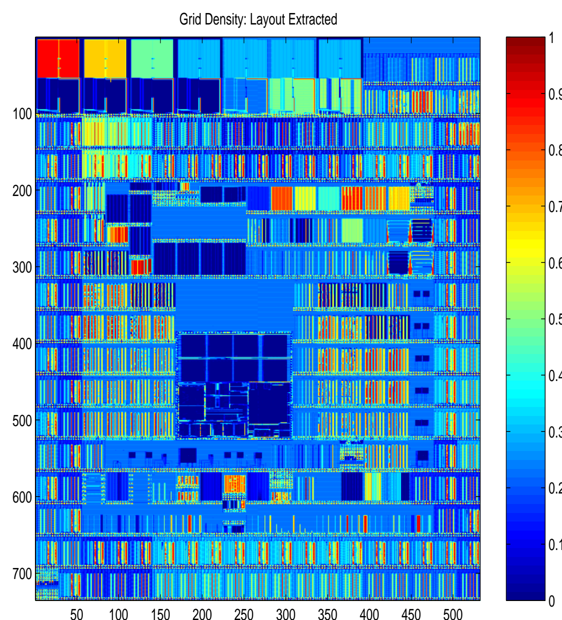
Calibrated Copper Pattern Dependent CMP Model

- CMP model needs:
  - Surface "envelope": Array Height
  - Step Height
  - Topography Pattern Density

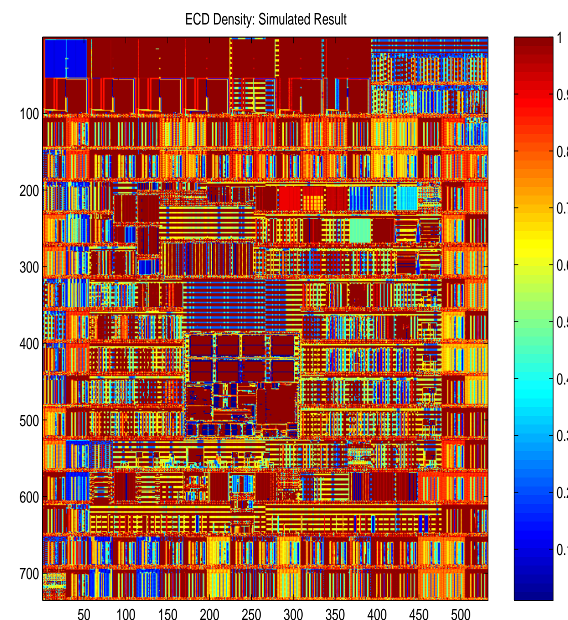
Prediction of dishing and erosion

Topography Pattern Density

- Topography density: as-plated surface topography pattern density of raised features
  - Depends on plating characteristics
  - Important as an input for CMP pattern density model

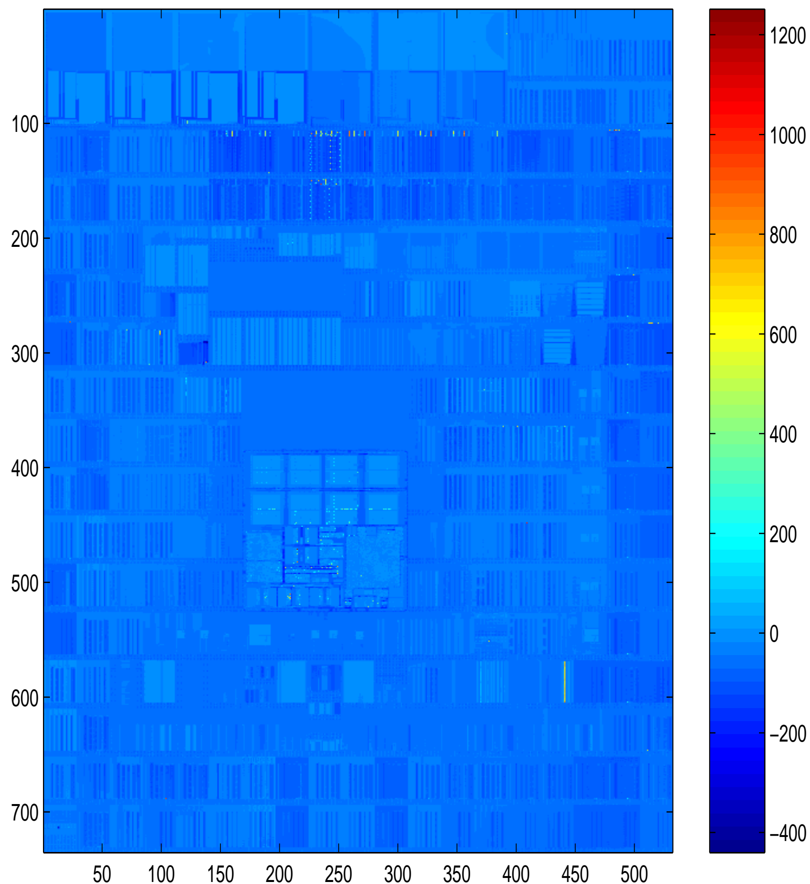


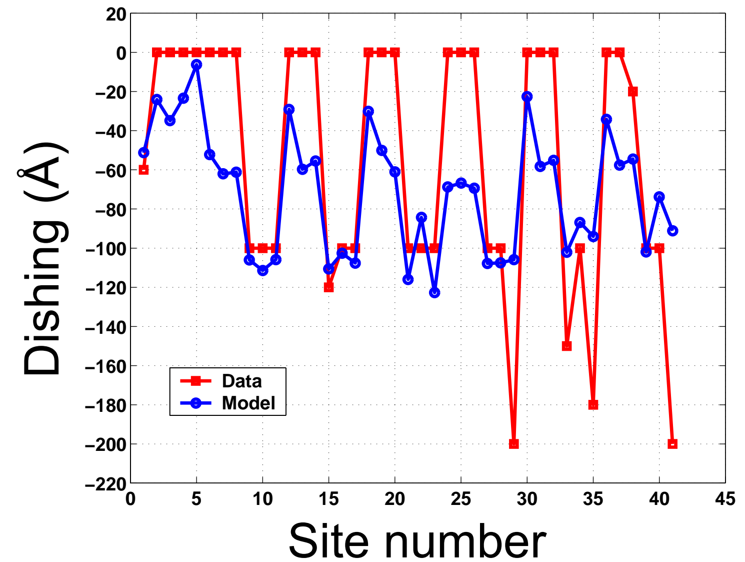
Layout Density



Topography Density

Plating/CMP: Final Dishing

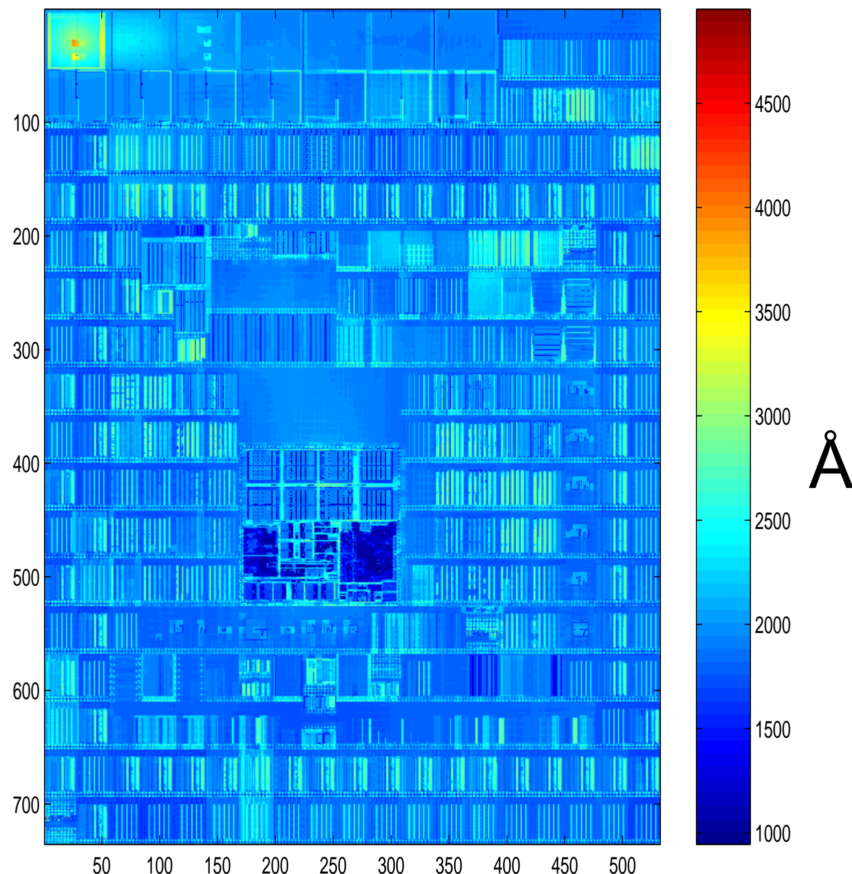


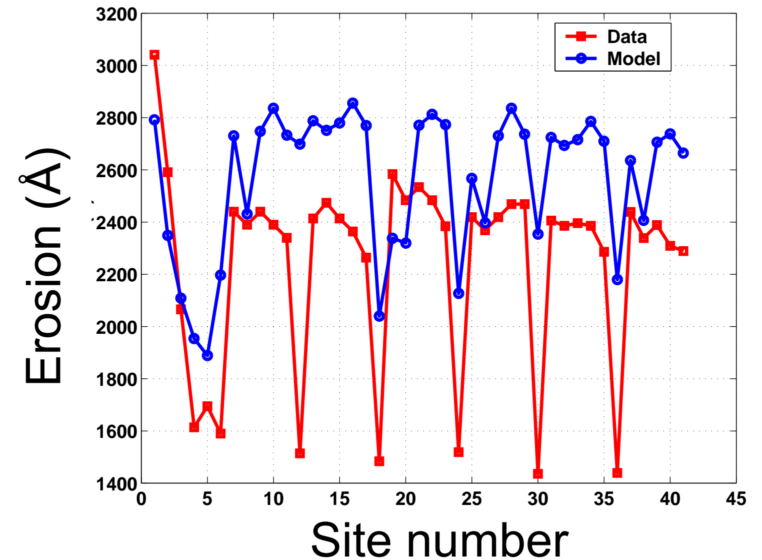


Dishing after step three

RMS Error = 140 Å

Plating CMP: Final Erosion





Erosion after step three

RMS Error = 420 Å

Conclusion

- Electroplating and CMP are Highly Pattern Dependent
- Copper Interconnect Pattern Dependent Characterization
  - Test Structure Design
    - Capture Key Pattern Effects: Isolated vs. Array, Density, Pitch, etc.
    - Three Polishing Length Scales: mm, 100μm, and 1μm Ranges.
  - Mask Design
    - Single layer
    - Multi layer
  - Physical and Electrical Measurements
  - Data Analysis
- Can Be Applied to Support Process Development, Optimization, and Formulation Of Design Rules
- Provides Data for Chip-Scale Modeling of Copper Interconnect

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